## Data Sheet

## FEATURES

Latch-up proof 8 kV HBM ESD rating Low on resistance (<10 $\Omega$ ) $\pm 9 \mathrm{~V}$ to $\pm 22 \mathrm{~V}$ dual-supply operation 9 V to 40 V single-supply operation 48 V supply maximum ratings<br>Fully specified at $\pm 15 \mathrm{~V}, \pm \mathbf{2 0} \mathrm{V},+12 \mathrm{~V}$, and $+\mathbf{3 6} \mathrm{V}$<br>$\mathrm{V}_{\mathrm{ss}}$ to $\mathrm{V}_{\mathrm{DD}}$ analog signal range

## APPLICATIONS

## Relay replacement

Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAMS


SWITCHES SHOWN FOR A LOGIC 1 INPUT. 彥
Figure 1. TSSOP Package


SWITCHES SHOWN FOR A LOGIC 1 INPUT.
Figure 2. LFCSP Package

## PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low Ron.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5436 can be operated from dual supplies up to $\pm 22 \mathrm{~V}$.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5436 can be operated from a single-rail power supply up to 40 V .
5. 3 V logic compatible digital inputs: $\mathrm{V}_{\mathrm{INH}}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=0.8 \mathrm{~V}$.
6. No $\mathrm{V}_{\mathrm{L}}$ logic power supply required.

Rev. C

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ADG5436

## SPECIFICATIONS

$\pm 15$ V DUAL SUPPLY
$\mathrm{V}_{\mathrm{DD}}=+15 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{SS}}=-15 \mathrm{~V} \pm 10 \%$, GND $=0 \mathrm{~V}$, unless otherwise noted.
Table 1.

| Parameter | $25^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |
| Analog Signal Range |  |  | $V_{D D}$ to $V_{S S}$ | V |  |
| On Resistance, Ron | 9.8 |  |  | $\Omega$ typ | $\mathrm{V}_{\mathrm{S}}= \pm 10 \mathrm{~V}, \mathrm{I}_{\mathrm{S}}=-10 \mathrm{~mA}$; see Figure 25 |
|  | 11 | 14 | 16 | $\Omega$ max | $\mathrm{V}_{\mathrm{DD}}=+13.5 \mathrm{~V}, \mathrm{~V}_{\text {SS }}=-13.5 \mathrm{~V}$ |
| On-Resistance Match Between Channels, $\Delta$ Ron | 0.35 |  |  | $\Omega$ typ | $\mathrm{V}_{\mathrm{s}}= \pm 10 \mathrm{~V}, \mathrm{I}_{\mathrm{s}}=-10 \mathrm{~mA}$ |
|  |  |  |  |  |  |
|  | 0.7 | 0.9 | 1.1 | $\Omega$ max |  |
| On-Resistance Flatness, Rflat (on) | 1.2 |  |  | $\Omega$ typ | $\mathrm{V}_{\mathrm{s}}= \pm 10 \mathrm{~V}, \mathrm{I}_{\mathrm{s}}=-10 \mathrm{~mA}$ |
|  | 1.6 | 2 | 2.2 | $\Omega$ max |  |
| LEAKAGE CURRENTS Source Off Leakage, Is (Off) |  |  |  |  | $\mathrm{V}_{\mathrm{DD}}=+16.5 \mathrm{~V}, \mathrm{~V}_{\text {SS }}=-16.5 \mathrm{~V}$ |
|  | $\pm 0.05$ |  |  | nA typ | $\mathrm{V}_{S}= \pm 10 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=\mp 10 \mathrm{~V}$; see Figure 28 |
|  | $\pm 0.25$ | $\pm 0.75$ | $\pm 6$ | nA max |  |
| Drain Off Leakage, $\mathrm{l}_{\mathrm{D}}$ (Off) | $\pm 0.1$ |  |  | nA typ | $\mathrm{V}_{\mathrm{S}}= \pm 10 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=\mp 10 \mathrm{~V}$; see Figure 28 |
|  | $\pm 0.4$ | $\pm 2$ | $\pm 12$ | nA max |  |
| Channel On Leakage, ld (On), Is (On) | $\pm 0.1$ |  |  | nA typ | $\mathrm{V}_{\mathrm{S}}=\mathrm{V}_{\mathrm{D}}= \pm 10 \mathrm{~V}$; see Figure 24 |
|  | $\pm 0.4$ | $\pm 2$ | $\pm 12$ | nA max |  |
| DIGITAL INPUTS |  |  |  |  |  |
| Input High Voltage, $\mathrm{V}_{\text {INH }}$ |  |  | 2.0 | $\checkmark$ min |  |
| Input Low Voltage, $\mathrm{V}_{1 \mathrm{IL}}$ |  |  | 0.8 | $V$ max |  |
| Input Current, linl or linh | 0.002 |  |  | $\mu \mathrm{A}$ typ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{GND}}$ or $\mathrm{V}_{\mathrm{DD}}$ |
|  |  |  | $\pm 0.1$ | $\mu \mathrm{A}$ max |  |
| Digital Input Capacitance, $\mathrm{Cl}_{\text {IN }}$ | 5 |  |  | pF typ |  |
| DYNAMIC CHARACTERISTICS ${ }^{1}$ |  |  |  |  |  |
| Transition Time, ttransition | 170 |  |  | ns typ | $\mathrm{RL}=300 \Omega, \mathrm{CL}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  | 235 | 285 | 316 | ns max | $\mathrm{V}_{\mathrm{s}}=10 \mathrm{~V}$; see Figure 31 |
| ton | 173 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  | 230 | 280 | 351 | $n \mathrm{nmax}$ | $\mathrm{V}_{\mathrm{s}}=10 \mathrm{~V}$; see Figure 33 |
| toff | 124 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  | 160 | 193 | 218 | ns max | $\mathrm{V}_{\mathrm{s}}=10 \mathrm{~V}$; see Figure 33 |
| Break-Before-Make Time Delay, $\mathrm{t}_{\mathrm{D}}$ | 55 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  |  |  | 18 | $n s$ min | $\mathrm{V}_{\mathrm{s} 1}=\mathrm{V}_{52}=10 \mathrm{~V}$; see Figure 32 |
| Charge Injection, Qinj | 200 |  |  | pC typ | $\begin{aligned} & \mathrm{V}_{\mathrm{S}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=0 \Omega, \mathrm{C}_{\mathrm{L}}=1 \mathrm{nF} \text {; } \\ & \text { see Figure } 34 \end{aligned}$ |
| Off Isolation | -78 |  |  | dB typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ; \\ & \text { see Figure } 27 \end{aligned}$ |
| Channel-to-Channel Crosstalk | -58 |  |  | dB typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ; \\ & \text { see Figure } 26 \end{aligned}$ |
| Total Harmonic Distortion + Noise | 0.009 |  |  | \% typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, 15 \mathrm{~V} \mathrm{p}-\mathrm{p}, \mathrm{f}=20 \mathrm{~Hz} \text { to } 20 \mathrm{kHz} \text {; } \\ & \text { see Figure } 29 \end{aligned}$ |
| -3 dB Bandwidth | 102 |  |  | MHz typ | $\mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{L}=5 \mathrm{pF}$; see Figure 30 |
| Insertion Loss | -0.7 |  |  | dB typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ; \\ & \text { see Figure } 30 \end{aligned}$ |
| $\mathrm{C}_{s}$ (Off) | 18 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{D}}$ (Off) | 62 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{D}}(\mathrm{On}), \mathrm{C}_{\text {S }}(\mathrm{On})$ | 83 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |


| Parameter | $25^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| POWER REQUIREMENTS | $\begin{aligned} & 45 \\ & 55 \\ & 0.001 \end{aligned}$ |  | 70 | $\mu \mathrm{A}$ typ $\mu \mathrm{A}$ max $\mu A$ typ | $\mathrm{V}_{\mathrm{DD}}=+16.5 \mathrm{~V}, \mathrm{~V}_{\text {SS }}=-16.5 \mathrm{~V}$ |
| ldo |  |  |  |  | Digital inputs $=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |
|  |  |  |  |  |  |
| Iss |  |  |  |  | Digital inputs $=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |
|  |  |  | 1 | $\mu \mathrm{A}$ max |  |
| $\mathrm{V}_{\mathrm{DD}} / \mathrm{V}_{\text {SS }}$ |  |  | $\pm 9 / \pm 22$ | $V$ min $/ V$ max | $\mathrm{GND}=0 \mathrm{~V}$ |

${ }^{1}$ Guaranteed by design; not subject to production test.

## $\pm 20$ V DUAL SUPPLY

$\mathrm{V}_{\mathrm{DD}}=+20 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{SS}}=-20 \mathrm{~V} \pm 10 \%, G N D=0 \mathrm{~V}$, unless otherwise noted.
Table 2.


| Parameter | $25^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Insertion Loss | -0.6 |  |  | dB typ | $\begin{aligned} & \mathrm{RL}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ; \\ & \text { see Figure } 30 \end{aligned}$ |
| $\mathrm{C}_{s}$ (Off) | 18 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{D}}$ (Off) | 63 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{d}}(\mathrm{On}), \mathrm{Cs}_{\text {( }}(\mathrm{On})$ | 82 |  |  | pF typ | $\mathrm{V}_{\mathrm{S}}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| POWER REQUIREMENTS | $\begin{aligned} & 50 \\ & 70 \\ & 0.001 \end{aligned}$ |  | 110 | $\mu \mathrm{A}$ typ <br> $\mu \mathrm{A}$ max <br> $\mu \mathrm{A}$ typ | $\mathrm{V}_{\mathrm{DD}}=+22 \mathrm{~V}, \mathrm{~V}_{S S}=-22 \mathrm{~V}$ |
| ldD |  |  | Digital inputs $=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |  |
|  |  |  |  |  |
| Iss |  |  | Digital inputs $=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |  |
|  |  |  | 1 | $\mu \mathrm{A}$ max |  |
| $V_{\text {DD }} / V_{S S}$ |  |  | $\pm 9 / \pm 22$ | $V$ min/V max | $\mathrm{GND}=0 \mathrm{~V}$ |

${ }^{1}$ Guaranteed by design; not subject to production test.

## 12 V SINGLE SUPPLY

$\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{SS}}=0 \mathrm{~V}, \mathrm{GND}=0 \mathrm{~V}$, unless otherwise noted.
Table 3.


| Parameter | $25^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Off Isolation | -78 |  |  | dB typ | $\mathrm{RL}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ;$ see Figure 27 |
| Channel-to-Channel Crosstalk | -58 |  |  | dB typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ; \\ & \text { see Figure } 26 \end{aligned}$ |
| Total Harmonic Distortion + Noise | 0.075 |  |  | \% typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, 6 \mathrm{~V} \mathrm{p}-\mathrm{p}, \mathrm{f}=20 \mathrm{~Hz} \text { to } 20 \mathrm{kHz} \text {; } \\ & \text { see Figure } 29 \end{aligned}$ |
| -3 dB Bandwidth | 106 |  |  | MHz typ | $\mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$; see Figure 30 |
| Insertion Loss | -1.3 |  |  | dB typ | $\mathrm{RL}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ;$ <br> see Figure 30 |
| $\mathrm{C}_{s}$ (Off) | 22 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=6 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{D}}$ (Off) | 67 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=6 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{D}}(\mathrm{On}), \mathrm{C}_{\mathrm{s}}(\mathrm{On})$ | 85 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=6 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| POWER REQUIREMENTS |  |  |  |  | $\mathrm{V}_{\mathrm{DD}}=13.2 \mathrm{~V}$ |
| IDD | 40 |  |  | $\mu \mathrm{A}$ typ | Digital inputs $=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |
|  | 50 |  | 65 | $\mu \mathrm{A}$ max |  |
| $V_{D D}$ |  |  | 9/40 | $\checkmark$ min/V max | $\mathrm{GND}=0 \mathrm{~V}, \mathrm{~V}_{\text {ss }}=0 \mathrm{~V}$ |

${ }^{1}$ Guaranteed by design; not subject to production test.

## 36 V SINGLE SUPPLY

$\mathrm{V}_{\mathrm{DD}}=36 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{SS}}=0 \mathrm{~V}, \mathrm{GND}=0 \mathrm{~V}$, unless otherwise noted.
Table 4.

| Parameter | $25^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |
| Analog Signal Range |  |  | 0 V to $\mathrm{V}_{\mathrm{DD}}$ | V |  |
| On Resistance, Ron | 10.6 |  |  | $\Omega$ typ | $\begin{aligned} & \mathrm{V}_{\mathrm{s}}=0 \mathrm{~V} \text { to } 30 \mathrm{~V}, \mathrm{I}_{\mathrm{s}}=-10 \mathrm{~mA} ; \\ & \text { see Figure } 25 \end{aligned}$ |
|  | 12 | 15 | 17 | $\Omega$ max | $\mathrm{V}_{\mathrm{DD}}=32.4 \mathrm{~V}, \mathrm{~V}_{S S}=0 \mathrm{~V}$ |
| On-Resistance Match Between Channels, $\Delta$ Ron | 0.35 |  |  | $\Omega \operatorname{typ}$ | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V} \text { to } 30 \mathrm{~V}, \mathrm{I}_{\mathrm{s}}=-10 \mathrm{~mA}$ |
|  |  |  |  |  |  |
|  | 0.7 | 0.9 | 1.1 | $\Omega$ max <br> $\Omega$ typ <br> $\Omega$ max |  |
| On-Resistance Flatness, Rflat(on) | 2.7 |  |  |  | $\mathrm{V}_{\mathrm{s}}=0 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{I}_{\mathrm{s}}=-10 \mathrm{~mA}$ |
|  | 3.2 | 3.8 | 4.5 |  |  |
| LEAKAGE CURRENTS |  |  |  | nA typ | $V_{D D}=39.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{SS}}=0 \mathrm{~V}$ |
| Source Off Leakage, Is (Off) | $\pm 0.05$ |  |  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{S}}=1 \mathrm{~V} / 30 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=30 \mathrm{~V} / 1 \mathrm{~V} ; \\ & \text { see Figure } 28 \end{aligned}$ |
|  | $\pm 0.25$ | $\pm 0.75$ | $\pm 6$ | $n A \max$ | $\begin{aligned} & \mathrm{V}_{\mathrm{S}}=1 \mathrm{~V} / 30 \mathrm{~V}, \mathrm{~V}_{\mathrm{D}}=30 \mathrm{~V} / 1 \mathrm{~V} ; \\ & \text { see Figure } 28 \end{aligned}$ |
| Drain Off Leakage, $\mathrm{I}_{\mathrm{D}}$ (Off) | $\pm 0.1$ |  |  | nA typ |  |
| Channel On Leakage, Id (On), Is (On) | $\pm 0.4$ | $\pm 2$ | $\pm 12$ | nA max <br> nA typ |  |
|  | $\pm 0.1$ |  |  |  | $\mathrm{V}_{\mathrm{S}}=\mathrm{V}_{\mathrm{D}}=1 \mathrm{~V} / 30 \mathrm{~V}$; see Figure 24 |
|  | $\pm 0.4$ | $\pm 2$ | $\pm 12$ | nA max |  |
| DIGITAL INPUTS |  |  |  |  |  |
| Input High Voltage, $\mathrm{V}_{\text {INH }}$ |  |  | 2.0 | $V$ min |  |
| Input Low Voltage, $\mathrm{V}_{\text {INL }}$ |  |  | 0.8 | $V$ max |  |
| Input Current, $\mathrm{I}_{\text {INL }}$ or $\mathrm{l}_{\mathrm{INH}}$ | 0.002 |  |  | $\mu \mathrm{A}$ typ | $\mathrm{V}_{\mathbb{I N}}=\mathrm{V}_{G N D}$ or $\mathrm{V}_{\mathrm{DD}}$ |
|  |  |  | $\pm 0.1$ | $\mu \mathrm{A}$ max |  |
| Digital Input Capacitance, CIN | 5 |  |  | pF typ |  |


| Parameter | $25^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | Unit | Test Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DYNAMIC CHARACTERISTICS ${ }^{1}$ |  |  |  |  |  |
| Transition Time, ttransition | 174 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  | 246 | 270 | 303 | ns max | $V_{s}=18 \mathrm{~V}$; see Figure 31 |
| ton | 180 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  | 247 | 270 | 301 | ns max | $\mathrm{V}_{\mathrm{s}}=18 \mathrm{~V}$; see Figure 33 |
| toff | 127 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, C_{L}=35 \mathrm{pF}$ |
|  | 179 | 193 | 215 | ns max | $\mathrm{V}_{5}=18 \mathrm{~V}$; see Figure 33 |
| Break-Before-Make Time Delay, to | 55 |  |  | ns typ | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ |
|  |  |  | 18 | ns min | $\mathrm{V}_{51}=\mathrm{V}_{52}=18 \mathrm{~V}$; see Figure 32 |
| Charge Injection, Qin | 250 |  |  | pC typ | $\mathrm{V}_{\mathrm{s}}=18 \mathrm{~V}, \mathrm{R}_{\mathrm{s}}=0 \Omega, \mathrm{C}_{\mathrm{L}}=1 \mathrm{nF} ;$ <br> see Figure 34 |
| Off Isolation | -78 |  |  | dB typ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} \text {; } \\ & \text { see Figure } 27 \end{aligned}$ |
| Channel-to-Channel Crosstalk | -58 |  |  | dB typ | $\begin{aligned} & \mathrm{RL}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} \text {; } \\ & \text { see Figure } 26 \end{aligned}$ |
| Total Harmonic Distortion + Noise | 0.03 |  |  | \% typ | $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, 18 \mathrm{~V} \mathrm{p}-\mathrm{p}, \mathrm{f}=20 \mathrm{~Hz} \text { to }$ <br> 20 kHz ; see Figure 29 |
| -3 dB Bandwidth | 98 |  |  | MHz typ | $\mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$; see Figure 30 |
| Insertion Loss | -0.8 |  |  | dB typ | $\mathrm{R}_{\mathrm{L}}=50 \Omega, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}, \mathrm{f}=1 \mathrm{MHz} ;$ see Figure 30 |
| $\mathrm{C}_{s}$ (Off) | 19 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=18 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $C_{\text {d }}$ (Off) | 40 |  |  | pF typ | $\mathrm{V}_{\mathrm{s}}=18 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{C}_{\mathrm{D}}(\mathrm{On}), \mathrm{C}_{\text {S }}(\mathrm{On})$ | 78 |  |  | pF typ | $\mathrm{V}_{\mathrm{S}}=18 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| POWER REQUIREMENTS |  |  |  |  | $\mathrm{V}_{\mathrm{DD}}=39.6 \mathrm{~V}$ |
| IDD | 80 |  |  | $\mu \mathrm{A}$ typ | Digital inputs $=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{DD}}$ |
|  |  |  | 130 | $\mu \mathrm{A}$ max |  |
| $V_{D D}$ |  |  | 9/40 | $V$ min/V max | $\mathrm{GND}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{ss}}=0 \mathrm{~V}$ |

${ }^{1}$ Guaranteed by design; not subject to production test.

## CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

| Parameter | $25^{\circ} \mathrm{C}$ | $85^{\circ} \mathrm{C}$ | $125^{\circ} \mathrm{C}$ | Unit |
| :---: | :---: | :---: | :---: | :---: |
| CONTINUOUS CURRENT, Sx OR Dx |  |  |  |  |
| $\mathrm{V}_{\mathrm{DD}}=+15 \mathrm{~V}, \mathrm{~V}_{\text {SS }}=-15 \mathrm{~V}$ |  |  |  |  |
| TSSOP ( $\theta_{\text {JA }}=112.6^{\circ} \mathrm{C} / \mathrm{W}$ ) | 122 | 77 | 44 | mA maximum |
| LFCSP ( $\theta_{\text {JA }}=30.4^{\circ} \mathrm{C} / \mathrm{W}$ ) | 217 | 116 | 53 | mA maximum |
| $\mathrm{V}_{\mathrm{DD}}=+20 \mathrm{~V}, \mathrm{~V}_{\text {SS }}=-20 \mathrm{~V}$ |  |  |  |  |
| TSSOP ( $\theta_{\mathrm{JA}}=112.6^{\circ} \mathrm{C} / \mathrm{W}$ ) | 130 | 80 | 45 | mA maximum |
| LFCSP ( $\theta_{\text {JA }}=30.4^{\circ} \mathrm{C} / \mathrm{W}$ ) | 229 | 121 | 54 | mA maximum |
| $\mathrm{V}_{\mathrm{DD}}=12 \mathrm{~V}, \mathrm{~V}_{S S}=0 \mathrm{~V}$ |  |  |  |  |
| TSSOP ( $\theta_{\mathrm{JA}}=112.6^{\circ} \mathrm{C} / \mathrm{W}$ ) | 84 | 56 | 36 | mA maximum |
| $\operatorname{LFCSP}\left(\theta_{\mathrm{JA}}=30.4^{\circ} \mathrm{C} / \mathrm{W}\right)$ | 150 | 90 | 48 | mA maximum |
| $V_{D D}=36 \mathrm{~V}, \mathrm{~V}_{S S}=0 \mathrm{~V}$ |  |  |  |  |
| $\operatorname{TSSOP}\left(\theta_{\mathrm{JA}}=112.6^{\circ} \mathrm{C} / \mathrm{W}\right)$ | 110 | 70 | 42 | mA maximum |
| LFCSP ( $\theta_{\mathrm{JA}}=30.4^{\circ} \mathrm{C} / \mathrm{W}$ ) | 196 | 109 | 52 | mA maximum |

## ABSOLUTE MAXIMUM RATINGS

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.
Table 6.

| Parameter | Rating |
| :---: | :---: |
| $V_{\text {dD }}$ to V ${ }_{\text {SS }}$ | 48 V |
| VDD to GND | -0.3 V to +48 V |
| $V_{\text {ss }}$ to GND | +0.3 V to -48 V |
| Analog Inputs ${ }^{1}$ | $\mathrm{V}_{S S}-0.3 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{DD}}+0.3 \mathrm{~V}$ or 30 mA , whichever occurs first |
| Digital Inputs ${ }^{1}$ | $\mathrm{V}_{\mathrm{SS}}-0.3 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{DD}}+0.3 \mathrm{~V}$ or 30 mA , whichever occurs first |
| Peak Current, Sx or Dx Pins | 375 mA (pulsed at 1 ms , 10\% duty cycle maximum) |
| Continuous Current, Sx or Dx ${ }^{2}$ | Data + 15\% |
| Temperature Range |  |
| Operating | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Junction Temperature | $150^{\circ} \mathrm{C}$ |
| Thermal Impedance, $\theta_{\mathrm{JA}}$ |  |
| 16-Lead TSSOP (4-Layer Board) | $112^{\circ} \mathrm{C} / \mathrm{W}$ |
| 16-Lead LFCSP | $30.4{ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Reflow Soldering Peak Temperature, Pb Free | $260(+0 /-5)^{\circ} \mathrm{C}$ |

[^0]Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.
Only one absolute maximum rating can be applied at any one time.

## ESD CAUTION

|  | ESD (electrostatic discharge) sensitive device. <br> Charged devices and circuit boards can discharge <br> without detection. Although this product features <br> patented or proprietary protection circuitry, damage <br> may occur on devices subjected to high energy ESD. <br> Therefore, proper ESD precautions should be taken to <br> avoid performance degradation or loss of functionality. |
| :--- | :--- |

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 3. TSSOP Pin Configuration


Figure 4. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. |  | Mnemonic | Function |
| :---: | :---: | :---: | :---: |
| TSSOP | LFCSP |  |  |
| 1 | 15 | IN1 | Logic Control Input 1. |
| 2 | 16 | S1A | Source Terminal 1A. This pin can be an input or output. |
| 3 | 1 | D1 | Drain Terminal 1. This pin can be an input or output. |
| 4 | 2 | S1B | Source Terminal 1B. This pin can be an input or output. |
| 5 | 3 | $\mathrm{V}_{\text {SS }}$ | Most Negative Power Supply Potential. |
| 6 | 4 | GND | Ground (0V) Reference. |
| 7,8,14 to 16 | 5, 7, 13, 14 | NC | No Connect. |
| 9 | 6 | IN2 | Logic Control Input 2. |
| 10 | 8 | S2A | Source Terminal 2A. This pin can be an input or output. |
| 11 | 9 | D2 | Drain Terminal 2. This pin can be an input or output. |
| 12 | 10 | S2B | Source Terminal 2B. This pin can be an input or output. |
| 13 | 11 | $V_{\text {DD }}$ | Most Positive Power Supply Potential. |
| Not applicable | 12 | EN | Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, INx logic inputs determine the on switches. |
| Not applicable |  | EPAD | The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, $\mathrm{V}_{\text {ss }}$. |

## TRUTH TABLE FOR SWITCHES

Table 8. ADG5436 TSSOP Truth Table

| $\mathbf{I N x}$ | SxA | SxB |
| :--- | :--- | :--- |
| 0 | Off | On |
| 1 | On | Off |

Table 9. ADG5436 LFCSP Truth Table

| EN | INx | SxA | SxB |
| :--- | :--- | :--- | :--- |
| 0 | X $^{1}$ | Off | Off |
| 1 | 0 | Off | On |
| 1 | 1 | On | Off |
| X is don't care. |  |  |  |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 5. On Resistance vs. $V_{s,} V_{D}$ (Dual Supply)


Figure 6. On Resistance vs. $V_{s,}, V_{D}$ (Dual Supply) Included


Figure 7. On Resistance vs. $V_{S}, V_{D}$ (Single Supply)


Figure 8. On Resistance vs. $V_{S}, V_{D}$ (Single Supply)


Figure 9. On Resistance vs. $V_{D}$ or $V_{S}$ for Different Temperatures, $\pm 15$ V Dual Supply


Figure 10. On Resistance vs. $V_{D}$ or $V_{s}$ for Different Temperatures, $\pm 20$ V Dual Supply


Figure 11. On Resistance vs. $V_{D}$ or $V_{s}$ for Different Temperatures, 12 V Single Supply


Figure 12. On Resistance vs. $V_{S}\left(V_{D}\right)$ for Different Temperatures, 36 V Single Supply


Figure 13. Leakage Currents vs. Temperature, $\pm 15$ V Dual Supply


Figure 14. Leakage Currents vs. Temperature, $\pm 20$ V Single Supply


Figure 15. Leakage Currents vs. Temperature, 12 V Single Supply


Figure 16. Leakage Currents vs. Temperature, 36 V Single Supply


Figure 17. Off Isolation vs. Frequency


Figure 18. Crosstalk vs. Frequency


Figure 19. Charge Injection vs. Source Voltage


Figure 20. ACPSRR vs. Frequency


Figure 21. THD $+N$ vs. Frequency


Figure 22. Bandwidth


Figure 23. $t_{\text {TRANSITION }}$ Time vs. Temperature

## TEST CIRCUITS



Figure 24. On Leakage


Figure 25. On Resistance


CHANNEL-TO-CHANNEL CROSSTALK $=20 \log \frac{V_{\text {OUT }}}{v_{\text {S }}}$
Figure 26. Channel-to-Channel Crosstalk

Figure 27. Off Isolation



Figure 28. Off Leakage


Figure 29. THD + Noise


Figure 30. Bandwidth


Figure 31. Switching Times


Figure 32. Break-Before-Make Time Delay $t_{D}$


Figure 33. Enable Delay, $t_{\text {ON }}(E N)$, toff (EN)


Figure 34. Charge Injection

## ADG5436

## TERMINOLOGY

$\mathrm{I}_{\mathrm{DD}}$
$I_{D D}$ represents the positive supply current.
Iss
Iss $_{\text {s }}$ represents the negative supply current.
$V_{D}, V_{s}$
$\mathrm{V}_{\mathrm{D}}$ and $\mathrm{V}_{\mathrm{S}}$ represent the analog voltage on Terminal D and Terminal S, respectively.
Ron
Ron represents the ohmic resistance between Terminal D and Terminal S.

## $\Delta$ Ron

$\Delta$ Ron represents the difference between the Ron of any two channels.
$\mathbf{R}_{\text {flat (ON) }}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $\mathrm{R}_{\text {fLat (ON) }}$.

Is (Off)
Is (Off) is the source leakage current with the switch off.
$\mathrm{I}_{\mathrm{D}}$ (Off)
$\mathrm{I}_{\mathrm{D}}$ (Off) is the drain leakage current with the switch off.
$\mathrm{I}_{\mathrm{D}}(\mathrm{On}), \mathrm{I}_{\mathrm{s}}(\mathrm{On})$
$\mathrm{I}_{\mathrm{D}}(\mathrm{On})$ and $\mathrm{I}_{\mathrm{S}}(\mathrm{On})$ represent the channel leakage currents with the switch on.
$V_{\text {INL }}$
$\mathrm{V}_{\text {INL }}$ is the maximum input voltage for Logic 0 .
$V_{\text {INH }}$
$\mathrm{V}_{\text {INH }}$ is the minimum input voltage for Logic 1.
$\mathrm{I}_{\mathrm{INL}}, \mathrm{I}_{\mathrm{INH}}$
$\mathrm{I}_{\text {INL }}$ and $\mathrm{I}_{\text {INH }}$ represent the low and high input currents of the digital inputs.
$\mathrm{C}_{\mathrm{D}}$ (Off)
$C_{D}$ (Off) represents the off switch drain capacitance, which is measured with reference to ground.
$\mathrm{C}_{\mathrm{s}}$ (Off)
$\mathrm{C}_{S}$ (Off) represents the off switch source capacitance, which is measured with reference to ground.
$\mathrm{C}_{\mathrm{D}}$ (On), $\mathrm{C}_{\mathrm{s}}$ (On)
$C_{D}(\mathrm{On})$ and $\mathrm{C}_{s}(\mathrm{On})$ represent on switch capacitances, which are measured with reference to ground.

## $\mathrm{C}_{\text {IN }}$

$\mathrm{C}_{\text {IN }}$ is the digital input capacitance.
ton
$t_{\text {ON }}$ represents the delay between applying the digital control input and the output switching on.
$\boldsymbol{t}_{\text {OfF }}$
toff represents the delay between applying the digital control input and the output switching off.
to
$t_{D}$ represents the off time measured between the $80 \%$ point of both switches when switching from one address state to another.

## Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

## Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

## Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

## Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB .

## On Response

On response is the frequency response of the on switch.

## Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.
Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

## AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

ADG5436

## TRENCH ISOLATION

In the ADG5436, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.
In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.


Figure 35. Trench Isolation

## APPLICATIONS INFORMATION

The Analog Devices, Inc., family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persist until the power supply is turned off. The ADG5436 high voltage switches allow single-
supply operation from +9 V to +40 V and dual-supply operation from $\pm 9 \mathrm{~V}$ to $\pm 22 \mathrm{~V}$. The ADG5436 (as well as other select devices within this family) achieves an 8 kV human body model ESD rating, which provides a robust solution eliminating the need for separate protect circuitry designs in some applications.

## OUTLINE DIMENSIONS



Figure 36. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters


## COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP]
$4 \mathrm{~mm} \times 4 \mathrm{~mm}$ Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

| Model $^{1}$ | Temperature Range | Package Description | Package Option |
| :--- | :--- | :--- | :--- |
| ADG5436BRUZ | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 -Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG5436BRUZ-REEL7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 -Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG5436BCPZ-REEL7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16 -Lead Lead Frame Chip Scale Package [LFCSP] | CP-16-17 |

${ }^{1} \mathrm{Z}=$ RoHS Compliant Part.


[^0]:    ${ }^{1}$ Overvoltages at the $I N x, S x$, and Dx pins are clamped by internal diodes.
    Current should be limited to the maximum ratings given.
    ${ }^{2}$ See Table 5.

