## Product Overview

The Qorvo QPD1025 is a $1800 \mathrm{~W}\left(\mathrm{P}_{3 \mathrm{~dB}}\right)$ discrete GaN on SiC HEMT which operates from 0.96 to 1.215 GHz . Input prematch within the package results in ease of external board match and saves board space. The device is in an industry standard air cavity package and is ideally suited for IFF, avionics and test instrumentation. The device can support both CW and pulsed operations.

RoHS compliant
Evaluation boards are available upon request.

## Functional Block Diagram




4-lead NI-1230 Package (Earless)

## Key Features

- Frequency: 0.96 to 1.215 GHz
- Output Power (P3dB) ${ }^{1}$ : 1862 W
- Linear Gain¹: 22.5 dB
- Typical PAE3dB ${ }^{1}: 77.2 \%$
- Operating Voltage: 65 V
- CW and Pulse capable

Note 1: @ 1.0 GHz Load Pull

## Applications

- IFF Transponders
- DME radar
- Avionics


## Ordering info

| Part No. | Description |
| :--- | :--- |
| QPD1025 | $0.96-1.215 \mathrm{GHz}$ Transistor (18 pcs in <br> tray) |
| QPD1025EVB1 | $1.0-1.1 \mathrm{GHz}$ EvaluationBoard |
| QPD1025EVB2 | $0.96-1.215 \mathrm{GHz}$ Evaluation Board |

Absolute Maximum Ratings ${ }^{1,2,3}$

| Parameter | Rating | Units |
| :--- | :---: | :---: |
| Breakdown Voltage,BVDG | 225 | V |
| Gate Voltage Range, VG | -7 to +2 | V |
| Drain Current, IDmAx | 142 | A |
| Gate Current Range, IG | See pg. 12 | mA |
| Power Dissipation, Pulsed, <br> PoIss $^{2}$ | 1209 | W |
| RF Input Power, Pulsed, Pin |  |  |
| Mounting Temperature <br> $(30$ Seconds) | 46.2 | dBm |
| Storage Temperature | 320 | ${ }^{\circ} \mathrm{C}$ |

## Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage
2. Pulsed, 1000 us PW, $20 \%$ DC, Package base at $85^{\circ} \mathrm{C}$
3. Pulsed, 100 us PW, $10 \% \mathrm{DC}, \mathrm{T}=25^{\circ} \mathrm{C}$

Recommended Operating Conditions ${ }^{1,2,3,4}$

| Parameter | Min | Typ | Max | Units |
| :--- | :---: | :---: | :---: | :---: |
| Operating Temp. Range | -40 | +25 | +85 | ${ }^{\circ} \mathrm{C}$ |
| Drain Voltage Range, VD | - | +65 | +70 | V |
| Drain Bias Current, IDQ |  | 1.5 |  | A |
| Drain Current, ID ${ }^{4}$ | - | 28 | - | A |
| Gate Voltage, VG ${ }^{3}$ | - | -2.8 | - | V |
| Power Dissipation (PD) ${ }^{2,4}$ | - | - | 685 | W |
| Power Dissipation (PD), CW ${ }^{2}$ | - | - | 496 | W |

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions
2. Package base at $85^{\circ} \mathrm{C}$
3. To be adjusted to desired $\mathrm{I}_{\mathrm{DQ}}$
4. Pulsed, 1000 us PW, $20 \%$ DC

Measured Load Pull Performance-65V Power Tuned ${ }^{1,2}$

| Parameter | Typical Values |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Frequency, F | 0.915 | 1.0 | 1.1 | 1.2 | GHz |
| Output Power at 3dB compression, P3dB | 59.9 | 59.7 | 59.7 | 59.8 | dBm |
| Power Added Efficiency at 3dB compression, PAE 3 dB | 63.2 | 62.8 | 65.7 | 61.9 | $\%$ |
| Gain at 3dB compression, G3dB | 17.9 | 17.5 | 17.3 | 17.2 | dB |

Notes:

1. Test conditions unless otherwise noted: $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \operatorname{lDQ}=750 \mathrm{~mA}$ (half device)
2. Pulsed, 100 us Pulse Width, $10 \%$ Duty Cycle.

## Measured Load Pull Performance - 65V Efficiency Tuned ${ }^{1,2}$

| Parameter | Typical Values |  |  |  |  | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency, F | 0.915 | 1.0 | 1.1 | 1.2 | GHz |  |
| Output Power at 3dB compression, P3dB | 57.5 | 57.7 | 58.5 | 58.3 | dBm |  |
| Power Added Efficiency at 3dB compression, PAE 3 dB | 77.6 | 77.2 | 77.0 | 74.6 | $\%$ |  |
| Gain at 3dB compression, G3dB | 19.7 | 19.5 | 18.7 | 19.0 | dB |  |

## Notes:

1. Test conditions unless otherwise noted: $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}$ (half device)
2. Pulsed, 100 us Pulse Width, $10 \%$ Duty Cycle.

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## Measured Load Pull Performance - 50V Power Tuned ${ }^{1,2}$

| Parameter | Typical Values |  |  |  |  | Units |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency, F | 0.915 | 1.0 | 1.1 | 1.2 | GHz |  |
| Output Power at 3dB compression, P3dB | 58.9 | 58.6 | 58.5 | 58.6 | dBm |  |
| Power Added Efficiency at 3dB compression, PAE 3 dB | 66.8 | 60.1 | 66.1 | 62.6 | $\%$ |  |
| Gain at 3dB compression, G3dB | 17.6 | 17 | 17 | 16.8 | dB |  |

## Notes

1. Test conditions unless otherwise noted: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{D}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}$ (half device)
2. Pulsed, 100 us Pulse Width, $10 \%$ Duty Cycle.

## Measured Load Pull Performance - 50V Efficiency Tuned ${ }^{1,2}$

| Parameter | Typical Values |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency, F | 0.915 | 1.0 | 1.1 | 1.2 | GHz |  |
| Output Power at 3dB compression, P3dB | 55.2 | 55.6 | 56.5 | 56.8 | dBm |  |
| Power Added Efficiency at 3dB compression, PAE 3 dB | 78.2 | 74.7 | 76.6 | 71.8 | $\%$ |  |
| Gain at 3dB compression, G3dB | 19.2 | 19 | 18.6 | 18.2 | dB |  |

## Notes

1. Test conditions unless otherwise noted: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{D}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}$ (half device)
2. Pulsed, 100 us Pulse Width, $10 \%$ Duty Cycle.

## RF Characterization - 1.0-1.1 GHz EVB1 Performance at $1.05 \mathrm{GHz}{ }^{1}$

| Parameter | Min | Typ | Max | Units |
| :--- | :---: | :---: | :---: | :---: |
| Linear Gain, GLIN | - | 21.2 | - | dB |
| Output Power at 3dB compression point, P3dB | - | 1461 | - | W |
| Drain Efficiency at 3dB compression point, DEFF3dB | - | 73.2 | - | $\%$ |
| Gain at 3dB compression point, G3dB | - | 18.2 | - | dB |
| Gate Leakage VD $=+10 \mathrm{~V}, \mathrm{VG}=-3.3 \mathrm{~V}$ | $-25^{2}$ | - | - | mA |

## Notes:

1. $\mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=1.5 \mathrm{~A}$ (combined), $\mathrm{Temp}=+25^{\circ} \mathrm{C}$, Pulse Width $=100$ us, Duty Cycle $=10 \%$
2. Gate leakage per path

## RF Characterization - 0.96-1.215 GHz EVB2 Performance ${ }^{1}$

| Parameter | Typ 0.96 GHz | Typ 1.08 GHz | Typ 1.2GHz | Units |
| :--- | :---: | :---: | :---: | :---: |
| Linear Gain, GLIN | 20 | 19.5 | 19.6 | dB |
| Output Power at 2dB compression point, P2dB | 1800 | 1678 | 1570 | W |
| Drain Efficiency at 2dB compression point, DEFF2dB | 64 | 68 | 66 | $\%$ |
| Gain at 3dB compression point, G2dB | 18 | 17.5 | 17.6 | dB |
| Gate Leakage VD $=+10 \mathrm{~V}, \mathrm{VG}=-3.3 \mathrm{~V}$ | $-25^{2}$ | - | - | mA |

Notes:

1. $\mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}$, $\mathrm{I}_{\mathrm{DQ}}=1.5 \mathrm{~A}$ (combined), Temp $=+25^{\circ} \mathrm{C}$, Pulse Width $=100$ us, Duty Cycle $=10 \%$
2. Gate leackage per path

## RF Characterization - Mismatch Ruggedness at $1.0 \mathrm{GHz}^{1,2,3}$

| Symbol | Parameter | dB Compression | Typical |
| :--- | :--- | :---: | :---: |
| VSWR | Impedance Mismatch Ruggedness | 3 | $10: 1$ |

## Notes:

1. Test conditions unless otherwise noted: $T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=1.5 \mathrm{~A}$ (combined)
2. Input drive power is determined at pulsed 3 dB compression under matched condition at EVB output connector
3. Pulse: 100 us, $10 \%$ Duty cycle

Maximum Gate Current vs. IR Surface Temperature


QPD1025
1800 W, 65 V, 0.96 - 1.215GHz, GaN RF Input-Matched Transistor

## Thermal and Reliability Information - Pulsed ${ }^{1}$



| Parameter | Conditions | Values | Units |
| :--- | :--- | :--- | :---: |
| Thermal Resistance, IR ${ }^{1}\left(\theta_{\mathrm{Jc}}\right)$ | $85^{\circ} \mathrm{C}$ Case backside Temperature |  |  |
| Pdiss $=518 \mathrm{~W}$, Pulse: 100 us PW, $10 \% \mathrm{DC}$ | 0.10 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |
| Peak IR Surface Temperature $\left(\mathrm{T}_{\mathrm{ch}}\right)$ | Pa | 131 | ${ }^{\circ} \mathrm{C}$ |

Notes:

1. Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Measured Load-Pull Smith Charts at 65V 1, 2,3

Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 18 for load pull reference planes where the performance was measured.

### 0.915GHz, Load-pull



3dB Compression Referenced to Peak Gain

## Measured Load-Pull Smith Charts at 65V ${ }^{1,2,3}$

Notes:
5. Test Conditions: $V_{D}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
6. The performance shown below is for only half of the device out of the two independent amplification paths.
7. See page 18 for load pull reference planes where the perform ance was measured.

### 1.0GHz, Load-pull



3dB Compression Referenced to Peak Gain

## Measured Load-Pull Smith Charts at 65V 1, 2, 3

Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two in dependent amplification paths.
3. See page 18 for load pull reference planes where the performance was measured.

### 1.1GHz, Load-pull



3dB Compression Referenced to Peak Gain

## Measured Load-Pull Smith Charts at 65V ${ }^{1,2,3}$

Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 18 for load pull reference planes where the performance was measured.

### 1.2GHz, Load-pull



[^0]
## Typical Measured Performance - Load-Pull Drive-up at 65V 1, 2,3

## Notes:

1. Test Conditions: $V_{D}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independentamplification paths.
3. See page 18 for load pull reference planes where the performance was measured.


Gain and Drain Eff. vs. Output Power


Gain and Drain Eff. vs. Output Power


Gain and Drain Eff. vs. Output Power
1.2 GHz - Power Tuned


Gain and DRain Eff. vs. Output Power


Gain and Drain Eff. vs. Output Power


Gain and Drain Eff. vs. Output Power 1.1 GHz - Efficiency Tuned


Gain and Drain Eff. vs. Output Power 1.2 GHz - Efficiency Tuned


## Measured Load-Pull Smith Charts at 50V 1, 2, 3

Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 18 for load pull reference planes where the perform ance was measured.

### 0.915GHz, Load-pull



3dB Compression Referenced to Peak Gain

## Measured Load-Pull Smith Charts at 50V ${ }^{1,2,3}$

Notes:
5. Test Conditions: $\mathrm{V}_{\mathrm{D}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
6. The performance shown below is for only half of the device out of the two independent amplification paths.
7. See page 18 for load pull reference planes where the performance was measured.


3dB Compression Referenced to Peak Gain

## Measured Load-Pull Smith Charts at 50V 1, 2,3

Notes:

1. Test Conditions: $V_{D}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 18 for load pull reference planes where the performance was measured.

### 1.1GHz, Load-pull



3dB Compression Referenced to Peak Gain

## Measured Load-Pull Smith Charts at 50V ${ }^{1,2,3}$

Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 18 for load pull reference planes where the perform ance was measured.

### 1.2GHz, Load-pull



3dB Compression Referenced to Peak Gain

## Typical Measured Performance - Load-Pull Drive-up at 50V 1, 2,3

Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=50 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=750 \mathrm{~mA}, 100$ us Pulse Width, $10 \%$ Duty Cycle, Temp $=25^{\circ} \mathrm{C}$.
2. The performance shown below is for only half of the device out of the two independentamplification paths.
3. See page 18 for load pull reference planes where the performance was measured.


QPD1025

## Pin Configuration and Description ${ }^{1}$



PIN 1
INDICATOR

Note:
1- The QPD1025 will be marked with the "QPD1025" designator and a lot code marked below the part designator. The "YY" represents the last two digits of the calendar year the part was manufactured, the "WW" is the work week of the assembly lot start, the " $M X X X$ " is the production lot number, and the " $Z Z Z$ " is an auto-generated serial number.

| Pin | Symbol | Description |
| :---: | :---: | :---: |
| 1,2 | RF IN / VG | Gate |
| 3,4 | RF OUT / VD | Drain |
| 5 | Source | Source / Ground / Backside of part |

## Mechanical Drawing ${ }^{1}$



Notes:

1. All dimensions are in inches.
2. Dimension tolerance is $\pm 0.005$ inches, unless noted otherwise.
3. Package base: Ceramic/Metal, Package lid: Ceramic
4. Package exposed metalization is gold plated
5. Part is epoxy sealed.
6. Parts meet industry NI1230 footprint
7. Body dimensions do not include runout which can be up to 0.020 inches per side.

## 1.0-1.1 GHz Application Circuit - Schematic



## Bias-up Procedure

1. Set $\mathrm{V}_{\mathrm{G}}$ to -5 V .
2. Set $I_{D}$ current limit to 4 A .
3. Apply $65 \mathrm{~V}_{\mathrm{D}}$.
4. Slowly adjust $\mathrm{V}_{\mathrm{G}}$ until $\mathrm{I}_{\mathrm{D}}$ is set to 1.5 A.
5. Apply RF.

## Bias-down Procedure

1. Turn off RF signal.
2. Turn off $\mathrm{V}_{\mathrm{D}}$
3. Wait 2 seconds to allow drain capacitor to discharge.
4. Turn off $\mathrm{V}_{\mathrm{G}}$

## 1.0-1.1 GHz Application Circuit EVB1 - Layout ${ }^{1,2}$

Notes:

1. PCB material is RO4350B 0.020" thick, 2 oz. copper each side.
2. The two gates could be tied together or (optionally) adjusted independently.


## 1.0-1.1 GHz Application Circuit - Bill of Material EVB1

| Reference Design | Value | Qty | Manufacturer | Part Number |
| :---: | :---: | :---: | :---: | :---: |
| U1 |  | 1 | QORVO | QPD1025L |
| C1, C5, C8 | 8.2pF | 3 | American Technical Ceramics | 600S8R2BT250XT |
| C11,C12,C13,C14 | 10pF | 4 | American Technical Ceramics | 100B100JW500XT |
| C15,C18 | 5.6pF | 2 | American Technical Ceramics | 100B5R6CT500XT |
| C16,C17,C28,C29 | 6.8pF | 4 | American Technical Ceramics | 800B6R8CT500XT |
| C19,C20 | 56pF | 2 | American Technical Ceramics | 800B560JT500XT |
| C2 | 0.7pF | 1 | American Technical Ceramics | 800B560JT500XT |
| C21,C22,C27 | 6.8pF | 3 | American Technical Ceramics | 100B100JW500XT |
| C24,C25 | 10uF | 2 | TDK Signapore PDE LTD | C5750X7S2A106M230KB |
| C3, 44 | 20pF | 2 | American Technical Ceramics | 600S200FT250XT |
| C30 | 3 pF | 1 | American Technical Ceramics | 800B3ROBT500XT |
| C31,C32 | 680uF | 2 | Vishay Americas Inc | MAL215099708E3 |
|  | 5.6pF | 2 | American Technical Ceramics | 600S5R6BW250XT |
| C9,C10 | 4.7uF | 2 | Murata Electronics | GRM31CR71H475KA12L |
| L1,L2 | 110nH | 2 | Coilcraft, Inc | 0805CS-111XJBC |
| R1 | 47 | 1 | Panasonic Industrial Devices | KTR03EZPF47R0 |
| R2,R3 | 10 | 2 | Vishay Dale Electronics | CRCW060310ROFKEA |
| Connector | N type F/M | 1 | Huber+Suhner, Inc | 23_N-50-0-33/133_NE |

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## Power Driveup Performance over Temperatures of 1.0-1.1 GHz EVB1 ${ }^{1}$

## Notes:

1. Test Conditions: $\mathrm{V}_{\mathrm{D}}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=1.5 \mathrm{~A}, 100$ us Pulse Width, $10 \%$ Duty Cycle.


Gain vs. Frequency vs. Temp

D. Efficiency at P3dB vs. Frequency vs. Temp


## Power Driveup Performance at $25^{\circ} \mathrm{C}$ of 1.0-1.1 GHz EVB1 ${ }^{1}$

Notes:

1. Test Conditions: $V_{D}=65 \mathrm{~V}, \mathrm{I}_{\mathrm{DQ}}=1.5 \mathrm{~A}, 100$ us Pulse Width, $10 \%$ Duty Cycle.


### 0.96 - 1.215 GHz Application Circuit - Schematic



| Bias-up Procedure | Bias-down Procedure |
| :--- | :--- |
| 2. Set $\mathrm{V}_{G}$ to -5 V . | 3. Turn off $R F$ signal. |
| 4. Set $\mathrm{I}_{\mathrm{D}}$ current limit to 4 A. | 4. Turn off $\mathrm{V}_{\mathrm{D}}$ |
| 5. Apply $65 \mathrm{~V} \mathrm{~V}_{\mathrm{D}}$. | 5. Wait 2 seconds to allow drain capacitor to discharge. |
| 6. Slowly adjust $\mathrm{V}_{G}$ until $\mathrm{I}_{\mathrm{D}}$ is set to 1.5 A. | 6. Turn off $\mathrm{V}_{G}$ |
| 7. Apply $R F$. |  |

### 0.96-1.215 GHz Application Circuit EVB2- Layout ${ }^{1,2}$

Notes:

1. PCB material is RO4350B 0.020" thick, 2 oz. copper each side.
2. The two gates could be tied together or (optionally) adjusted independently.

0.96 - 1.215 GHz Application Circuit - Bill of Material

| Reference Designator | Value | Qty | Manufacturer | Part Number |
| :--- | :--- | ---: | :--- | :--- |
| L1,L2 | 110 nH | 2 | Coilcraft, Inc | 0805CS-111XJBC |
| C2 | 0.7 pF | 1 | American Technical Ceramics | 600S0R7FT250XT |
| C3,C4 | 20 pF | 2 | American Technical Ceramics | 600S200T250T |
| C6,C7 | 5.6 pF | 2 | American Technical Ceramics | 600S5R6T250T |
| C21, C22, C27 | 6.8 pF | 3 | American Technical Ceramics | 600S6R8FT250XT |
| C1, C5,C8 | 8.2 pF | 3 | American Technical Ceramics | 600S8R2FT250XT |
| C19,C20 | 12 pF | 2 | American Technical Ceramics | 800B120BC500XT |
| C23 | 1.5 pF | 1 | American Technical Ceramics | 800B1R5BC500XT |
| C30 | 1.8 pF | 1 | American Technical Ceramics | 800B1R8BT500XT |
| C28,C29 | 2.4 pF | 2 | American Technical Ceramics | 800B2R4BC500XT |
| C12,C13,C15,C16,C17,C18 | $5.6 p F$ | 6 | American Technical Ceramics | 800B5R6BC500XT |
| C11,C14 | 8.2 pF | 2 | American Technical Ceramics | 800B8R2BC500XT |
| C24,C25 | 10 uF | 2 | TDK Singapore (Pte) Ltd | C5750X7S2A106M230KB |
| R2,R3 | 10 Ohms | 2 | Vishay Dale Electronics | CRCW060310R0FKEA |
| Connectors | N type | 2 | Huber+Suhner, Inc | CRCW060310R0FKEA |
| R1 | 47 Ohms | 1 | Panasonic Industrial Devices | ERJ-3EKF47R0 |
| C9,C10 | 4.7 uF | 2 | Murata Electronics | GRM31CR71H475KA12L |
| C31, C32 | 680 uF | 2 | Vishay Americas Inc | MAL215099708E3 |

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## Performance at $25^{\circ} \mathrm{C}$ of 0.96 - 1.215 GHz EVB2 ${ }^{1}$

Notes:

1. Test Conditions: VD $=65 \mathrm{~V}, \mathrm{IDQ}=1.5 \mathrm{~A}, 100$ us Pulse Width, $10 \%$ Duty Cycle.


G2dB vs. Frequency @25C


Pdiss vs. Frequency @25C


Frequency (GHz)

P2dB vs. Frequency @25C

D. E. at P2dB vs. Frequency @25C


## Recommended Solder Temperature Profile



## Handling Precautions

| Parameter | Rating | Standard |
| :--- | :--- | :--- |

## Solderability

Compatible with both lead-free ( $260^{\circ} \mathrm{C}$ max. reflow temp.) and tin/lead ( $245^{\circ} \mathrm{C}$ max. reflow temp.) soldering processes.
Solder profiles available upon request.
Contact plating:NiAu.Au thickness is 100micro-inches

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU .

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ( $\mathrm{C}_{15} \mathrm{H}_{12} \mathrm{Br}_{4} \mathrm{O}_{2}$ ) Free
- PFOS Free
- SVHC Free


## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:
$\begin{array}{ll}\text { Web: } & \text { www.qorvo.com } \\ \text { Email: } & \text { Tel: }+1.844 .890 .8163\end{array}$
For technical questions and application information: Email: info-products@qorvo.com

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[^0]:    3dB Compression Referenced to Peak Gain

