Low-Power 12.5-Gbps Dual-Lane 2:1/1:2 Mux/Buffer With Equalization and De-Emphasis

Check for Samples: DS125MB203

FEATURES

- **Comprehensive Family, Proven System Interoperability**
  - **DS125BR111: One-Lane Repeater**
  - **DS125BR210: Two-Channel Repeater**
  - **DS125BR401: Four-Lane Repeater**
  - **DS125BR800: Eight-Channel Repeater**
  - **DS125MB203: Two-Port, 2:1/1:2 Mux**
  - **DS125DF410: Four-Channel Retimer With CDR**
- **Low 65-mW/Channel (Typical) Power Consumption, With Option to Power Down Unused Channels**
- **Transparent Management of Link Training Protocol for PCIe and 10G-KR**
- **Advanced Signal Conditioning Features**
  - **Receive Equalization up to 30dB at 6.25 GHz**
  - **Transmit De-emphasis up to -12dB**
  - **Transmit Output Voltage Control: 700 mV to 1300 mV**
- **Programmable via Pin Selection, EEPROM, or SMBus Interface**
- **Single Supply Voltage: 2.5 V or 3.3 V (selectable)**
- **40°C to 85°C Operating Temperature Range**
- **3-kV HBM ESD Rating**
- **Flow-Thru Pinout in 10mmx5.5mm 54-Pin Leadless QFN Package**

SUPPORTED PROTOCOLS

- **SAS/SATA (up to 6 Gbps), Fibre Channel (up to 10GFC)**
- **PCIe Gen-3/2/1, 10G-KR, 10GbE, XAUI, RXAUI**
- **sRIO, Infiniband, Interlaken, CPRI, OBSAI**
- **Other proprietary interface up to 12.5 Gbps**

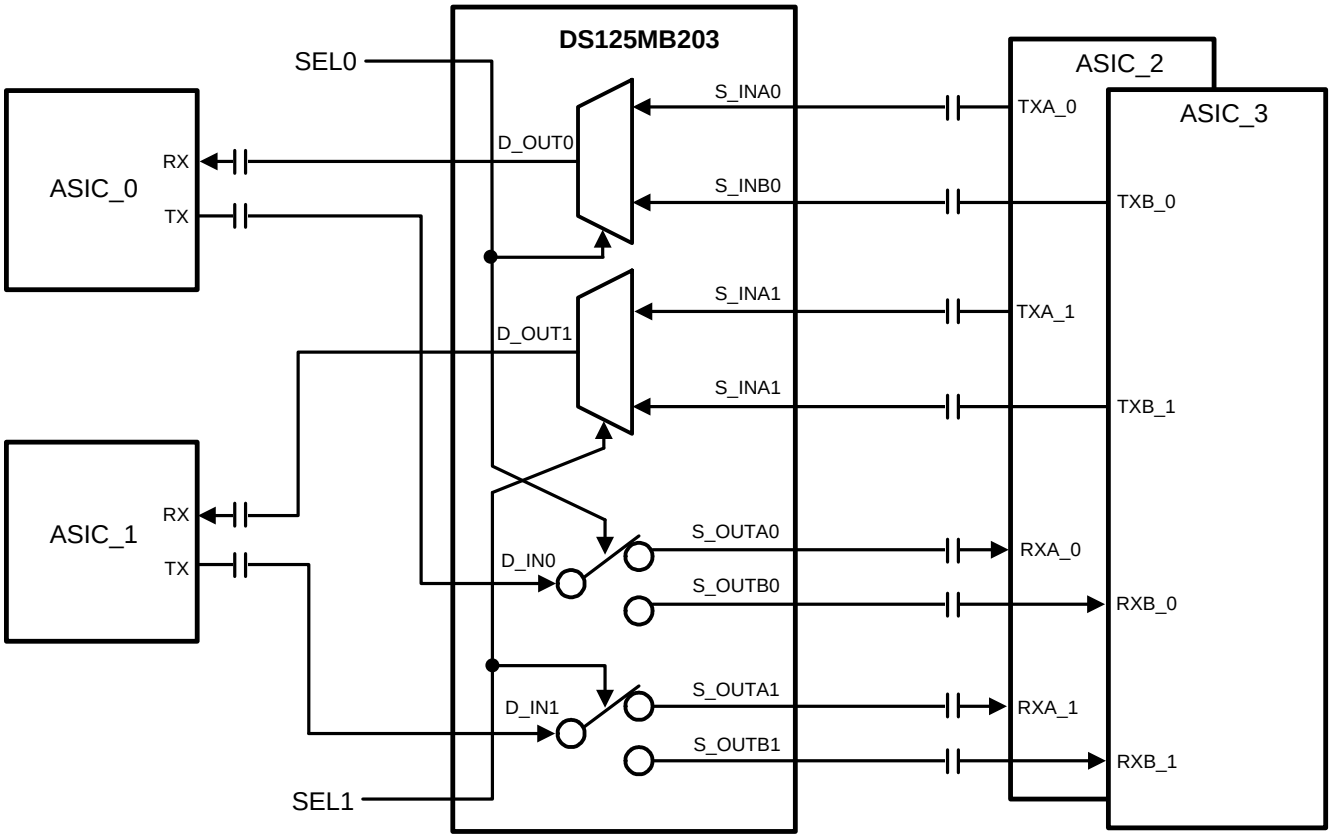
DESCRIPTION

The DS125MB203 is an extremely low-power high-performance dual-port 2:1 mux and 1:2 switch/fanout designed to support high-availability systems using PCIe Gen-3/2/1, 10G-KR, and other high-speed interface serial protocols up to 12.5 Gbps. The integrated signal conditioning function eliminates the need for external devices, reducing BOM cost and board space. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +30 dB at 6.25 GHz (12.5 Gbps) and is capable of opening an input eye that is completely closed due to inter symbol interference (ISI) induced by interconnect medium such as 30in+ backplane traces or 8m+ copper cables. The transmitter provides a de-emphasis boost of up to -12 dB and output voltage amplitude control from 700 mV to 1300 mV.

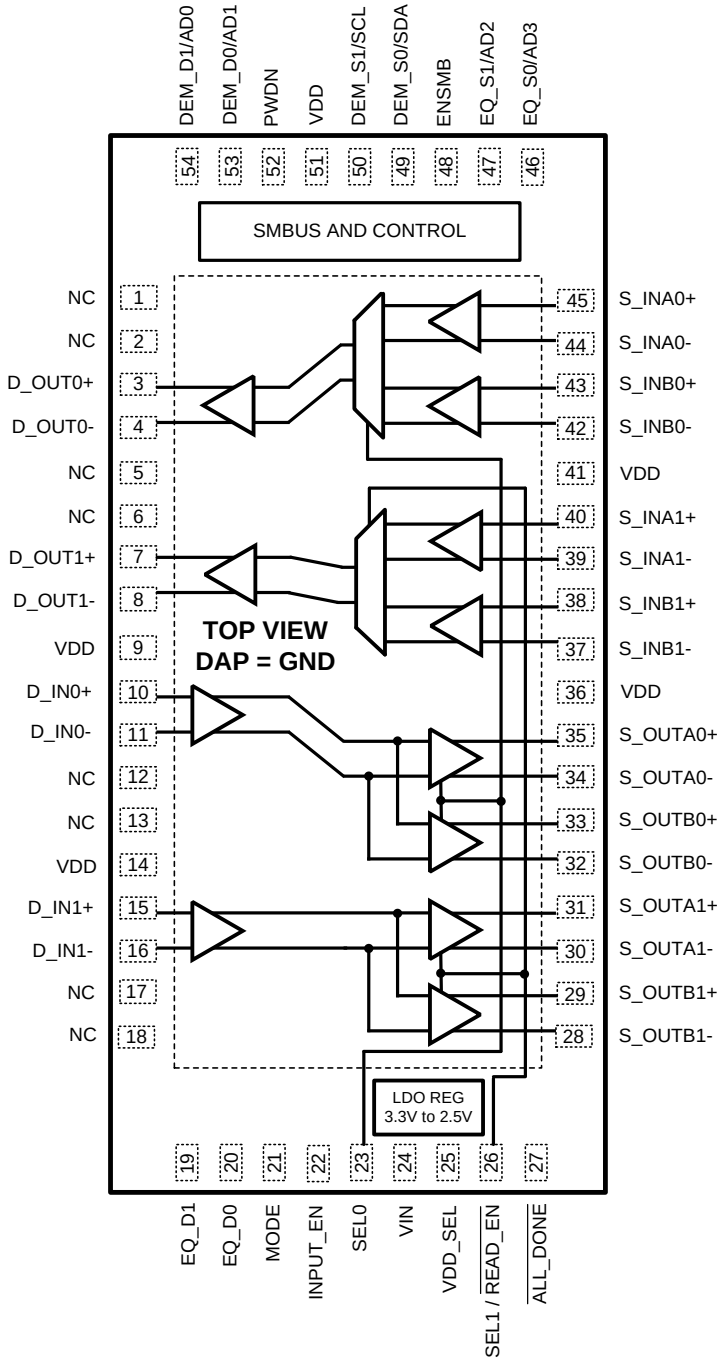
When operating in 10G-KR and PCIe Gen-3 mode, the DS125MB203 transparently allows the host controller and the end point to optimize the full link and negotiate transmit equalizer coefficients. This seamless management of the link training protocol ensures system level interoperability with minimum latency. With a low power consumption of 390 mW (typ) total or 195 mW/port (bidirectional) and option to turn off unused ports, the DS125MB203 enables energy-efficient system design. A single supply of 3.3 V or 2.5 V is required to power the device.

The programmable settings can be applied via pin settings, SMBus (I2C) protocol or an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up. This eliminates the need for an external microprocessor or software driver.

Typical Application



Pin Diagram



NOTE: Above 54-lead QFN graphic is a TOP VIEW, looking down through the package.

Figure 1. DS125MB203 Pin Diagram 54 Lead WQFN Package
See Package Number NJY0054A

PIN DESCRIPTIONS(1)

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Speed I/O's			
D_IN0+, D_IN0-, D_IN1+, D_IN1-	10, 11, 15, 16	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50Ω termination resistor connects D_INn+ to VDD and D_INn- to VDD. AC coupling required on high-speed I/O
D_OUT0+, D_ OUT0-, D_OUT1+, D_OUT1-	3, 4, 7, 8	O	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
S_INA0+, S_INA0-, S_INA1+, S_INA1-	45, 44, 40, 39	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50Ω termination resistor connects S_INAn+ to VDD and S_INAn- to VDD. AC coupling required on high-speed I/O
S_OUTA0+, S_OUTA0-, S_OUTA1+, S_OUTA1-	35, 34, 31, 30	O	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
S_INB0+, S_INB0-, S_INB1+, S_INB1-	43, 42, 38, 37	I	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50Ω termination resistor connects S_INBn+ to VDD and S_INBn- to VDD. AC coupling required on high-speed I/O
S_OUTB0+, S_OUTB0-, S_OUTB1+, S_OUTB1-	33, 32, 29, 28	O	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
Control Pins - Shared (LVCMOS)			
ENSMB	48	I, FLOAT, LVCMOS	System Management Bus (SMBus) enable pin Tie 1kΩ to VDD = Register Access SMBus Slave mode FLOAT = Read External EEPROM (Master SMBUS Mode) Tie 1kΩ to GND = Pin Mode
ENSMB = 1 (SMBUS SLAVE MODE), Float (SMBUS MASTER MODE)			
SCL	50	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode SMBUS clock input pin is enabled (slave mode) SMBUS clock output when loading configuration from EEPROM (master mode)
SDA	49	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bidirectional SDA pin is enabled. Data input or open drain (pull-down only) output.
AD0-AD3	54, 53, 47, 46	I, LVCMOS	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs.
$\overline{\text{READ\_EN}}$	26	I, LVCMOS	ENSMB = FLOAT (SMBUS master mode) When using an External EEPROM, a transition from high to low starts the load from the external EEPROM
ENSMB = 0 (PIN MODE)			
EQ_D0, EQ_D1 EQ_S0, EQ_S1	20, 19 46, 47	I, 4-LEVEL, LVCMOS	EQ_D[1:0] and EQ_S[1:0] control the level of equalization on the high speed input pins. The pins are active only when ENSMB is deasserted (low). The input are organized into two sides. The D side is controlled with the EQ_D[1:0] pins and the S side is controlled with the EQ_S[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The EQ_S[1:0] pins are converted to SMBUS AD2/ AD3 inputs. EQ_D[1:0] pins are not used. See Table 2

(1) LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not ensured. Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%. Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%. For 3.3V mode operation, VIN pin = 3.3V and the "VDD" for the 4-level input is 3.3V. For 2.5V mode operation, VDD pin = 2.5V and the "VDD" for the 4-level input is 2.5V.

PIN DESCRIPTIONS[1] (continued)

Pin Name	Pin Number	I/O, Type	Pin Description
DEM_S0, DEM_S1 DEM_D0, DEM_D1	49, 50 53, 54	I, 4-LEVEL, LVCMOS	DEM_D[1:0] and DEM_S[1:0] control the level of VOD and de-emphasis on the high speed output. The pins are active only when ENSMB is deasserted (low). The output are organized into two sides. The D side is controlled with the DEM_D[1:0] pins and the S side is controlled with the DEM_S[1:0] pins. When ENSMB goes high the SMBus registers provide independent control of each channel. The DEM_D[1:0] and DEM_S[1:0] pins are converted to SMBUS AD1/AD0 and SCL/SDA inputs. See Table 3
Control Pins — Both Pin and SMBus Modes (LVCMOS)			
MODE	21	I, 4-LEVEL, LVCMOS	MODE control pin selects operating modes. Tie 1kΩ to GND = GEN 1,2 and SAS 1,2 Float = Auto Mode Select (for PCIe) Tie 20kΩ to GND = PCIe GEN-3 without De-emphasis Tie 1kΩ to VDD = PCIe GEN-3 with De-emphasis See Table 7
INPUT_EN	22	I, 4-LEVEL, LVCMOS	0: Normal Operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 ohms. 20kΩ to GND: Reserved FLOAT: AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable 1: Normal Operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 ohms.
SEL0	23	I, 4-LEVEL, LVCMOS	Select pin for Lane 0. 0: selects input **S_INB0+/-**, output **S_OUTB0+/-**. 20kΩ to GND: selects input **S_INB0+/-**, output **S_OUTA0+/-**. FLOAT: selects input **S_INA0+/-**, output **S_OUTB0+/-**. 1: selects input **S_INA0+/-**, output **S_OUTA0+/-**.
SEL1	26	I, 4-LEVEL, LVCMOS	Select pin for Lane 1. 0: selects input **S_INB1+/-**, output **S_OUTB1+/-**. 20kΩ to GND: selects input **S_INB1+/-**, output **S_OUTA1+/-**. FLOAT: selects input **S_INA1+/-**, output **S_OUTB1+/-**. 1: selects input **S_INA1+/-**, output **S_OUTA1+/-**.
VDD_SEL	25	I, FLOAT	Controls the internal regulator FLOAT = 2.5V mode Tied to GND: 3.3V mode
PWDN	52	I, LVCMOS	0: Normal Operation (device is enabled). 1: Low Power Mode.
Output (LVCMOS)			
$\overline{\text{ALL\_DONE}}$	27	0, LVCMOS	Valid Register Load Status Output 0: External EEPROM load passed 1: External EEPROM load failed
Power			
VIN	24	Power	In 3.3V mode, feed 3.3V +/-10% to VIN In 2.5V mode, leave floating.
VDD	9, 14,36, 41, 51	Power	Power supply pins CML/analog 2.5V mode, connect to 2.5V +/-5% 3.3V mode, connect 0.1 uF cap to each VDD pin
GND	DAP	Power	Ground pad (DAP - die attach pad).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (VDD - 2.5V mode)		-0.5V to +2.75V
Supply Voltage (VIN - 3.3V mode)		-0.5V to +4.0V
LVCMOS Input/Output Voltage		-0.5V to +4.0V
CML Input Voltage		-0.5V to (VDD+0.5)
CML Input Current		-30 to +30 mA
Junction Temperature		125°C
Storage Temperature		-40°C to +125°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Derate NJY0054A Package		52.6mW/°C above +25°C
ESD Rating	HBM, STD - JESD22-A114F	3 kV
	MM, STD - JESD22-A115-A	150 V
	CDM, STD - JESD22-C101-D	1000 V
Thermal Resistance	θ_{JC}	11.5°C/W
	θ_{JA}, No Airflow, 4 layer JEDEC	19.1°C/W
For soldering specifications: See application note SNOA549.		

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage (2.5V mode)	2.375	2.5	2.625	V
Supply Voltage (3.3V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V
Supply Noise up to 50 MHz[1]			100	mVp-p

(1) Allowed supply noise (mVp-p sine wave) under typical conditions.

Electrical Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Power						
IDD	Power Dissipation	VDD = 2.5 V supply EQ Enabled, VOD = 1.0 Vp-p, PWDN = 0		390	500	mW
		VIN = 3.3 V supply EQ Enabled, VOD = 1.0 Vp-p, PWDN = 0		515	685	mW
LVCMOS / LVTTL DC Specifications						
V_{ih}	High Level Input Voltage		2.0		3.6	V
V_{il}	Low Level Input Voltage		0		0.8	V
V_{oh}	High Level Output Voltage (ALL_DONE pin)	I_{oh}= −4mA	2.0			V

Electrical Characteristics (continued)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{ol}	Low Level Output Voltage (ALL_DONE pin)	I_{ol}= 4mA			0.4	V
I_{ih}	Input High Current (RESET pin)	VIN = 3.6 V, LVCMOS = 3.6 V	-15		+15	uA
	Input High Current with internal resistors (4–level input pin)		+20		+150	uA
I_{il}	Input Low Current (RESET pin)	VIN = 3.6 V, LVCMOS = 0 V	-15		+15	uA
	Input Low Current with internal resistors (4–level input pin)		-160		-40	uA
CML Receiver Inputs (IN_n+, IN_n-)						
$RL_{rx\text{-}diff}$	RX Differential return loss	0.05 - 7.5 GHz		-15		dB
		7.5 - 15 GHz		-5		dB
$RL_{rx\text{-}cm}$	RX Common mode return loss	0.05 - 5 GHz		-10		dB
$Z_{rx\text{-}dc}$	RX DC common mode impedance	Tested at VDD = 2.5 V	40	50	60	Ω
$Z_{rx\text{-}diff\text{-}dc}$	RX DC differntial mode impedance	Tested at VDD = 2.5 V	80	100	120	Ω
$V_{rx\text{-}diff\text{-}dc}$	Differential RX peak to peak voltage (VID)	Tested at pins	0.6	1.0	1.2	V
$V_{rx\text{-}signal\text{-}det\text{-}diff\text{-}pp}$	Signal detect assert level for active data signal	0101 pattern at 12.5 Gbps		180		mVp-p
$V_{rx\text{-}idle\text{-}det\text{-}diff\text{-}pp}$	Signal detect de-assert level for electrical idle	0101 pattern at 12.5 Gbps		110		mVp-p
High Speed Outputs						
$V_{tx\text{-}diff\text{-}pp}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, terminated by 50Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEM_x[1:0] = R, F, (1)	0.8	1.0	1.2	Vp-p
$V_{tx\text{-}de\text{-}ratio\_3.5}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM_x[1:0] = R, F		-3.5		dB
$V_{tx\text{-}de\text{-}ratio\_6}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEM_x[1:0] = F, 0		-6		dB
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX Dj > 1.5 MHz				0.15	UI
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	TX RMS jitter < 1.5 MHz				3.0	ps RMS
$T_{TX\text{-}RISE\text{-}FALL}$	TX rise/fall time	20% to 80% of differential output voltage	35	45		ps
$T_{RF\text{-}MISMATCH}$	TX rise/fall mismatch	20% to 80% of differential output voltage		0.01	0.1	UI
$RL_{TX\text{-}DIFF}$	TX Differential return loss	0.05 - 7.5 GHz		-15		dB
		7.5 - 15 GHz		-5		dB
$RL_{TX\text{-}CM}$	TX Common mode return loss	0.05 - 5 GHz		-10		dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance			100		Ω
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	TX AC common mode voltage	VOD = 1.0 Vp-p, DEM_x[1:0] = R, F			100	mVpp
$I_{TX\text{-}SHORT}$	TX short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle				100	mV

(1) In PCIe GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEM_x[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS125MB203 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCIe GEN3 handshake negotiation link training.

Electrical Characteristics (continued)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltgae between TX+ and TX-				25	mV
$T_{TX-IDLE-DATA}$	Max time to transition to differential DATA signal after IDLE	VID = 1.0 Vp-p, 8 Gbps		3.5		ns
$T_{TX-DATA-IDLE}$	Max time to transition to IDLE after differential DATA signal	VID = 1.0 Vp-p, 8 Gbps		6.2		ns
$T_{PLHD/PHLD}$	Differential Propagation Delay	EQ = 00, (2)		200		ps
T_{LSK}	Lane to lane skew	T = 25C, VDD = 2.5V		25		ps
T_{PPSK}	Part to part propagation delay skew	T = 25C, VDD = 2.5V		40		ps
$T_{MUX-SWITCH}$	Mux/Switch Time			100		ns
Equalization						
DJE1	Residual deterministic jitter at 12 Gbps	30” 5mils FR4, VID = 0.6 Vp-p, PRBS15, **EQ = 07'h,** DEM = 0 dB		0.18		UI
DJE2	Residual deterministic jitter at 8 Gbps	30” 5mils FR4, VID = 0.6 Vp-p, PRBS15, **EQ = 07'h,** DEM = 0 dB		0.11		UI
DJE3	Residual deterministic jitter at 5 Gbps	30” 5mils FR4, VID = 0.6 Vp-p, PRBS15, **EQ = 07'h,** DEM = 0 dB		0.07		UI
DJE4	Residual deterministic jitter at 12 Gbps	5 meters 30 awg cable, VID = 0.6 Vp-p, PRBS15,**EQ = 07'h,** DEM = 0 dB		0.25		UI
DJE5	Residual deterministic jitter at 12 Gbps	8 meters 30 awg cable, VID = 0.6 Vp-p, PRBS15, **EQ = 0F'h,** DEM = 0 dB		0.33		UI
De-emphasis (MODE = 0)						
DJD1	Residual deterministic jitter at 12 Gbps	Input Channel: 20” 5mils FR4, Output Channel: 10” 5mils FR4, VID = 0.6 Vp-p, PRBS15, EQ = 03'h, VOD = 1.0 Vp-p, **DEM = −3.5 dB**		0.1		UI

(2) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Unit
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(1)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(1) (2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V, (1) (2) (3)		2000		Ω
		Pullup V_{DD} = 2.5V, (1) (2) (3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
TSU:STA	Repeated Start Condition Setup Time		0.6			µs
TSU:STO	Stop Condition Setup Time		0.6			µs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	(4)	0.6		50	µs
t_F	Clock/Data Fall Time	(4)			300	ns
t_R	Clock/Data Rise Time	(4)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	(4) (5)			500	ms

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(5) Ensured by Design. Parameter not tested in production.

TIMING DIAGRAMS

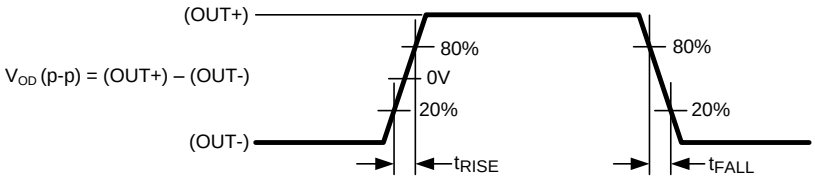


Figure 2. CML Output and Rise and FALL Transition Time

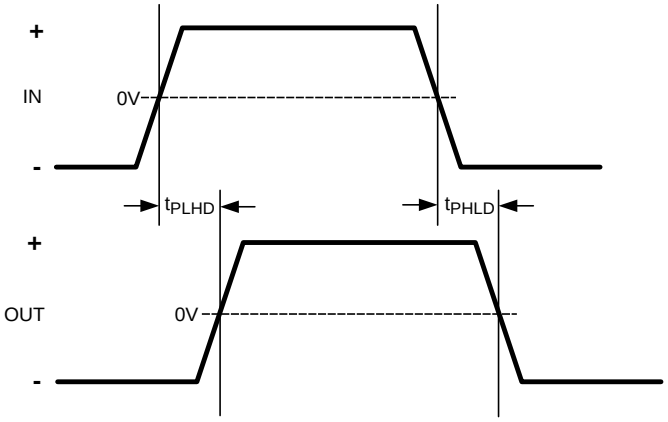


Figure 3. Propagation Delay Timing Diagram

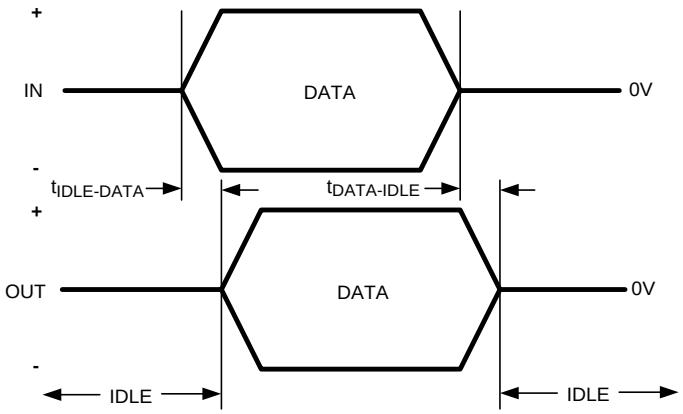


Figure 4. Transmit IDLE-DATA and DATA-IDLE Response Time

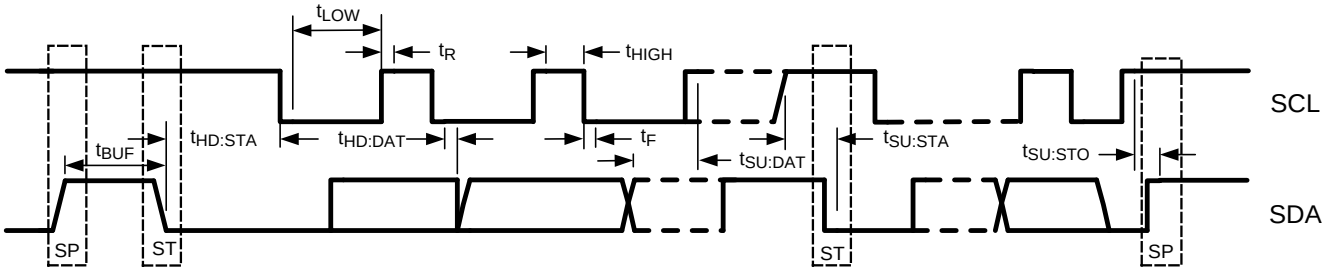


Figure 5. SMBus Timing Parameters

FUNCTIONAL DESCRIPTION

The DS125MB203 is a dual lane 2:1 multiplexer and 1:2 switch or fan-out buffer with signal conditioning. The DS125MB203 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS125MB203 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register informations from external EEPROM; please refer to SMBUS Master Mode for additional information.

Pin Control Mode:

When in pin mode (ENSMB = 0), equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per Table 3. For PCIe applications, the RXDET pins provides automatic and manual control for input termination (50Ω or >50KΩ). MODE setting is also pin controllable with pin selections (Gen 1/2, auto detect and PCIe Gen 3). The receiver electrical idle detect threshold is also adjustable via the SD_TH pin.

SMBUS Mode:

When in SMBus mode (ENSMB = 1), the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB, the EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins (MODE, INPUT_EN, and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PWDN is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most high speed applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de- Emphasis levels are set by registers.

The 4-level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Table 1. 4-Level Control Pin Settings

Level	Setting	3.3V Mode	2.5V Mode
0	Tie 1kΩ to GND	0.10 V	0.08 V
R	Tie 20kΩ to GND	1/3 x V_{IN}	1/3 x V_{DD}
Float	Float (leave pin open)	2/3 x V_{IN}	2/3 x V_{DD}
1	Tie 1kΩ to V_{IN} or V_{DD}	V_{IN} - 0.05 V	V_{DD} - 0.04 V

Typical 4-Level Input Thresholds

- Level 1 - 2 = 0.2 * V_{IN} or V_{DD}
- Level 2 - 3 = 0.5 * V_{IN} or V_{DD}
- Level 3 - 4 = 0.8 * V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5V regulator the 1K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1K resistors into a single lower value resistor. As an example; combining two inputs with a single 500 Ohm resistor is a good way to save board space.

3.3V or 2.5V Supply Mode Operation

The DS125MB203 has an optional internal voltage regulator to provide the 2.5V supply to the device. In 3.3V mode operation, the VIN pin = 3.3V is used to supply power to the device. The internal regulator will provide the 2.5V to the VDD pins of the device and a 0.1 uF cap is needed at each of the 5 VDD pins for power supply de-coupling (total capacitance should be ≤0.5 uF), and the VDD pins should be left open. The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5V mode operation, the VIN pin should be left open and 2.5V supply must be applied to the 5 VDD pins to power the device. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

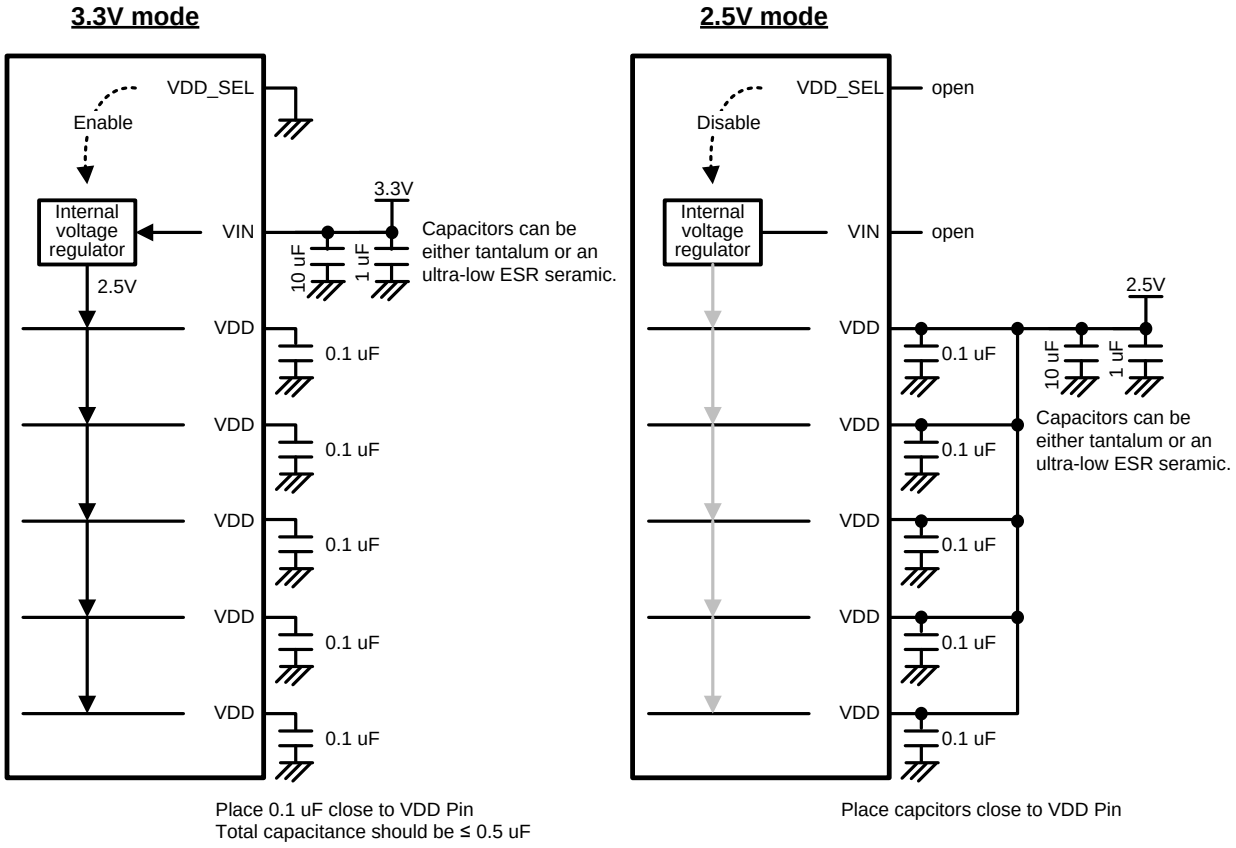


Figure 6. 3.3V or 2.5V Supply Connection Diagram

PCIe Signal Integrity

When using the DS125MB203 in PCIe GEN-3 systems, there are specific signal integrity settings to ensure signal integrity margin. The settings were achieved with completing extensive testing. Please contact your field representative for more information regarding the testing completed to achieve these settings.

For tuning the in the downstream direction (from CPU to EP).

- EQ: use the guidelines outlined in Table 2.
- De-Emphasis: use the guidelines outlined in Table 3.
- VOD: use the guidelines outlined in Table 3.

For tuning in the upstream direction (from EP to CPU).

- EQ: use the guidelines outlined in Table 2.
- De-Emphasis:
  - For trace lengths < 15in set to -3.5 dB
  - For trace lengths > 15in set to -6 dB
- VOD: set to 900 mV

Table 2. Equalizer Settings

Level	EQ_D1 EQ_S1	EQ_D0 EQ_S0	EQ – 8 bits [7:0]	dB at 1.5 GHz	dB at 2.5 GHz	dB at 4 GHz	dB at 6 GHz	Suggested Use(1)
1	0	0	0000 0000 = 0x00	2.5	3.5	3.8	3.1	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	3.8	5.4	6.7	6.7	FR4 5-10 inch trace
3	0	Float	0000 0010 = 0x02	5.0	7.0	8.4	8.4	FR4 10 inch trace
4	0	1	0000 0011 = 0x03	5.9	8.0	9.3	9.1	FR4 15-20 inch trace
5	R	0	0000 0111 = 0x07	7.4	10.3	12.8	13.7	FR4 20-30 inch trace
6	R	R	0001 0101 = 0x15	6.9	10.2	13.9	16.2	FR4 25-30 inch trace
7	R	Float	0000 1011 = 0x0B	9.0	12.4	15.3	15.9	FR4 25-30 inch trace
8	R	1	0000 1111 = 0x0F	10.2	13.8	16.7	17.0	8m, 30awg cable
9	Float	0	0101 0101 = 0x55	8.5	12.6	17.5	20.7	
10	Float	R	0001 1111 = 0x1F	11.7	16.2	20.3	21.8	
11	Float	Float	0010 1111 = 0x2F	13.2	18.3	22.8	23.6	
12	Float	1	0011 1111 = 0x3F	14.4	19.8	24.2	24.7	
13	1	0	1010 1010 = 0xAA	14.4	20.5	26.4	28.0	
14	1	R	0111 1111 = 0x7F	16.0	22.2	27.8	29.2	
15	1	Float	1011 1111 = 0xBF	17.6	24.4	30.2	30.9	
16	1	1	1111 1111 = 0xFF	18.7	25.8	31.6	31.9	

(1) Cable and FR4 lengths are for reference only. FR4 lengths based on a 100 Ohm differential stripline with 5-mil traces and 8-mil trace separation. Optimal EQ setting should be determined via simulation and prototype verification.

Table 3. De-emphasis and Output Voltage Settings

Level	DEM_D1 DEM_S1	DEM_D0 DEM_S0	VOD Vp-p	DEM dB(1)	Inner Amplitude Vp-p	Suggested Use(2)
1	0	0	0.6	0	0.6	FR4 <5 inch 4–mil trace
2	0	R	0.8	0	0.8	FR4 <5 inch 4–mil trace
3	0	Float	0.8	- 3.5	0.55	FR4 10 inch 4–mil trace
4	0	1	0.9	0	1.0	FR4 <5 inch 4–mil trace
5	R	0	0.9	- 3.5	0.45	FR4 10 inch 4–mil trace
6	R	R	0.9	- 6	0.5	FR4 15 inch 4–mil trace
7	R	Float	1.0	0	1.0	FR4 <5 inch 4–mil trace
8	R	1	1.0	- 3.5	0.7	FR4 10 inch 4–mil trace
9	Float	0	1.0	- 6	0.5	FR4 15 inch 4–mil trace
10	Float	R	1.1	0	1.1	FR4 <5 inch 4–mil trace
11	Float	Float	1.1	- 3.5	0.7	FR4 10 inch 4–mil trace
12	Float	1	1.1	- 6	0.55	FR4 15 inch 4–mil trace
13	1	0	1.2	0	1.2	FR4 <5 inch 4–mil trace
14	1	R	1.2	- 3.5	0.8	FR4 10 inch 4–mil trace
15	1	Float	1.2	- 6	0.6	FR4 15 inch 4–mil trace
16	1	1	1.2	- 9	0.45	FR4 20 inch 4–mil trace

(1) The VOD output amplitude and DEM de-emphasis levels are set with the DEMD/S[1:0] pins.
The de-emphasis levels are also available in PCIe GEN-3 mode when MODE = 1 (tied to VDD).
(2) FR4 lengths are for reference only. FR4 lengths based on a 100 Ohm differential stripline with 5-mil traces and 8-mil trace separation. Optimal DEM settings should be determined via simulation and prototype verification.

Table 4. Input Termination Condition with PWDN, INPUT_EN and SEL0 / SEL1

PWDN (PIN 52)	INPUT_EN (PIN 22	SEL0 SEL1	MODE	Input Termination S_INA0 S_INA1	Input Termination S_INB0 S_INB1	Input Termination D_IN0 D_IN1
1	X	X	Low Power	High Z	High Z	High Z
0	0	X	Manual Mux Mode	50 Ω	50 Ω	50 Ω
0	R	X	Reserved	Reserved	Reserved	Reserved
0	F	0	Auto - continuous poll, DIN_B	High Z	Pre Detect: Hi-Z Post Detect: 50 Ω	Pre Detect: Hi-Z Post Detect: 50 Ω
0	F	R	Auto - continuous poll, DIN_B	High Z	Pre Detect: Hi-Z Post Detect: 50 Ω	Pre Detect: Hi-Z Post Detect: 50 Ω
0	F	F	Auto - continuous poll, DIN_A	Pre Detect: Hi-Z Post Detect: 50 Ω	High Z	Pre Detect: Hi-Z Post Detect: 50 Ω
0	F	1	Auto - continuous poll, DIN_A	Pre Detect: Hi-Z Post Detect: 50 Ω	High Z	Pre Detect: Hi-Z Post Detect: 50 Ω
0	1	X	Manual Fanout Mode	50 Ω	50 Ω	50 Ω

RX-Detect Polling in SAS/SATA (up to 6 Gbps) Applications

Unlike PCIe systems, SAS/SATA (up to 6 Gbps) systems use a low speed Out-Of-Band or OOB communications sequence to detect and communicate between Controllers/Expanders and target drives. This communication eliminates the need to detect for endpoints like PCIe. For non-PCIe systems, it is recommended to tie the INPUT_EN pin high or low . This will ensure any OOB sequences sent from the SAS Controller/Expander will reach the target drive without any additional latency due to the termination detection sequence defined by PCIe.

Table 5. Mux/Switch and Fanout Control

SEL0 (PIN 23)	SEL1 (PIN 26)	INPUT_EN (PIN 22)	Description of Connection Path
0	0	0	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
0	0	R	Reserved
0	0	F	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
0	0	1	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0 and S_OUTA0. D_IN1 connects to S_OUTB1 and S_OUTA1.
R	R	0	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
R	R	R	Reserved
R	R	F	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
R	R	1	D_OUT0 connects to S_INB0. D_OUT1 connects to S_INB1. D_IN0 connects to S_OUTB0 and S_OUTA0. D_IN1 connects to S_OUTB1 and S_OUTA1.

Table 5. Mux/Switch and Fanout Control (continued)

F	F	0	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
F	F	R	Reserved
F	F	F	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTB0. S_OUTA0 is in IDLE (output muted). D_IN1 connects to S_OUTB1. S_OUTA1 is in IDLE (output muted).
F	F	1	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTB0 and S_OUTA0. D_IN1 connects to S_OUTB1 and S_OUTA1.
1	1	0	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
1	1	R	Reserved
1	1	F	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0. S_OUTB0 is in IDLE (output muted). D_IN1 connects to S_OUTA1. S_OUTB1 is in IDLE (output muted).
1	1	1	D_OUT0 connects to S_INA0. D_OUT1 connects to S_INA1. D_IN0 connects to S_OUTA0 and S_OUTB0. D_IN1 connects to S_OUTA1 and S_OUTB1.

Table 6. Signal Detect Threshold Level(1)

SMBus REG bit [3:2] and [1:0]	Assert Level (typ)	De-assert Level (typ)
10	210 mVp-p	150 mVp-p
01	160 mVp-p	100 mVp-p
00 (default)	180 mVp-p	110 mVp-p
11	190 mVp-p	130 mVp-p

(1) VDD = 2.5V, 25°C and 0101 pattern at 8 Gbps

Table 7. MODE Operation With Pin Control

MODE (PIN 21)	Driver Characteristics	PCIe	SAS SATA	10G-KR	10GbE	CPRI OBSAI	SRIO (R)XAUI	Interlaken Infiniband
0	Limiting		X		X	X	X	X
R	Transparent without DE							
F (default)	Automatic	X						
1	Transparent with DE			X				

Note: SAS/SATA limited to 6 Gbps. Automatic operation allows input to sense the incoming data-rate and utilize a "Transparent" output driver for operation at or above 8 Gbps.

MODE operation with SMBus Registers

When in SMBus mode (Slave or Master), the MODE pin retains control of the output driver characteristics. In order to override this control function, Register 0x08[2] must be written with a "1". Writting this bit enables MODE control of each channel individually using the channel registers defined in Table 8.

SMBUS Master Mode

The DS125MB203 devices support reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS125MB203 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines below. **NOTE: SEL0, SEL1 and INPUT_EN control are to be set with the external strap pins because there no EEPROM bits to configure them.**

- Set ENSMB = Float — enable the SMBUS master mode.
- The external EEPROM device address byte must be 0xA0'h and capable of 400 kHz operation at 2.5V and 3.3V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.

When tying multiple DS125MB203 devices to the SDA and SCL bus, use these guidelines to configure the devices.

- Use SMBus AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM. Example below is for 4 device.
  - U1: AD[3:0] = 0000 = 0xB0'h,
  - U2: AD[3:0] = 0001 = 0xB2'h,
  - U3: AD[3:0] = 0010 = 0xB4'h,
  - U4: AD[3:0] = 0011 = 0xB6'h
- Use a pull-up resistor on SDA and SCL; value = 2k ohms
- Daisy-chain READEN# (pin 26) and ALL_DONE# (pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  - 1. Tie READEN# of the 1st device in the chain (U1) to GND
  - 2. Tie ALL_DONE# of U1 to READEN# of U2
  - 3. Tie ALL_DONE# of U2 to READEN# of U3
  - 4. Tie ALL_DONE# of U3 to READEN# of U4
  - 5. Optional: Tie ALL_DONE# output of U4 to a LED to show the devices have been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS125MB203 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location, to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS125MB203 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS125MB203 device.

```
:20000000000010000004070 02FAD4002FAD4002FAD4002FAD401805F5A8005F5A8005F5AD8
:20002000 8005F5A800005454 0000000000000000000000000000000000000000000000F6
:20006000000000000000000000000000000000000000000000000000000000000000000080
:20008000000000000000000000000000000000000000000000000000000000000000000060
:2000A000000000000000000000000000000000000000000000000000000000000000000040
:2000C000000000000000000000000000000000000000000000000000000000000000000020
:2000E000000000000000000000000000000000000000000000000000000000000000000000
:20004000000000000000000000000000000000000000000000000000000000000000000A0
```

Table 8. EEPROM Register Map With Default Value

EEPROM Address	Byte	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	0	00	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	RES	RES	RES	RES
Binary			0	0	0	0	0	0	0	0
Description	1	00	RES	RES	RES	RES	RES	RES	RES	RES
Binary			0	0	0	0	0	0	0	0
Description	2	10	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Binary			0	0	0	1	0	0	0	0
Description	3	00	PWDN_ch7	PWDN_ch6	PWDN_ch5	PWDN_ch4	PWDN_ch3	PWDN_ch2	PWDN_ch1	PWDN_ch0
Binary			0	0	0	0	0	0	0	0
Description	4	00	RES	RES	RES	RES	Ovrd_RESET	RES	RES	RES
Binary			0	0	0	0	0	0	0	0
Description	5	04	RES	RES	RES	RES	RES	rxdet_btb_en	RES	RES
Binary			0	0	0	0	0	1	0	0
Description	6	07	RES	Ovrd_RX_DET	Ovrd_MODE	RES	RES	rx_delay_sel_2	rx_delay_sel_1	rx_delay_sel_0
Binary			0	0	0	0	0	1	1	1
Description	7	00	RD_delay_sel_3	RD_delay_sel_2	RD_delay_sel_1	RD_delay_sel_0	RES	RES	ch0_RXDET_1	ch0_RXDET_0
Binary			0	0	0	0	0	0	0	0
Description	8	2F	ch0_BST_7	ch0_BST_6	ch0_BST_5	ch0_BST_4	ch0_BST_3	ch0_BST_2	ch0_BST_1	ch0_BST_0
Binary			0	0	1	0	1	1	1	1
Description	9	AD	ch0_RES	ch0_RES	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_RES_2	ch0_RES_1	ch0_RES_0
Binary			1	0	1	0	1	1	0	1
Description	10	40	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_Slow	ch0_RES_1	ch0_RES_0	ch0_RES_1	ch0_RES_0
Binary			0	1	0	0	0	0	0	0
Description	11	02	ch1_RES	ch1_RES	ch1_RXDET_1	ch1_RXDET_0	ch1_BST_7	ch1_BST_6	ch1_BST_5	ch1_BST_4
Binary			0	0	0	0	0	0	1	0
Description	12	FA	ch1_BST_3	ch1_BST_2	ch1_BST_1	ch1_BST_0	ch1_Sel_scp	ch1_Sel_MODE	ch1_RES_2	ch1_RES_1
Binary			1	1	1	1	1	0	1	0
Description	13	D4	ch1_RES_0	ch1_VOD_2	ch1_VOD_1	ch1_VOD_0	ch1_DEM_2	ch1_DEM_1	ch1_DEM_0	ch1_Slow
Binary			1	1	0	1	0	1	0	0
Description	14	00	ch1_RES_1	ch1_RES_0	ch1_RES_1	ch1_RES_0	ch2_RES	ch2_RES	ch2_RXDET_1	ch2_RXDET_0
Binary			0	0	0	0	0	0	0	0
Description	15	2F	ch2_BST_7	ch2_BST_6	ch2_BST_5	ch2_BST_4	ch2_BST_3	ch2_BST_2	ch2_BST_1	ch2_BST_0
Binary			0	0	1	0	1	1	1	1

Table 8. EEPROM Register Map With Default Value (continued)

EEPROM Address	Byte	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	16	AD	ch2_RES	ch2_RES	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_RES_2	ch2_RES_1	ch2_RES_0
Binary			1	0	1	0	1	1	0	1
Description	17	40	ch2_RES_2	ch2_RES_1	ch2_RES_0	ch2_Slow	ch2_RES_1	ch2_RES_0	ch2_RES_1	ch2_RES_0
Binary			0	1	0	0	0	0	0	0
Description	18	02	ch3_RES	ch3_RES	ch3_RXDET_1	ch3_RXDET_0	ch3_BST_7	ch3_BST_6	ch3_BST_5	ch3_BST_4
Binary			0	0	0	0	0	0	1	0
Description	19	FA	ch3_BST_3	ch3_BST_2	ch3_BST_1	ch3_BST_0	ch3_Sel_scp	ch3_Sel_MODE	ch3_RES_2	ch3_RES_1
Binary			1	1	1	1	1	0	1	0
Description	20	D4	ch3_RES_0	ch3_VOD_2	ch3_VOD_1	ch3_VOD_0	ch3_DEM_2	ch3_DEM_1	ch3_DEM_0	ch3_Slow
Binary			1	1	0	1	0	1	0	0
Description	21	01	ch3_RES_1	ch3_RES_0	ch3_RES_1	ch3_RES_0	ovrd_fast_idle	en_h_idle_th_n	en_h_idle_th_s	en_fast_idle_n
Binary			0	0	0	0	0	0	0	1
Description	22	80	en_fast_idle_s	eqsd_mgain_n	eqsd_mgain_s	ch4_RES	ch4_RES	ch4_RXDET_1	ch4_RXDET_0	ch4_BST_7
Binary			1	0	0	0	0	0	0	0
Description	23	5F	ch4_BST_6	ch4_BST_5	ch4_BST_4	ch4_BST_3	ch4_BST_2	ch4_BST_1	ch4_BST_0	ch4_Sel_scp
Binary			0	1	0	1	1	1	1	1
Description	24	5A	ch4_Sel_MODE	ch4_RES_2	ch4_RES_1	ch4_RES_0	ch4_VOD_2	ch4_VOD_1	ch4_VOD_0	ch4_DEM_2
Binary			0	1	0	1	1	0	1	0
Description	25	80	ch4_DEM_1	ch4_DEM_0	ch4_Slow	ch4_RES_1	ch4_RES_0	ch4_RES_1	ch4_RES_0	ch5_RES
Binary			1	0	0	0	0	0	0	0
Description	26	05	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES	ch5_RES
Binary			0	0	0	0	0	1	0	1
Description	27	F5	ch5_RES	ch5_RES	ch5_RES	ch5_Sel_scp	ch5_Sel_MODE	ch5_RES_2	ch5_RES_1	ch5_RES_0
Binary			1	1	1	1	0	1	0	1
Description	28	A8	ch5_VOD_2	ch5_VOD_1	ch5_VOD_0	ch5_DEM_2	ch5_DEM_1	ch5_DEM_0	ch5_Slow	ch5_RES_1
Binary			1	0	1	0	1	0	0	0
Description	29	00	ch5_RES_0	ch5_RES_1	ch5_RES_0	ch6_RES	ch6_RES	ch6_RXDET_1	ch6_RXDET_0	ch6_BST_7
Binary			0	0	0	0	0	0	0	0
Description	30	5F	ch6_BST_6	ch6_BST_5	ch6_BST_4	ch6_BST_3	ch6_BST_2	ch6_BST_1	ch6_BST_0	ch6_Sel_scp
Binary			0	1	0	1	1	1	1	1
Description	31	5A	ch6_Sel_MODE	ch6_RES_2	ch6_RES_1	ch6_RES_0	ch6_VOD_2	ch6_VOD_1	ch6_VOD_0	ch6_DEM_2
Binary			0	1	0	1	1	0	1	0

Table 8. EEPROM Register Map With Default Value (continued)

EEPROM Address	Byte	HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Blt 0
Description	32	80	ch6_DEM_1	ch6_DEM_0	ch6_Slow	ch6_RES_1	ch6_RES_0	ch6_RES_1	ch6_RES_0	ch7_RES
Binary			1	0	0	0	0	0	0	0
Description	33	05	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES	ch7_RES
Binary			0	0	0	0	0	1	0	1
Description	34	F5	ch7_RES	ch7_RES	ch7_RES	ch7_Sel_scp	ch7_Sel_MODE	ch7_RES_2	ch7_RES_1	ch7_RES_0
Binary			1	1	1	1	0	1	0	1
Description	35	A8	ch7_VOD_2	ch7_VOD_1	ch7_VOD_0	ch7_DEM_2	ch7_DEM_1	ch7_DEM_0	ch7_Slow	ch7_RES_1
Binary			1	0	1	0	1	0	0	0
Description	36	00	ch7_RES_0	ch7_RES_1	ch7_RES_0	iph_dac_ns_1	iph_dac_ns_0	ipp_dac_ns_1	ipp_dac_ns_0	ipp_dac_1
Binary			0	0	0	0	0	0	0	0
Description	37	00	ipp_dac_0	RD23_67	RD01_45	RD_PD_ovrd	RD_Sel_test	RD_RESET_ovrd	PWDB_input_DC	DEM_VOD_ovrd
Binary			0	0	0	0	0	0	0	0
Description	38	54	DEM_ovrd_N2	DEM_ovrd_N1	DEM_ovrd_N0	VOD_ovrd_N2	VOD_ovrd_N1	VOD_ovrd_N0	SPARE0	SPARE1
Binary			0	1	0	1	0	1	0	0
Description	39	54	DEM__ovrd_S2	DEM__ovrd_S1	DEM_ovrd_S0	VOD_ovrd_S2	VOD_ovrd_S1	VOD_ovrd_S0	SPARE0	SPARE1
Binary			0	1	0	1	0	1	0	0

Table 9. Example of EEPROM for Four Devices Using Two Address Maps

EEPROM Address	Address (Hex)	EEPROM Data	Comments
0	00	0x43	CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x0B	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x30	Device 3 Address Location
11	0B	0x00	Begin Device 0, 1 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x00	EQ CHB0 = 00
17	11	0xAB	VOD CHB0 = 1.0V
18	12	0x00	DEM CHB0 = 0 (0dB)
19	13	0x00	EQ CHB1 = 00
20	14	0x0A	VOD CHB1 = 1.0V
21	15	0xB0	DEM CHB1 = 0 (0dB)
22	16	0x00	
23	17	0x00	EQ CHB2 = 00
24	18	0xAB	VOD CHB2 = 1.0V
25	19	0x00	DEM CHB2 = 0 (0dB)
26	1A	0x00	EQ CHB3 = 00
27	1B	0x0A	VOD CHB3 = 1.0V
28	1C	0xB0	DEM CHB3 = 0 (0dB)
29	1D	0x01	
30	1E	0x80	
31	1F	0x01	EQ CHA0 = 00
32	20	0x56	VOD CHA0 = 1.0V
33	21	0x00	DEM CHA0 = 0 (0dB)
34	22	0x00	EQ CHA1 = 00
35	23	0x15	VOD CHA1 = 1.0V
36	24	0x60	DEM CHA1 = 0 (0dB)
37	25	0x00	
38	26	0x01	EQ CHA2 = 00
39	27	0x56	VOD CHA2 = 1.0V
40	28	0x00	DEM CHA2 = 0 (0dB)
41	29	0x00	EQ CHA3 = 00
42	2A	0x15	VOD CHA3 = 1.0V
43	2B	0x60	DEM CHA3 = 0 (0dB)
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	

Table 9. Example of EEPROM for Four Devices Using Two Address Maps (continued)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
47	2F	0x54	End Device 0, 1 - Address Offset 39
48	30	0x00	Begin Device 2, 3 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x00	EQ CHB0 = 00
54	36	0xAB	VOD CHB0 = 1.0V
55	37	0x00	DEM CHB0 = 0 (0dB)
56	38	0x00	EQ CHB1 = 00
57	39	0x0A	VOD CHB1 = 1.0V
58	3A	0xB0	DEM CHB1 = 0 (0dB)
59	3B	0x00	
60	3C	0x00	EQ CHB2 = 00
61	3D	0xAB	VOD CHB2 = 1.0V
62	3E	0x00	DEM CHB2 = 0 (0dB)
63	3F	0x00	EQ CHB3 = 00
64	40	0x0A	VOD CHB3 = 1.0V
65	41	0xB0	DEM CHB3 = 0 (0dB)
66	42	0x01	
67	43	0x80	
68	44	0x01	EQ CHA0 = 00
69	45	0x56	VOD CHA0 = 1.0V
70	46	0x00	DEM CHA0 = 0 (0dB)
71	47	0x00	EQ CHA1 = 00
72	48	0x15	VOD CHA1 = 1.0V
73	49	0x60	DEM CHA1 = 0 (0dB)
74	4A	0x00	
75	4B	0x01	EQ CHA2 = 00
76	4C	0x56	VOD CHA2 = 1.0V
77	4D	0x00	DEM CHA2 = 0 (0dB)
78	4E	0x00	EQ CHA3 = 00
79	4F	0x15	VOD CHA3 = 1.0V
80	50	0x60	DEM CHA3 = 0 (0dB)
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 2, 3 - Address Offset 39

Note: CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. This example has all channels set to EQ = 00 (min boost), VOD = 1.0V, DEM = 0 (0dB) and multiple device can point to the same address map.

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB = 1kΩ to VDD to enable SMBus slave mode and allow access to the configuration registers.

The DS125MB203 has the AD[3:0] inputs in SMBus mode. These pins are the user set SMBUS slave address inputs. The AD[3:0] pins have internal pull-down. When left floating or pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, the DS125MB203 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). The device supports up to 16 address byte, which can be set with the AD[3:0] inputs. Below are the 16 addresses.

Table 10.

AD[3:0] Settings	Address Bytes (HEX)
0000	B0
0001	B2
0010	B4
0011	B6
0100	B8
0101	BA
0110	BC
0111	BE
1000	C0
1001	C2
1010	C4
1011	C6
1100	C8
1101	CA
1110	CC
1111	CE

The SDA, SCL pins are 3.3V tolerant, but are not 5V tolerant. External pull-up resistor is required on the SDA. The resistor value can be from 1 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Table 11 for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

See Table 11 for more information.

Table 11. SMBUS Slave Mode Register Map

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x00	Observation	7	Reserved	R/W	0x00	Set bit to 0.
		6:3	Address Bit AD[3:0]	R		Observation of AD[3:0] bit [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0
		2	EEPROM Read Done	R		1: Device completed the read from external EEPROM.
		1	Reserved	R/W		Set bit to 0.
		0	Reserved	R/W		Set bit to 0.
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Power Down per Channel [7]: CH7 (NC – S_OUTB1) [6]: CH6 (D_IN1 – S_OUTA1) [5]: CH5 (NC – S_OUTB0) [4]: CH4 (D_IN0 – S_OUTA0) [3]: CH3 (D_OUT1 – S_INB1) [2]: CH2 (NC – S_INA1) [1]: CH1 (D_OUT0 – S_INB0) [0]: CH0 (NC – S_INA0) 00'h = all channels enabled FF'h = all channels disabled; device in low power state Note: override RESET pin in Reg_02.
0x02	Override RESET Control	7:1	Reserved	R/W	0x00	Set bits to 0.
		0	Override RESET			1: Block RESET pin control; use Reg_01 to configure. 0: Allow RESET pin control.
0x05	Slave Mode CRC Bits	7:0	CRC bits	R/W	0x00	CRC bits [7:0]
0x06	Slave Register Control	7:5	Reserved	R/W	0x10	Set bits to 0.
		4	Reserved			Set bit to 1.
		3	Register Enable			1: Enables high speed channel control via SMBus registers without CRC 0: Channel control via SMBus registers requires correct CRC in Reg 0x05 Note: In order to change VOD, DEM and EQ of the channels in slave mode without also setting CRC each time, set this bit to 1.
		2:0	Reserved			Set bits to 0.
0x07	Digital Reset and Control	7	Reserved	R/W	0x01	Set bit to 0.
		6	Reset Registers			Self clearing reset for SMBus registers. Writing a [1] will return register settings to default values
		5	Reset SMBus Master			Self clearing reset to SMBus master state machine
		4:0	Reserved			Set bits to 0 0001'b.
0x08	Override RXDET, MODE	7:4	Reserved	R/W	0x00	Set bits to 0.
		3	Override RXDET			1: Block RXDET control; use register to configure. 0: Allow RXDET control.
		2	Override MODE			1: Block MODE pin control; use register to configure. 0: Allow MODE pin control
		1:0				Set bits to 0.

Table 11. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x0E	CH0 - S_INA0 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x0F	CH0 - S_INA0 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.
0x10	Reserved	7:0	Reserved	R/W	0xAD	
0x11	Reserved	7:0	Reserved	R/W	0x02	
0x12	Reserved	7:0	Reserved	R/W	0x00	
0x15	CH1 - S_INB0 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x16	CH1 - S_INB0 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.
0x17	CH1 - D_OUT0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN-3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V

Table 11. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x18	CH1 - D_OUT0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH1 - CHB1. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x19	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x1C	CH2 - S_INA1 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0				Set bits to 0.
0x1D	CH2 - S_INA1 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.
0x1E	Reserved	7:0	Reserved	R/W	0xAD	
0x1F	Reserved	7:0	Reserved	R/W	0x02	
0x20	Reserved	7:0	Reserved	R/W	0x00	
0x23	CH3 - S_INB1 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x24	CH3 - S_INB1 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.

Table 11. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x25	CH3 - D_OUT1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V
0x26	CH3 - D_OUT1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET CH1 - CHB1. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x27	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x2B	CH4 - D_IN0 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.
0x2C	CH4 - D_IN0 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.
0x2D	CH4 - S_OUTA0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V

Table 11. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x2E	CH4 - S_OUTA0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x2F	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x32	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x33	Reserved	7:0	Reserved	R/W	0x2F	
0x34	CH5 - S_OUTB0 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V
0x35	CH5 - S_OUTB0 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x36	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x39	CH6 - D_IN1 RXDET	7:4	Reserved	R/W	0x00	Set bits to 0.
		3:2	RXDET			00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET control in Reg_08.
		1:0	Reserved			Set bits to 0.

Table 11. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x3A	CH6 - D_IN1 EQ	7:0	EQ Control	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.
0x3B	CH6 - S_OUTA1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V
0x3C	CH6 - S_OUTA1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x3D	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x40	Reserved	7:0	Reserved	R/W	0x00	Set bits to 0.
0x41	Reserved	7:0	Reserved	R/W	0x2F	EQ Control - total of 256 levels. See Table 2.
0x42	CH7 - S_OUTB1 VOD	7	Short Circuit Protection	R/W	0xAD	1: Enable the short circuit protection 0: Disable the short circuit protection
		6	MODE Control			1: PCIe GEN 1/2, 10GE 0: PCIe GEN 3, 10G-KR Note: override the MODE pin in Reg_08.
		5:3	Reserved			Set bits to default value - 101.
		2:0	VOD Control			VOD Control 000: 0.6 V 001: 0.7 V 010: 0.8 V 011: 0.9 V 100: 1.0 V 101: 1.1 V (default) 110: 1.2 V 111: 1.3 V

Table 11. SMBUS Slave Mode Register Map (continued)

Address	Register Name	Bit(s)	Field	Type	Default	Description
0x43	CH7 - S_OUTB1 DEM	7	RXDET STATUS	R	0x02	Observation bit for RXDET. CH7 - CHA3. 1: RX = detected 0: RX = not detected
		6:5	MODE STATUS	R		Observation bit for MODE.
		4:3	Reserved	R/W		Set bits to 0.
		2:0	DEM Control	R/W		DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x44	Reserved	7:4	Reserved	R/W	0x00	Set bits to 0.
0x51	Device ID	7:5	VERSION	R	0x46	010'b
		4:0	ID			00110'b
0x5E	Override SEL1, SEL0 and INPUT_EN	7:3	Reserved	R/W	0x00	Set bits to 0.
		2	Override SEL1 pin			1: Block SEL1 pin control; use Reg_5F to configure. 0: Allow SEL1 pin control
		1	Override SEL0 pin			1: Block SEL0 pin control; use Reg_5F to configure. 0: Allow SEL0 pin control
		0	Override INPUT_EN pin			1: Block INPUT_EN pin control; use Reg_5F to configure. 0: Allow INPUT_EN pin control
0x5F	Control SEL1, SEL0 and INPUT_ENl	7:6	SEL1 Control	R/W	0x00	Select for Lane 1. 00: 0 - selects input S_INB1+/-, output S_OUTB1+/-. 01: 20kΩ to GND - selects input S_INB1+/-, output S_OUTA1+/- 10: FLOAT - selects input S_INA1+/-, output S_OUTB1+/- 11: 1 - selects input S_INA1+/-, output S_OUTA1+/-.
		5:4	SEL0 Control			Select for Lane 0. 00: 0 - selects input S_INB0+/-, output S_OUTB0+/-. 01: 20kΩ to GND - selects input S_INB0+/-, output S_OUTA0+/- 10: FLOAT - selects input S_INA0+/-, output S_OUTB0+/- 11: 1 - selects input S_INA0+/-, output S_OUTA0+/-.
		3:2	INPUT_EN Control			00: 0 - Normal Operation, FANOUT is disabled, use SEL0/1 to select the A or B input/output (see SEL0/1 pin), input always enabled with 50 ohms. 01: 20kΩ to GND - Reserved. 10: FLOAT - AUTO - Use RX Detect, SEL0/1 to determine which input or output to enable, FANOUT is disable. 11: 1 - Normal Operation, FANOUT is enabled (both S_OUT0/1 are ON). Input always enabled with 50 ohms.
		1:0	Reserved			Set bits to 0.

APPLICATIONS INFORMATION

GENERAL RECOMMENDATIONS

The DS125MB203 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and LPDS outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187(SNOA401) for additional information on QFN (WQFN) packages.

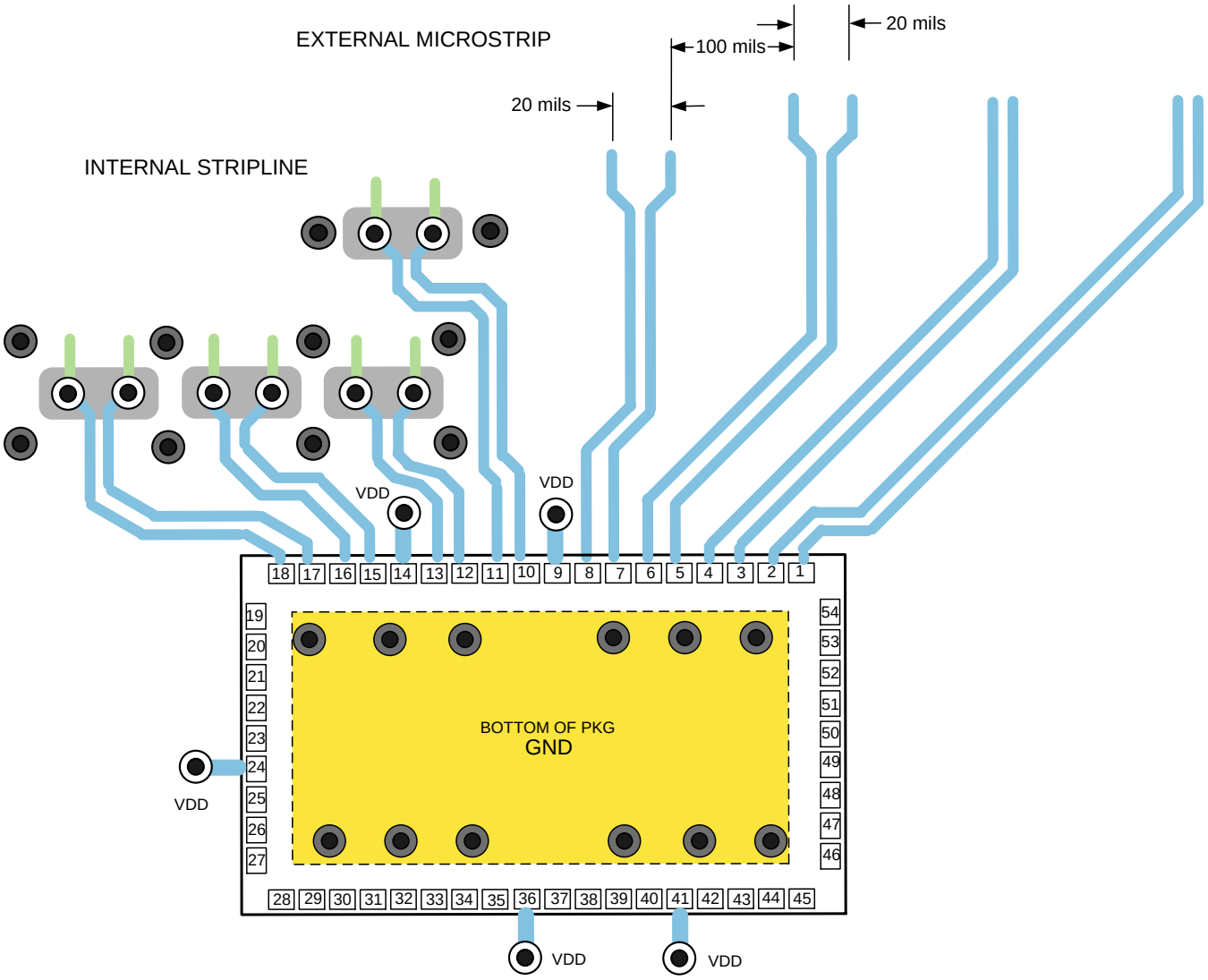


Figure 7. Typical Routing Options

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the deterimential high frequency effects of stubs on the signal path.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS125MB203 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS125MB203. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Typical Performance Curves Characteristics

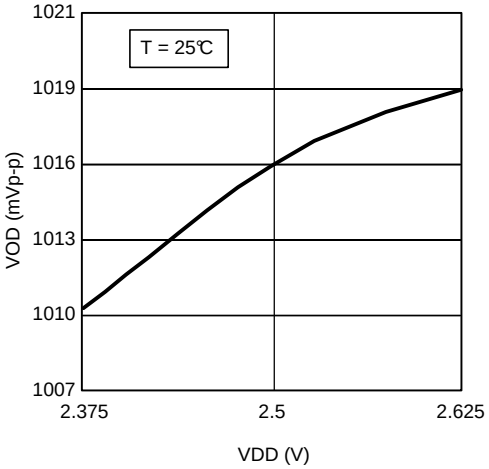


Figure 8. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Supply Voltage (VDD)

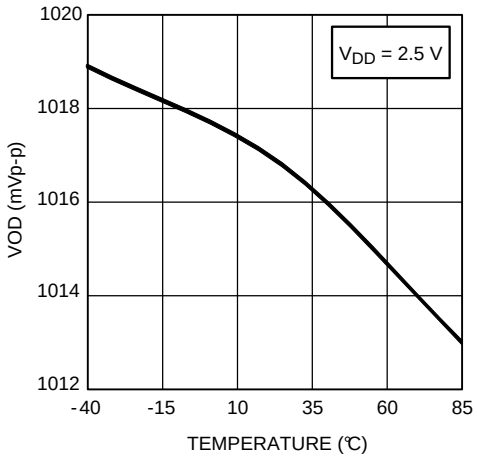


Figure 9. Output Differential Voltage (VOD = 1.0 Vp-p) vs. Temperature

Typical Performance Eye Diagrams Characteristics

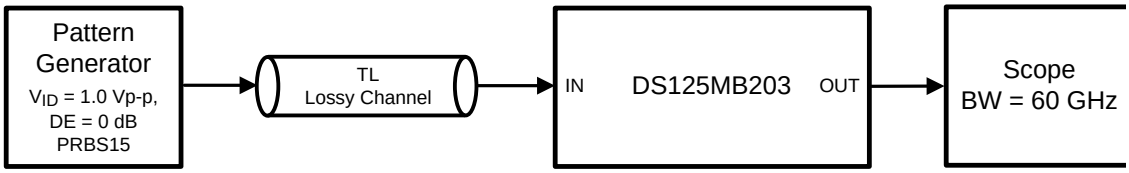


Figure 10. Test Setup Connections Diagram

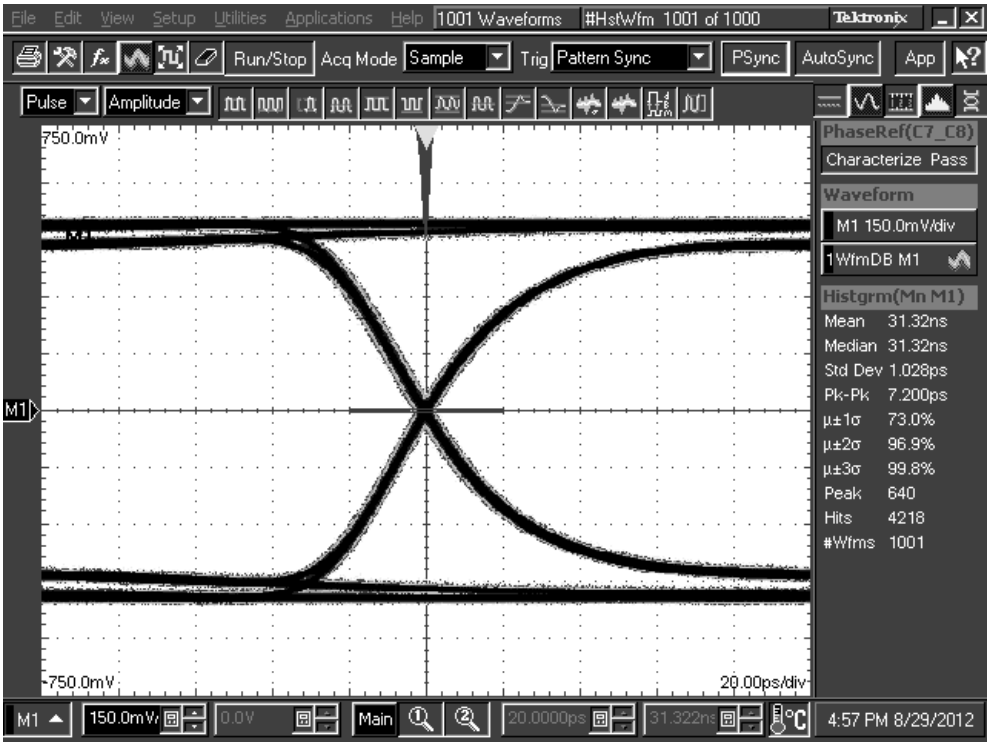


Figure 11. TL = 10 inch 5–mil FR4 trace, 5 Gbps
DS125MB203 settings: EQ[1:0] = 0, F = 02'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

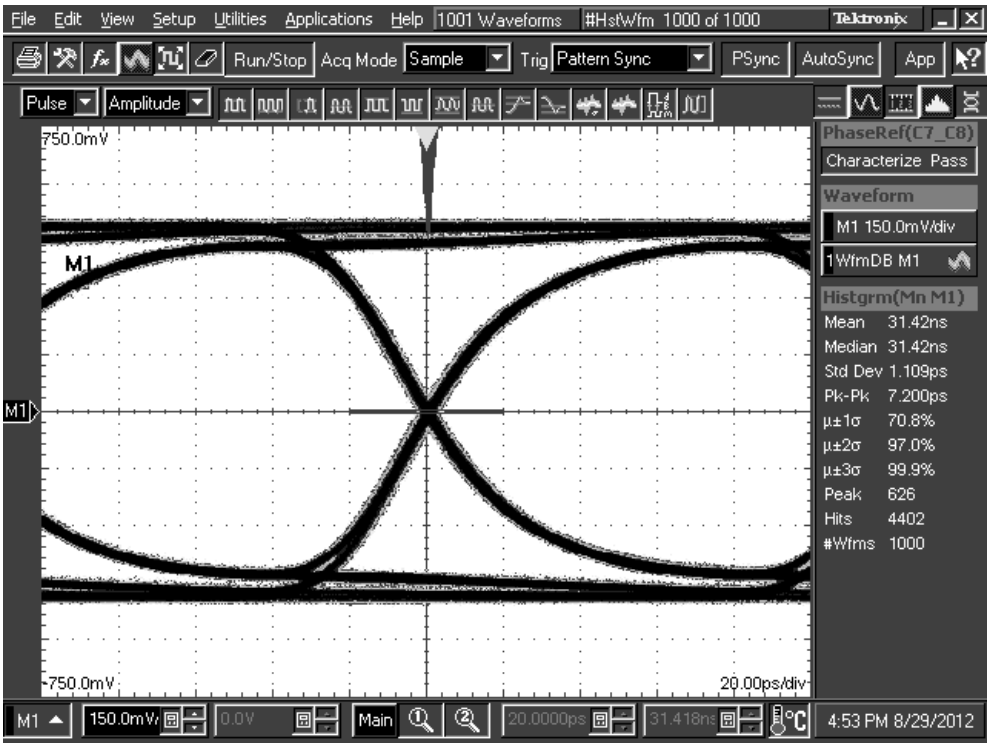


Figure 12. TL = 10 inch 5–mil FR4 trace, 8 Gbps
DS125MB203 settings: EQ[1:0] = 0, F = 02'h, DEM[1:0] = 0, 1

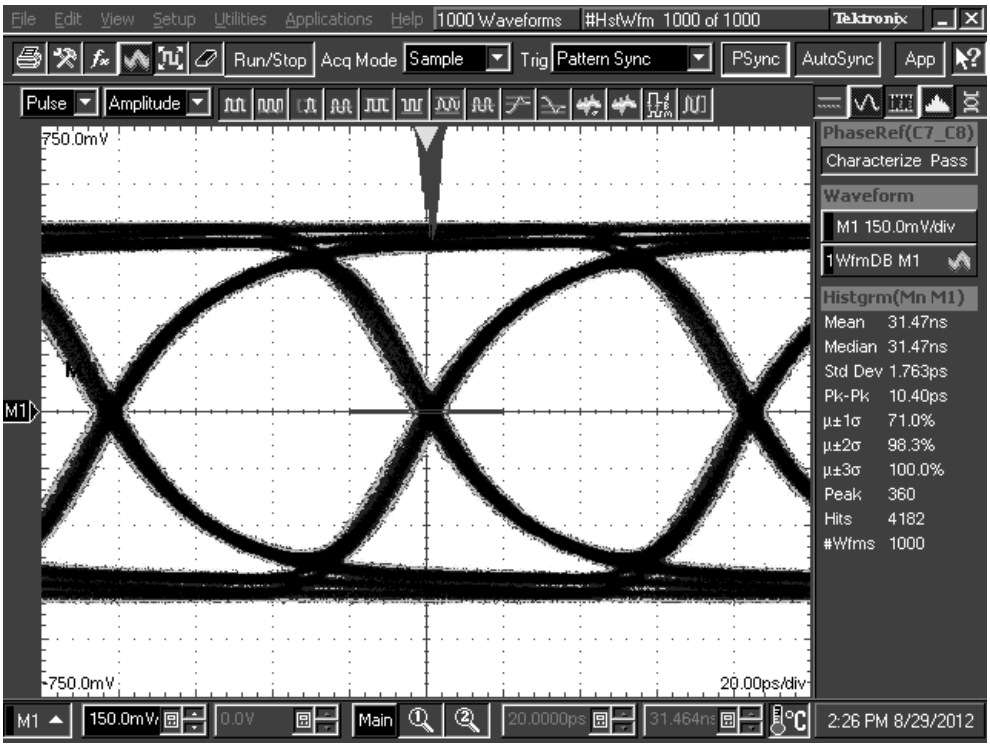


Figure 13. TL = 10 inch 5–mil FR4 trace, 12 Gbps
DS125MB203 settings: EQ[1:0] = 0, R = 01'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

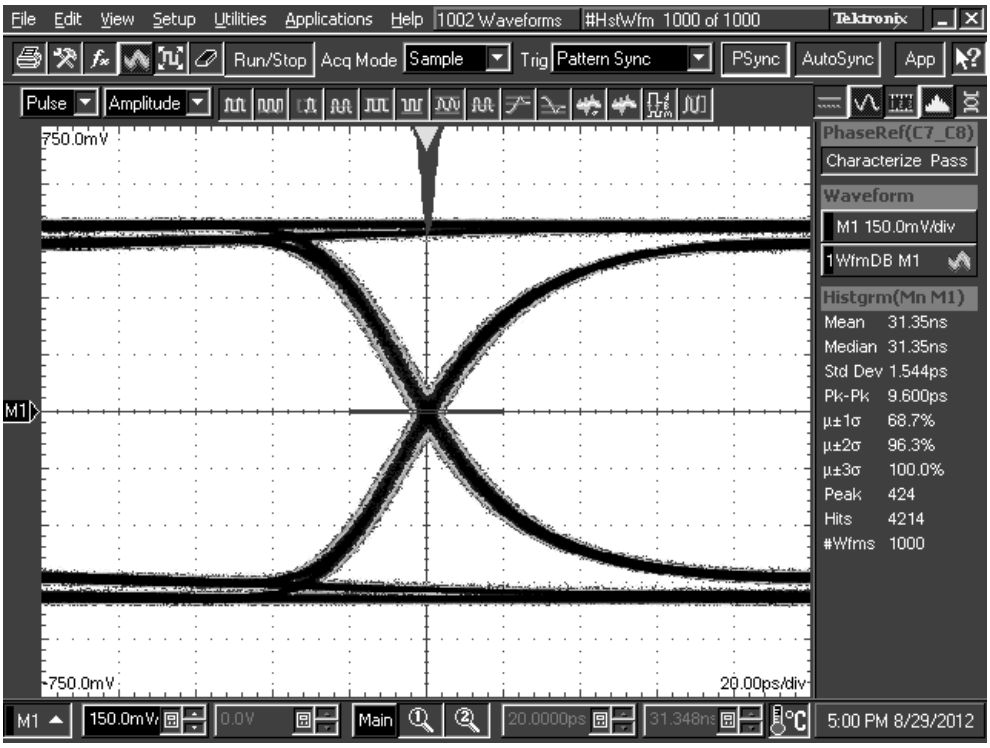


Figure 14. TL = 20 inch 5–mil FR4 trace, 5 Gbps
DS125MB203 settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = 0, 1

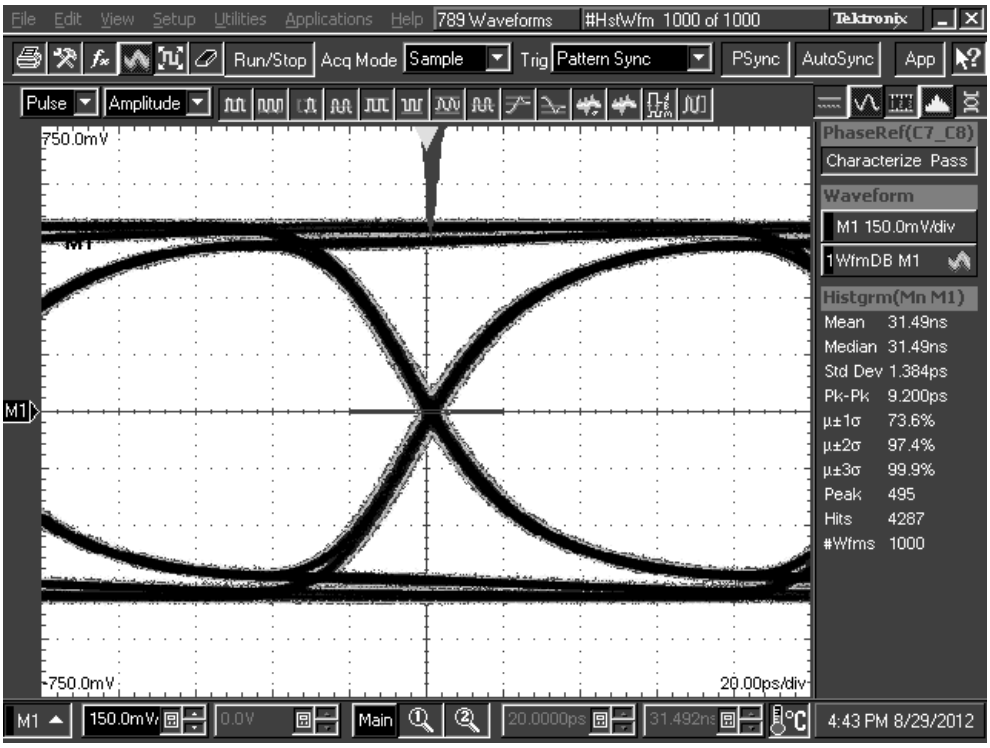


Figure 15. TL = 20 inch 5–mil FR4 trace, 8 Gbps
DS125MB203 settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

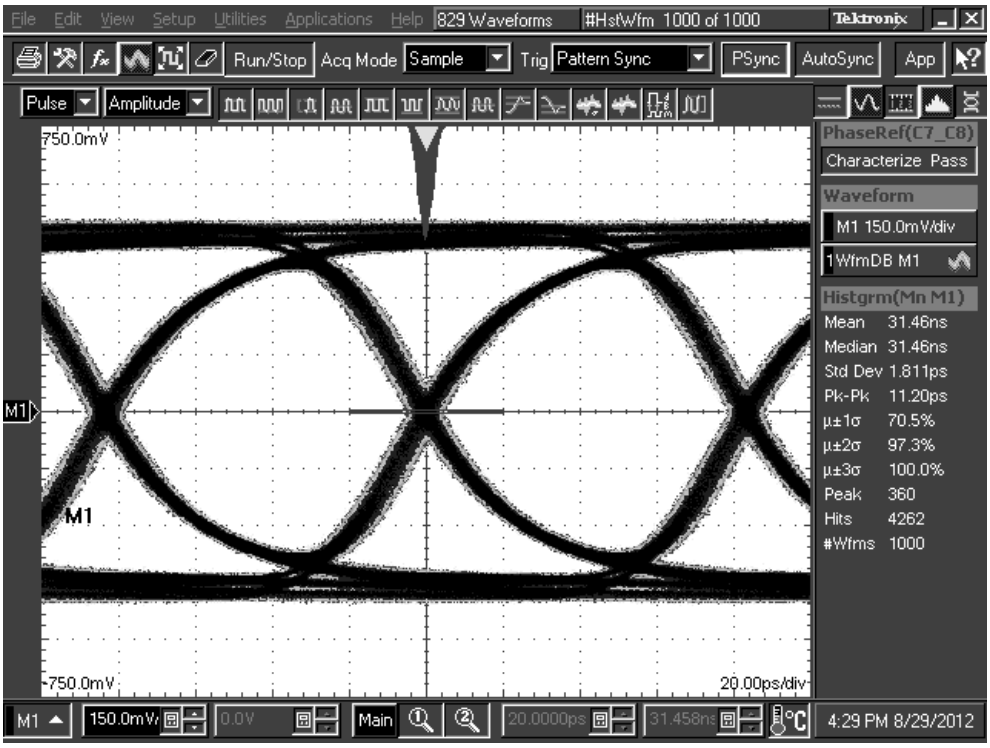


Figure 16. TL = 20 inch 5–mil FR4 trace, 12 Gbps
DS125MB203 settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = 0, 1

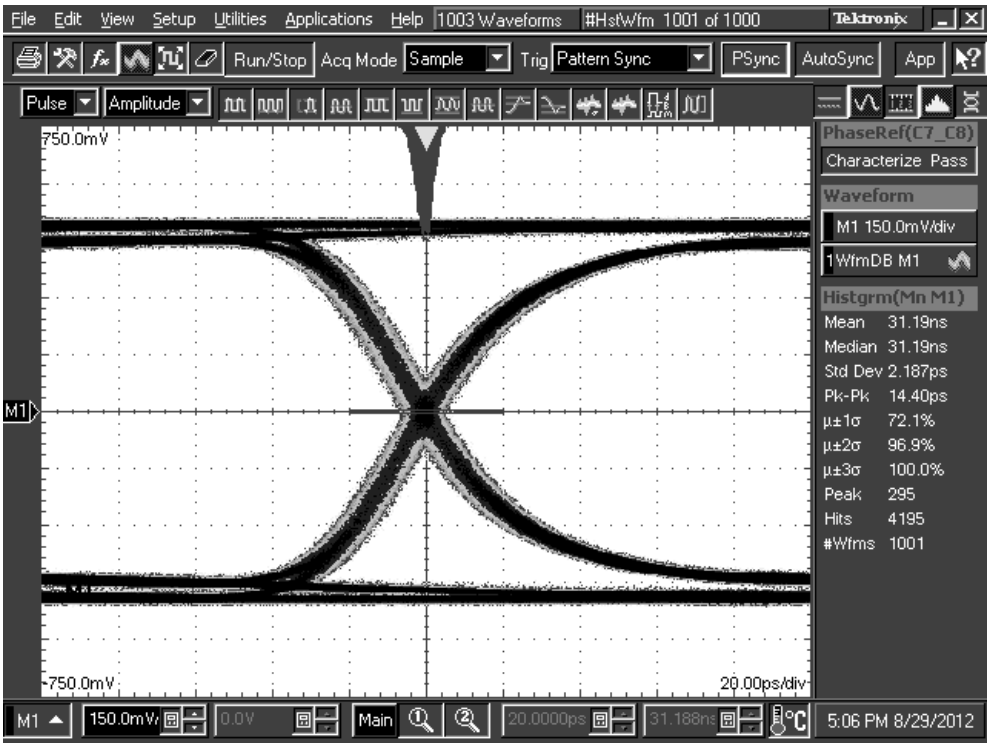


Figure 17. TL = 30 inch 5–mil FR4 trace, 5 Gbps
DS125MB203 settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

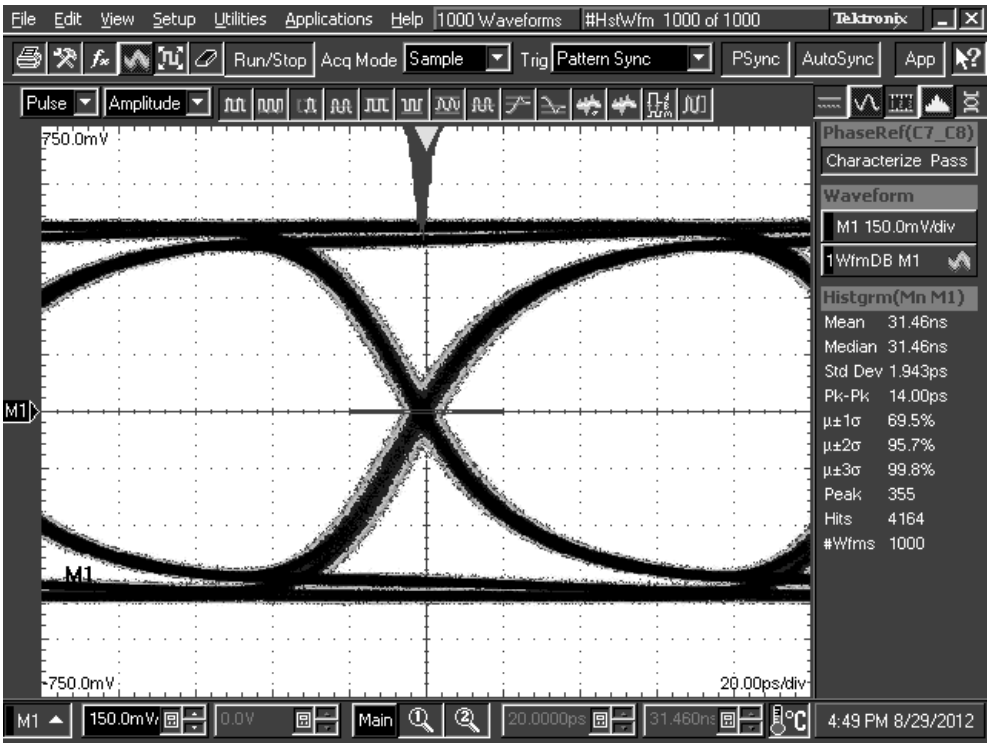


Figure 18. TL = 30 inch 5–mil FR4 trace, 8 Gbps
DS125MB203 settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

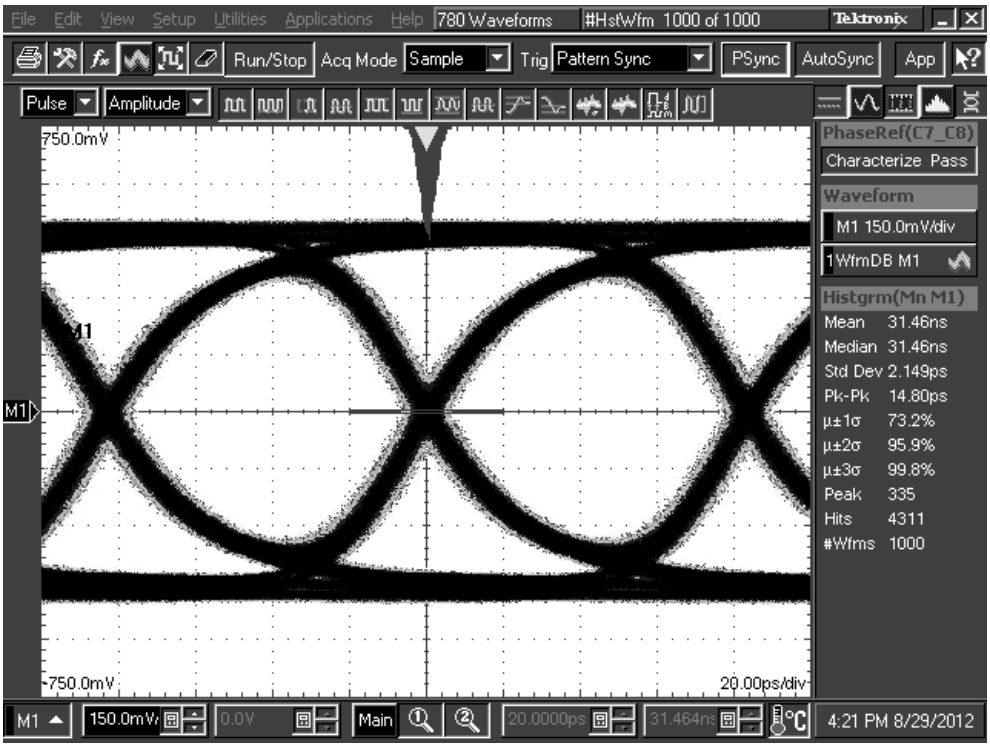


Figure 19. TL = 30 inch 5–mil FR4 trace, 12 Gbps
DS125MB203 settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

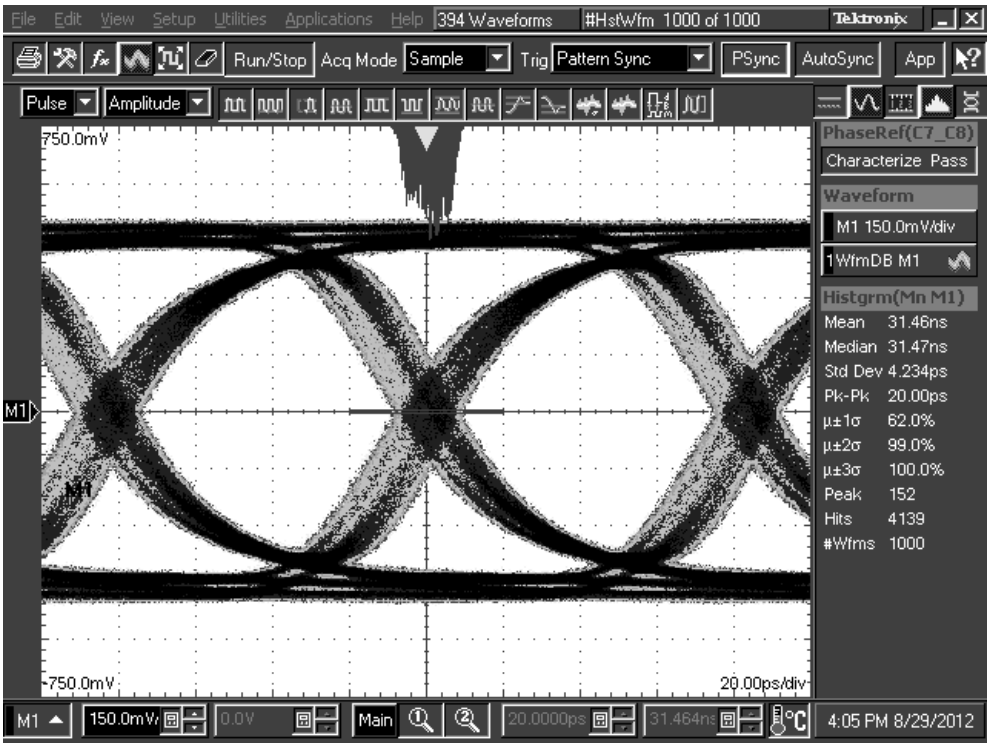


Figure 20. TL1 = 5-meter 30-AWG 100 Ohm Twin-axial Cable, 12 Gbps
DS125MB203 settings: EQ[1:0] = R, 0 = 07'h, DEM[1:0] = 0, 1

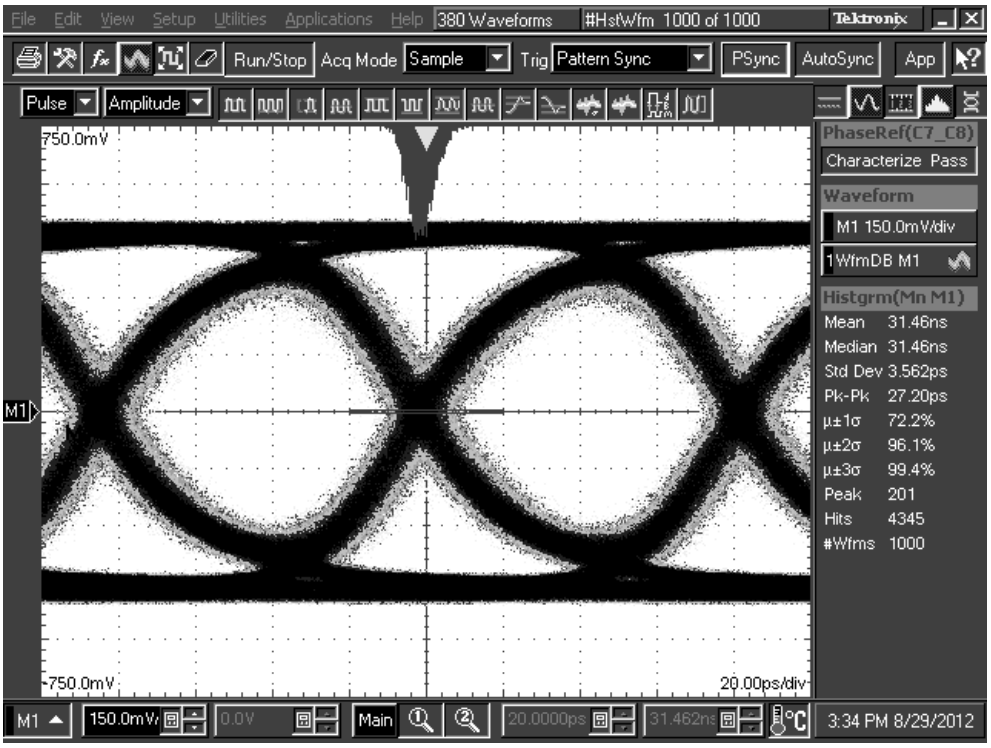


Figure 21. TL1 = 8-meter 30-AWG 100 Ohm Twin-axial Cable, 12 Gbps
DS125MB203 settings: EQ[1:0] = R, 1 = 0F'h, DEM[1:0] = 0, 1

Typical Performance Eye Diagrams Characteristics (continued)

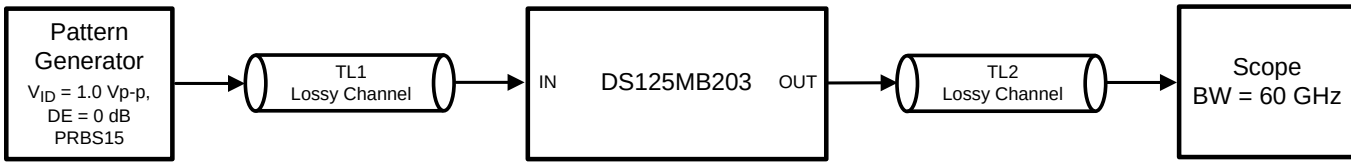


Figure 22. Test Setup Connections Diagram

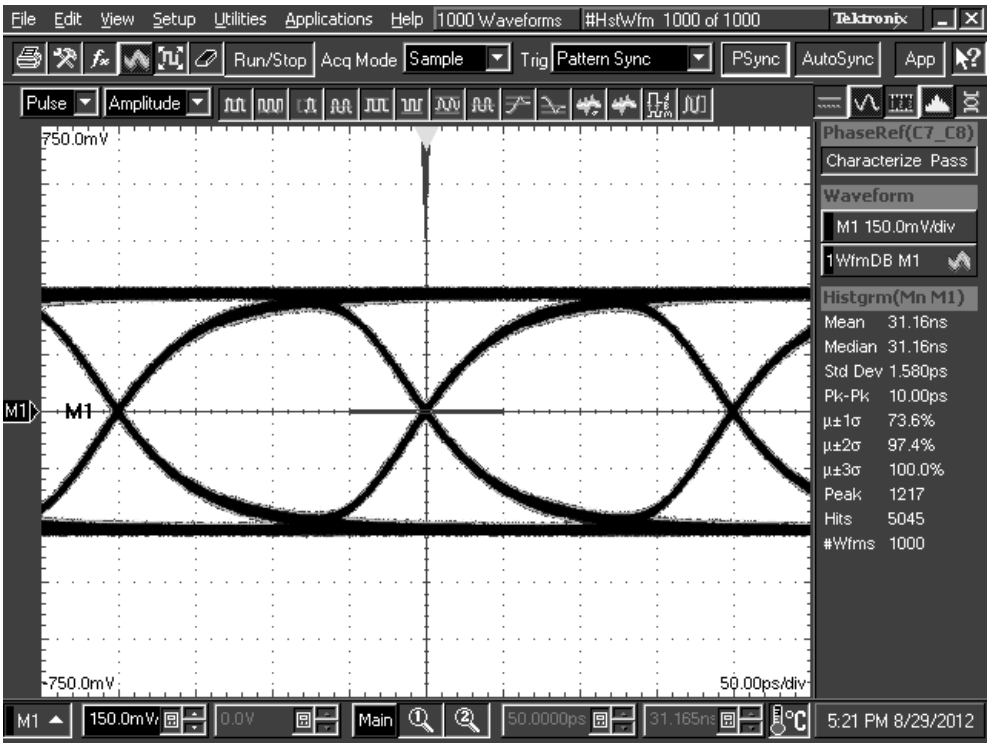


Figure 23. TL1 = 20 inch 5–mil FR4 trace, TL2 = 10 inch 5–mil FR4 trace, 5 Gbps DS125MB203 settings: EQ[1:0] = 0, 1 = 03'h, DEM[1:0] = R, 0

Typical Performance Eye Diagrams Characteristics (continued)

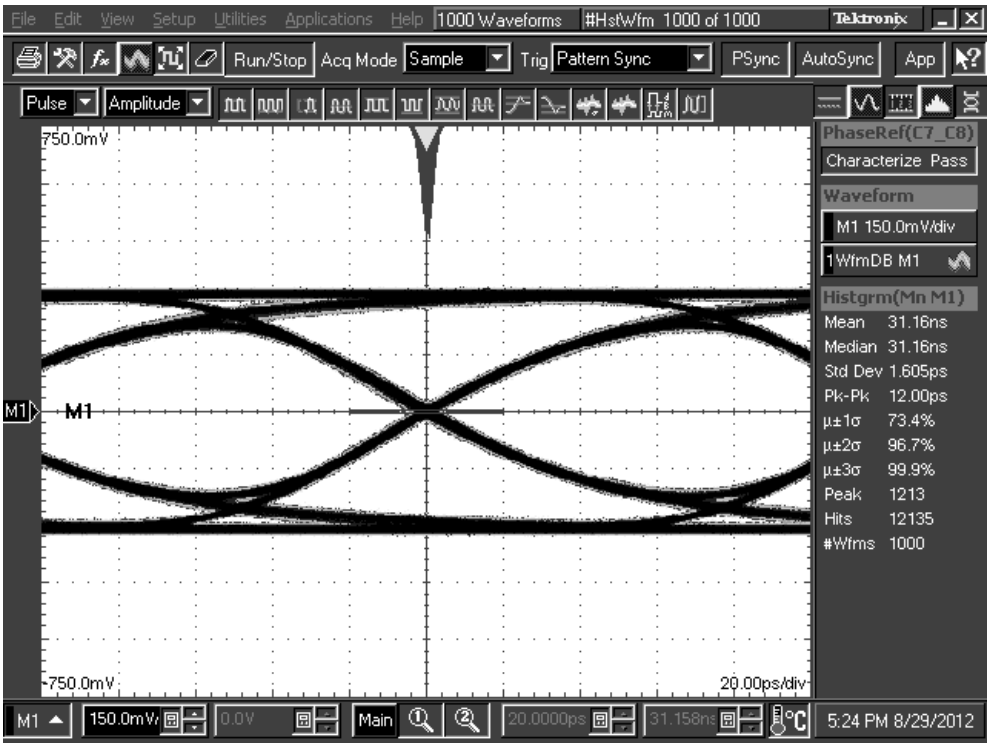


Figure 24. TL1 = 20 inch 5–mil FR4 trace, TL2 = 10 inch 5–mil FR4 trace, 8 Gbps DS125MB203 settings: EQ[1:0] = R, 1 = 03'h, DEM[1:0] = R, 0

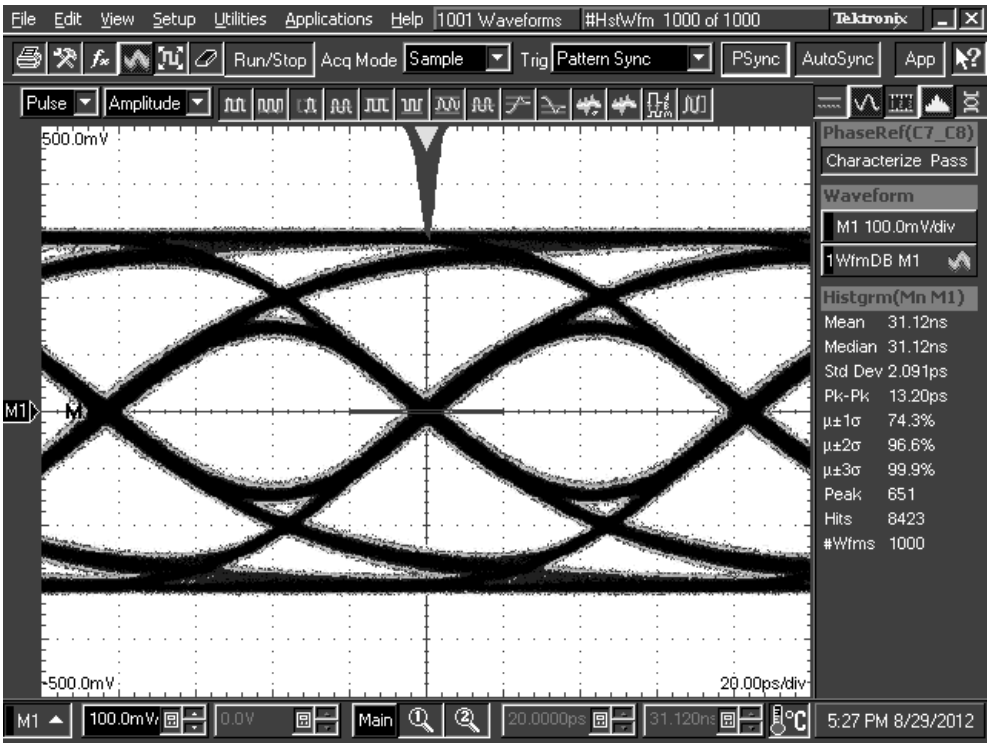


Figure 25. TL1 = 20 inch 5–mil FR4 trace, TL2 = 10 inch 5-mil FR4 trace, 12 Gbps DS125MB203 settings: EQ[1:0] = R, 1 = 03'h, DEM[1:0] = R, 0

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	40

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS125MB203SQ/NOPB	ACTIVE	WQFN	NJY	54	2000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS125MB203	Samples
DS125MB203SQE/NOPB	ACTIVE	WQFN	NJY	54	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS125MB203	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

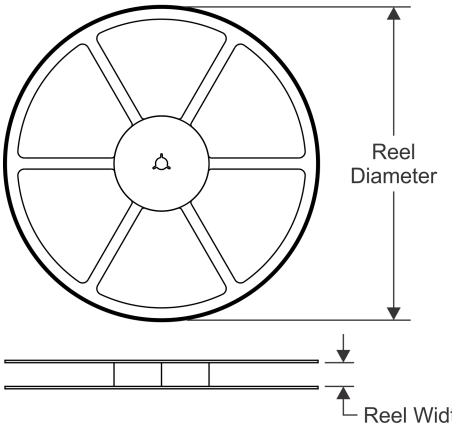
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

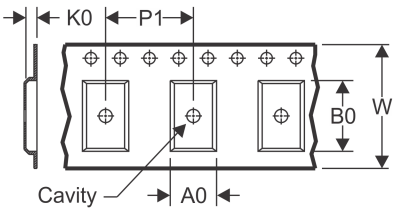
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

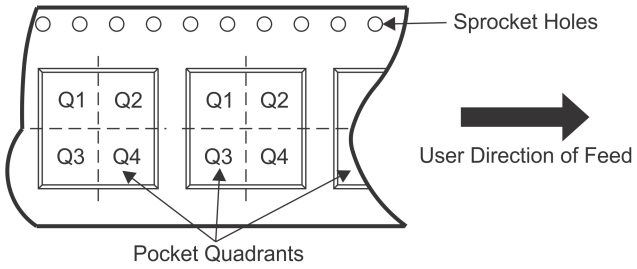


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

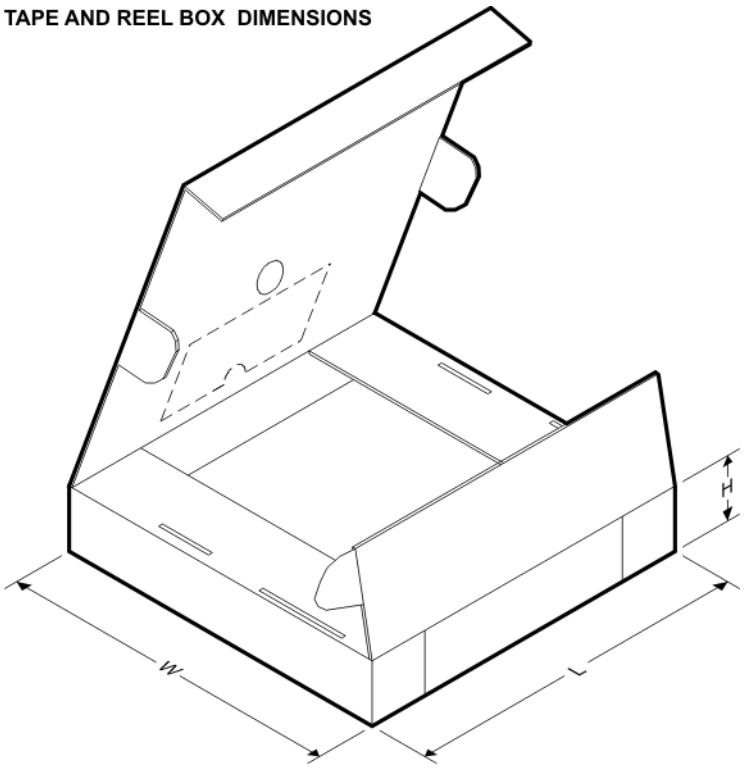
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

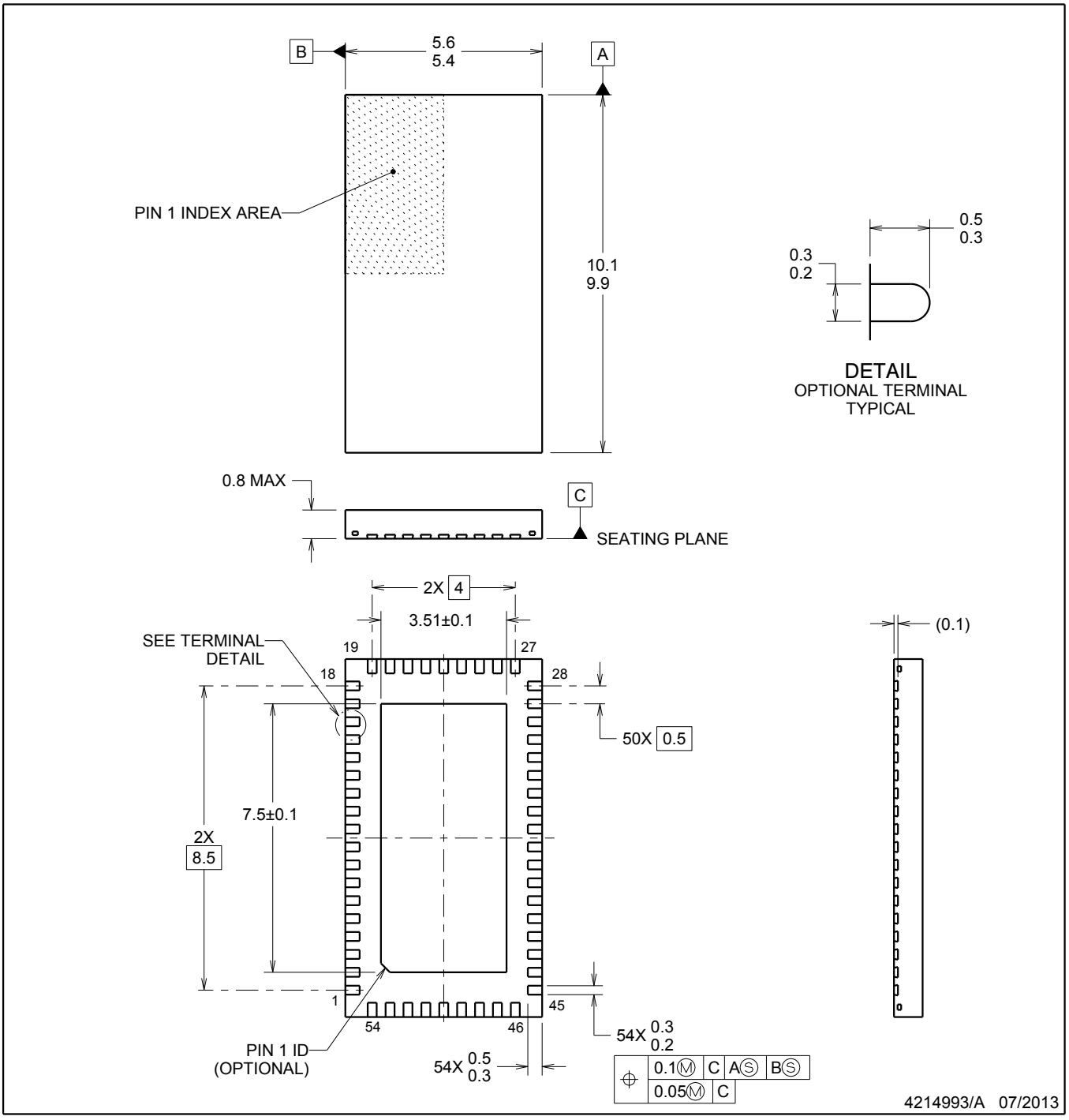
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS125MB203SQ/NOPB	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS125MB203SQE/NOPB	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



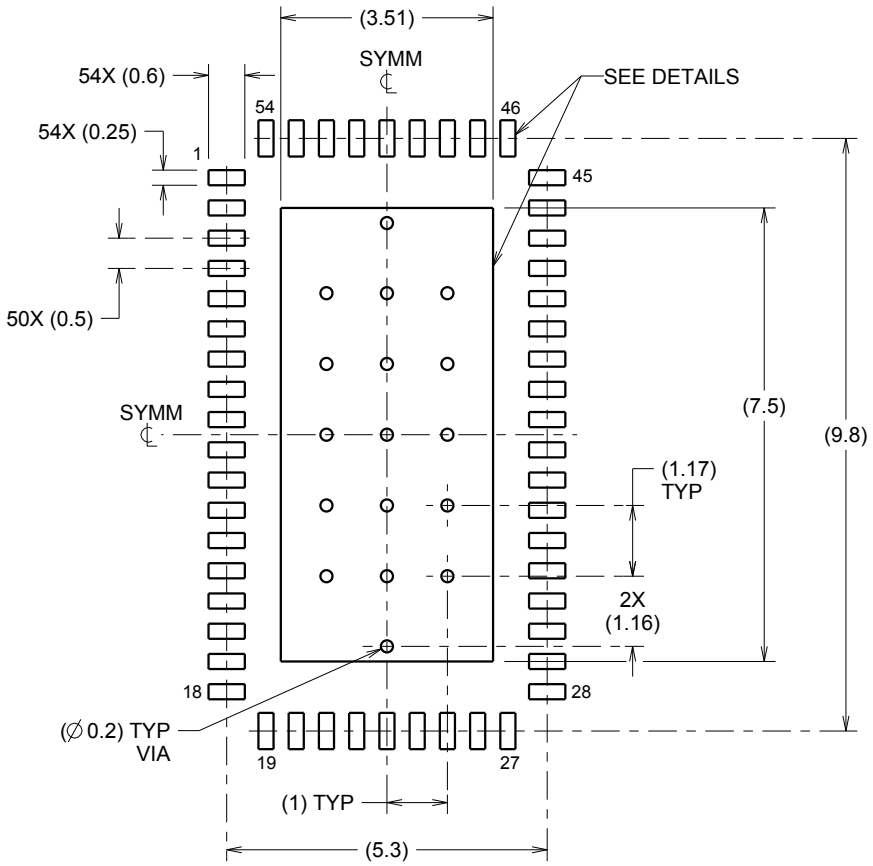
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS125MB203SQ/NOPB	WQFN	NJY	54	2000	367.0	367.0	38.0
DS125MB203SQE/NOPB	WQFN	NJY	54	250	213.0	191.0	55.0

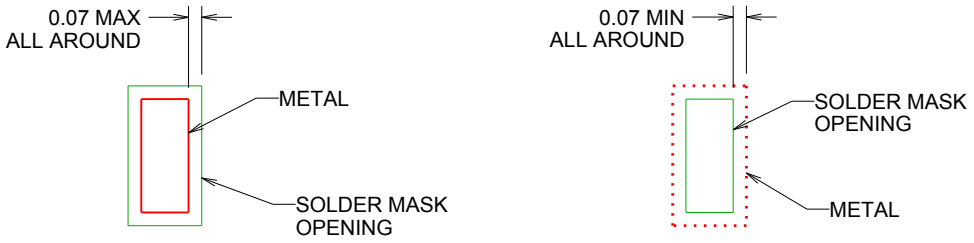


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

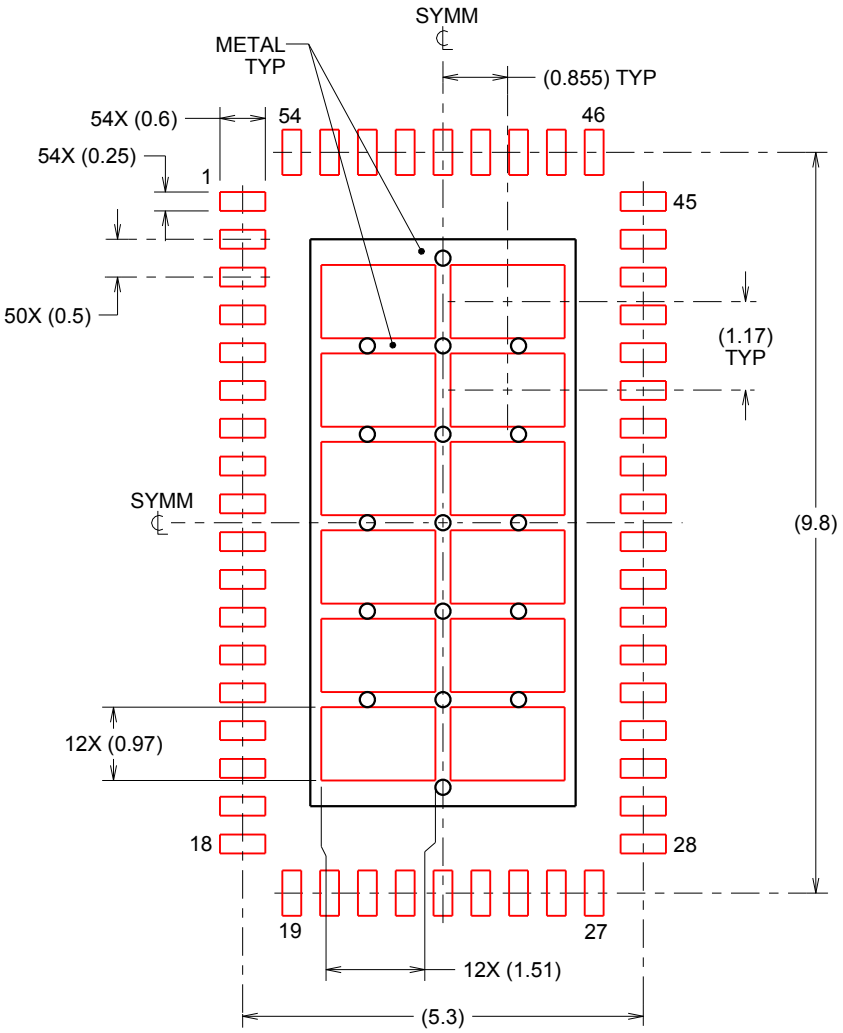
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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