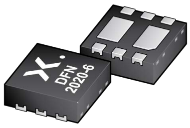


PMDPB85UPE

20 V dual P-channel Trench MOSFET

Rev. 1 — 20 June 2012 | Product data sheet

1. Product profile

1.1 General description

Dual small-signal P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- 2 kV ElectroStatic Discharge (ESD) protection

1.3 Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

1.4 Quick reference data

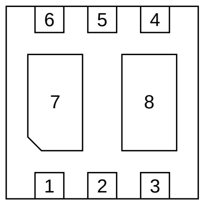
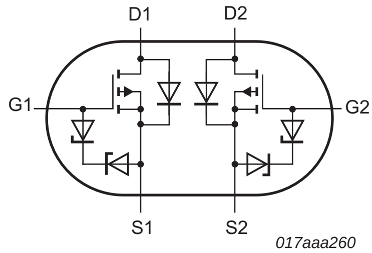
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-	-3.7	A
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -1.3 A; T_j = 25 °C		-	82	103	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1		
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1	Transparent top view	017aaa260
8	D2	drain TR2	**DFN2020-6 (SOT1118)**	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB85UPE	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB85UPE	2C

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-3.7	A
		V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-2.9	A
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-1.8	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-11.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	515	mW
			[1]	-	1170	mW
		T_{sp} = 25 °C		-	8330	mW
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-1.2	A

Table 5. Limiting values *...continued*

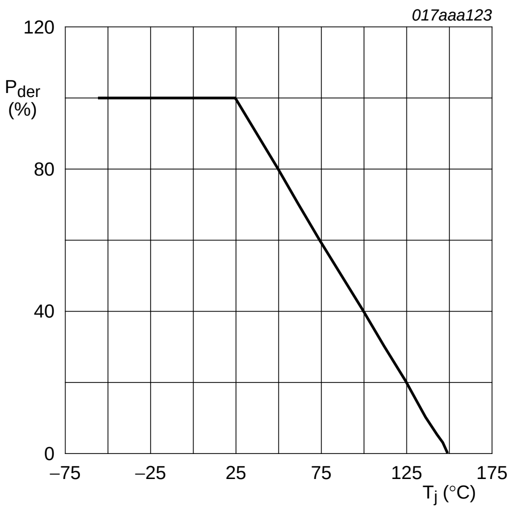
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	[3]	-	2000	V
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

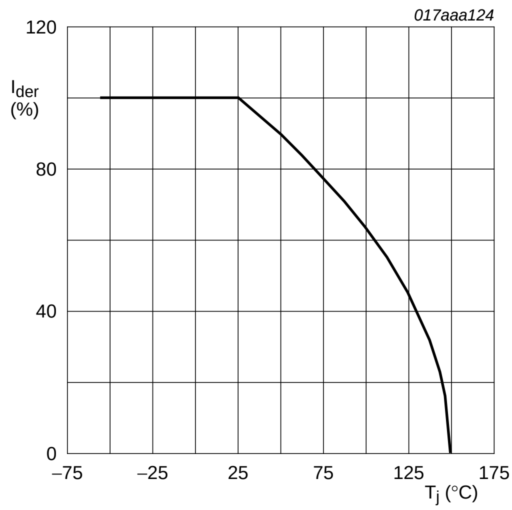
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



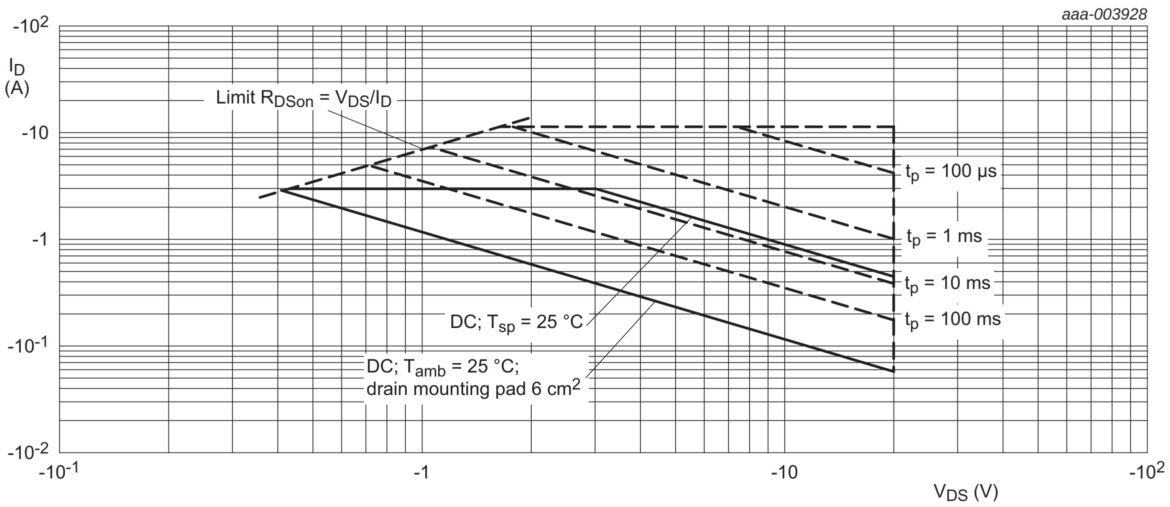
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

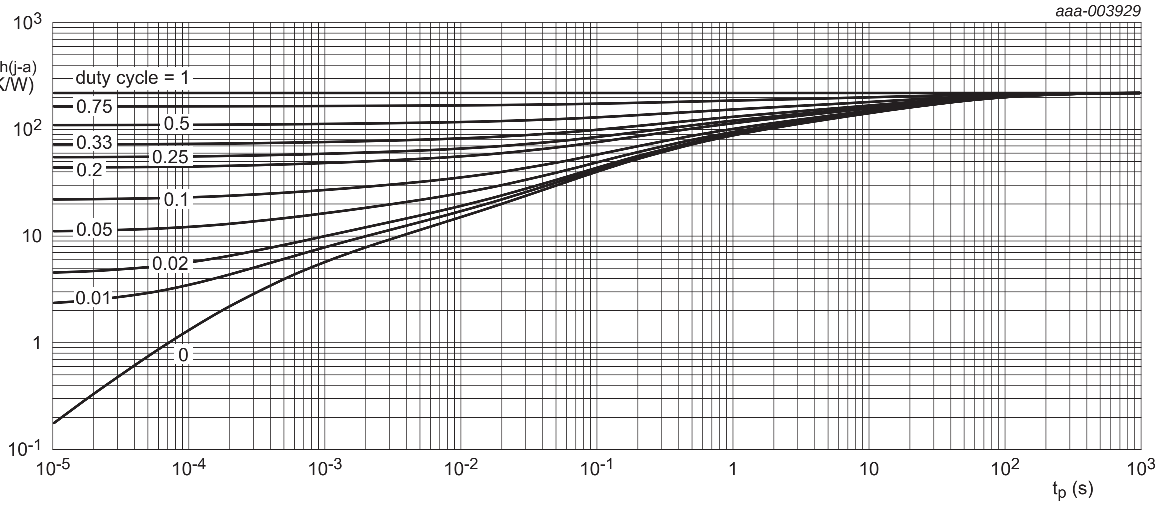
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	211	243	K/W
			[2]	-	93	107	K/W
		in free air; t ≤ 5 s	[2]	-	55	64	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	12	15	K/W

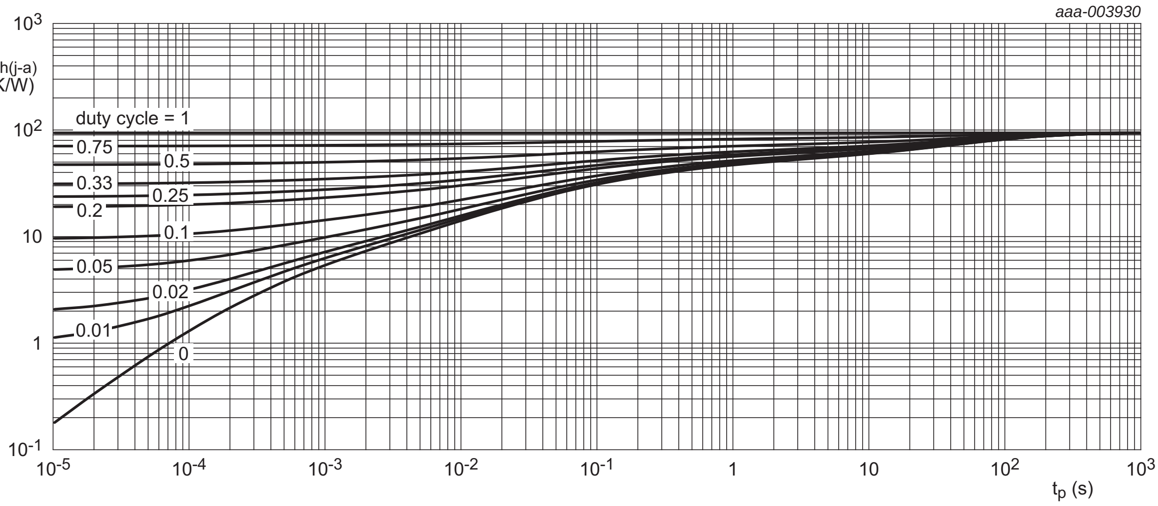
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



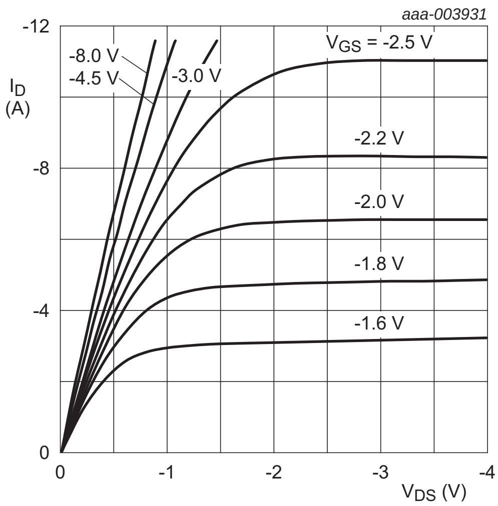
FR4 PCB, mounting pad for drain 6 cm^2

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

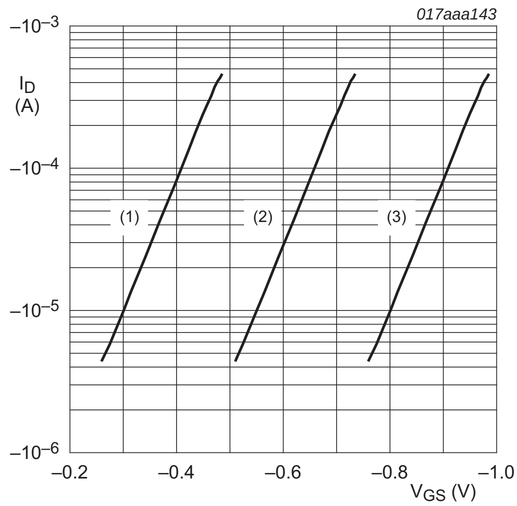
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C	-20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C	-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	µA
		V_{DS} = -20 V; V_{GS} = 0 V; T_j = 150 °C	-	-	-10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	10	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-10	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -1.3 A; T_j = 25 °C	-	82	103	mΩ
		V_{GS} = -4.5 V; I_D = -1.3 A; T_j = 150 °C	-	114	144	mΩ
		V_{GS} = -2.5 V; I_D = -1.1 A; T_j = 25 °C	-	107	146	mΩ
		V_{GS} = -1.8 V; I_D = -0.8 A; T_j = 25 °C	-	142	210	mΩ
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -1.3 A; T_j = 25 °C	-	6	-	S
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	V_{DS} = -10 V; I_D = -1.3 A; V_{GS} = -4.5 V; T_j = 25 °C	-	5.4	8.1	nC
Q_{GS}	gate-source charge		-	0.7	-	nC
Q_{GD}	gate-drain charge		-	1	-	nC
C_{iss}	input capacitance	V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	514	-	pF
C_{oss}	output capacitance		-	78	-	pF
C_{rss}	reverse transfer capacitance		-	59	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -10 V; I_D = -1.3 A; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	6	-	ns
t_r	rise time		-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	47	-	ns
t_f	fall time		-	21	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	I_S = -0.3 A; V_{GS} = 0 V; T_j = 25 °C	-	-0.7	-1.2	V



T_j = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



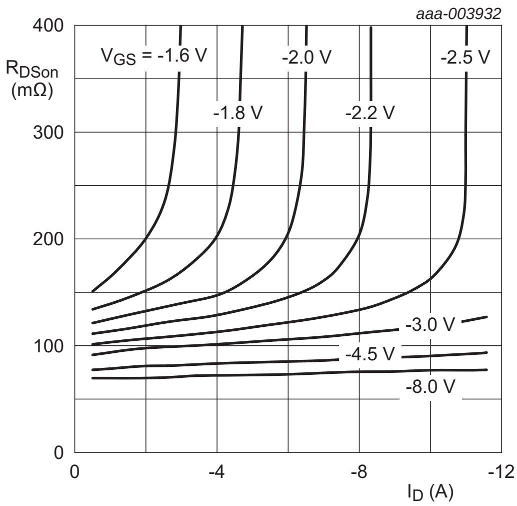
T_j = 25 °C; V_{DS} = -3 V

(1) minimum values

(2) typical values

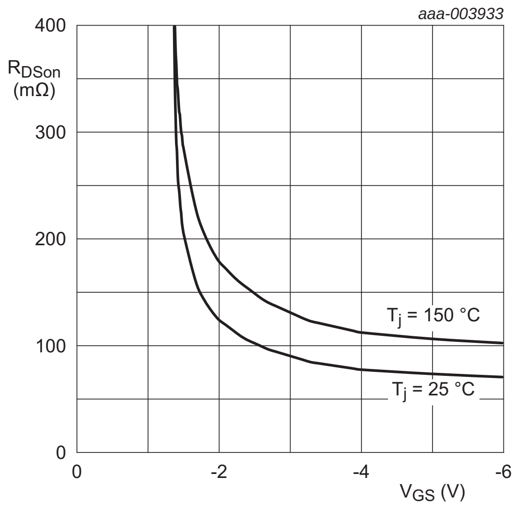
(3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage



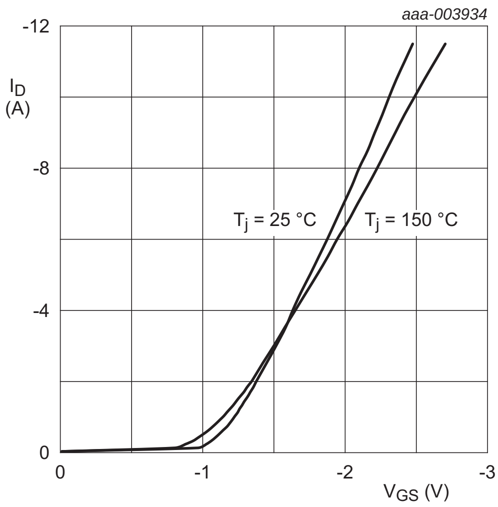
T_j = 25 °C

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



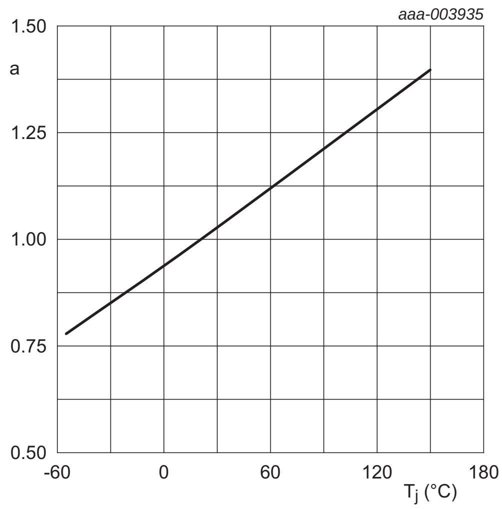
I_D = -1.3 A

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



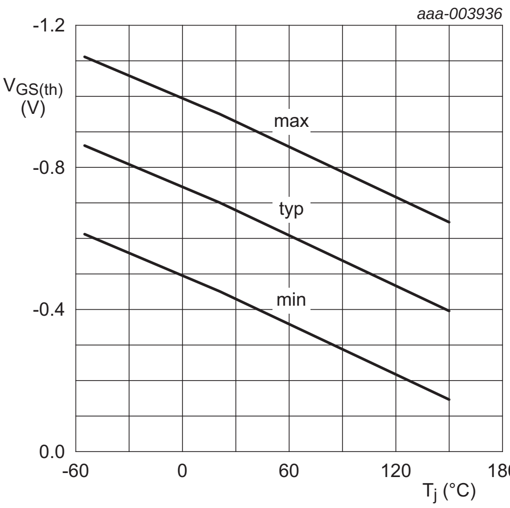
$V_{DS} > I_D \times R_{DSon}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



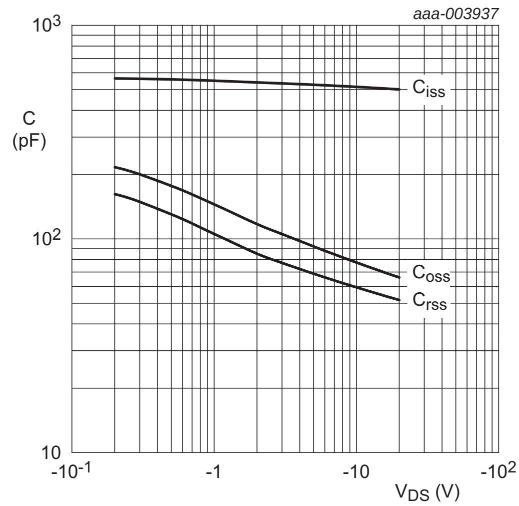
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



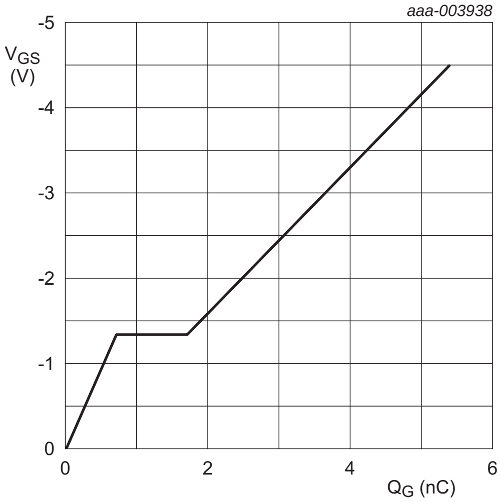
I_D = -0.25 mA; $V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -1.3 A; V_{DS} = -10 V; T_{amb} = 25 °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

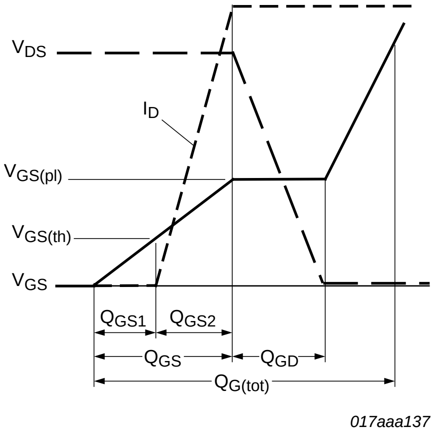
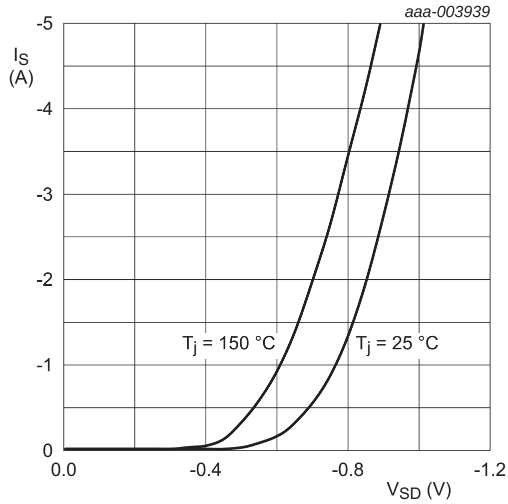


Fig 15. Gate charge waveform definitions



V_{GS} = 0 V

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

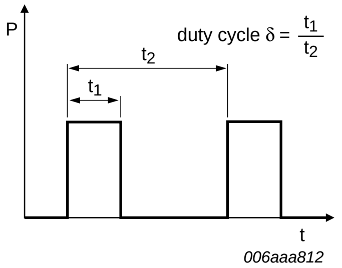


Fig 17. Duty cycle definition

9. Package outline

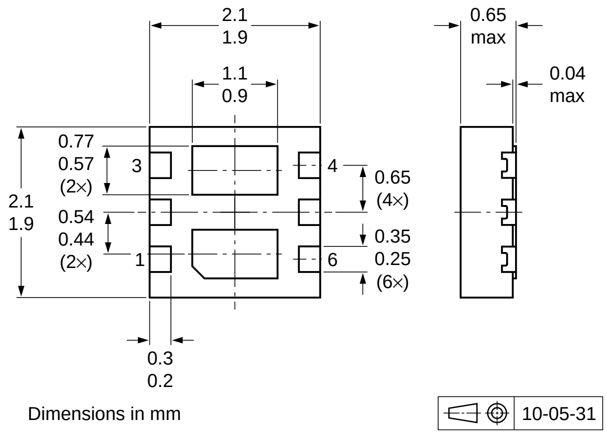


Fig 18. Package outline DFN2020-6 (SOT1118)

10. Soldering

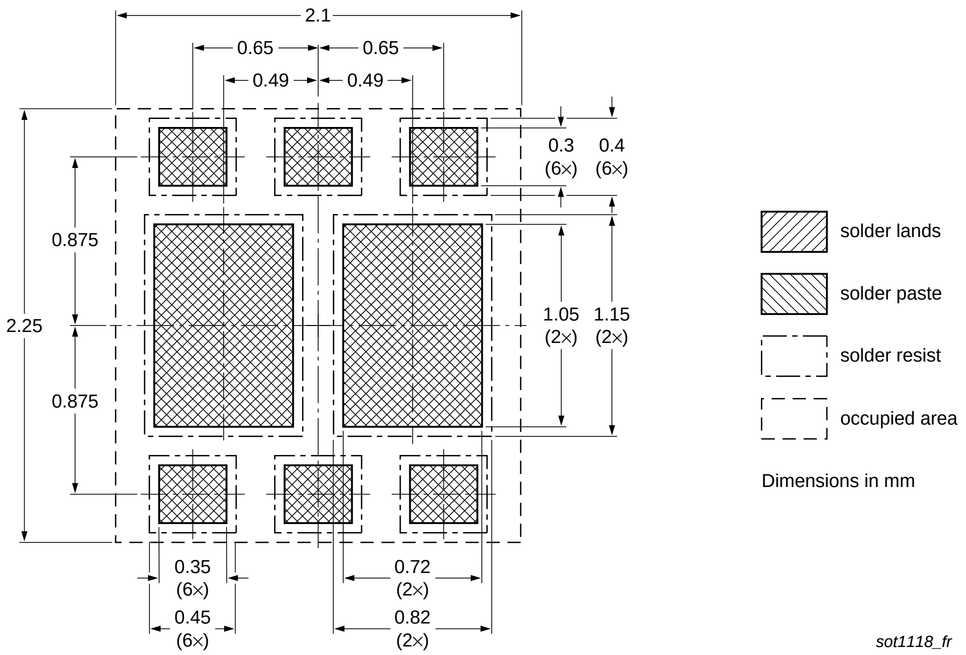


Fig 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB85UPE v.1	20120620	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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14. Contents

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Date of release: 20 June 2012