International
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REFERENCE DESIGN

IRAUDAMP9

1.7 kW / 2-Ω Single Channel Class D Audio Power Amplifier Using the IRS2092S and IRFB4227

By

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CAUTION:

International Rectifier recommends the following guidelines for safe operation and handling of IRAUDAMP9 demo board:

- **Always wear safety glasses when operating demo board**
- **Avoid physical contact with exposed metal surfaces when operating the demo board**
- **Turn off demo board when placing or removing measurement probes**

TABLE OF CONTENTS

PAGE

Introduction

The IRAUDAMP9 reference design is a single-channel 1.7-kW (@ 2Ω load) half-bridge Class D audio power amplifier. This reference design demonstrates how to use the IRS2092S Class D audio controller and external gate buffer, to implement protection circuits, and design an optimum PCB layout using the IRFB4227 (x 2 Pairs) TO-220 MOSFETs. This reference design may require additional heatsink or fan for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies for ease of use. The 1-channel design is capable of delivering higher than its rated power with provision of larger heat sink (Rth <2° C / W).

Applications

- Pro-Audio amplifiers
- Powered speakers
- Active Sub-woofers
- P.A. Systems
- Car audio amplifier
- Musical Instrument Amplifier

Features

Output Power:	1.7 kW Single channel (2 Ω load, 1kHz, THD+N=10%),
Residual Noise:	290μV, IHF-A weighted, AES-17 filter
Distortion:	0.07% THD+N @ 600W, 2Ω
Efficiency:	97% @ 1.7 kW, 2Ω
Multiple Protection Features:	Output Over-current protection (OCP), high side and low side Input Over-voltage protection (OVP), Input Under-voltage protection (UVP), Output DC-offset protection (DCP), Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltages	±75V	
Load Impedance	2Ω	
Self-Oscillating Frequency	300kHz	No input signal, Adjustable
Gain Setting	33dB	1Vrms input yields 1-kW sinusoidal output power

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS2092S Audio Controller and Gate-Driver, IRFB4227 (x 2 Pairs) TO-220 MOSFETs	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 48V to ±80V	Bipolar power supply
Output Power CH1: (1% THD+N)	1200W	1kHz Sinewave
Output Power CH1: (10% THD+N)	1700W	1kHz Sinewave
Rated Load Impedance	2 Ω	Non-inductive Resistive load
Idling Supply Current	+67mA , -105mA	No input signal
Total Idle Power Consumption	13.2 W	No input signal
System Efficiency	97% 94% 74 %	@ +/- 75V 1.7 kW, 2Ω @ +/- 75V 1.2 kW, 2Ω @ +/- 75V 125 W (1/8 Po-rated), 2Ω

Audio Performance	Class D Output	Notes / Conditions
THD+N, @ 1W THD+N, @ 125W THD+N, @ 250W THD+N, @ 500W THD+N, @ 1250W THD+N, @ 1700W	0.024% 0.025% 0.025% 0.049% 1.0 % 10.0%	1kHz, +/-75Vbus, 2-ohm load
Dynamic Range	99.4 dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 22Hz - 20kHz AES17	290μV	Self-oscillating – 300kHz AP BW:<10Hz- 20kHz AES17 IHF-A weighted
Damping Factor	81.9	1kHz, relative to 2Ω load
Frequency Response : 20Hz-20kHz	±1dB	1W, 2Ω Load

Thermal Performance	Typical	Notes / Conditions
Idling	T_C = 56°C	No signal input, T_A=25°C, after 5 min
125W (1/8 rated power)	T_C = 104°C	Continuous @ T_A=25°C *requires larger heatsink design for continuous operation
1.2 kW	T_C = 118°C	At OTP shutdown after 130 sec, T_A=25°C

Physical Specifications

Dimensions	7.76”(L) x 5.86”(W) x 2.2”(H) 192 mm (L) x 149mm (W) x 56mm(H)
Weight	0.54kgm

Connection Setup

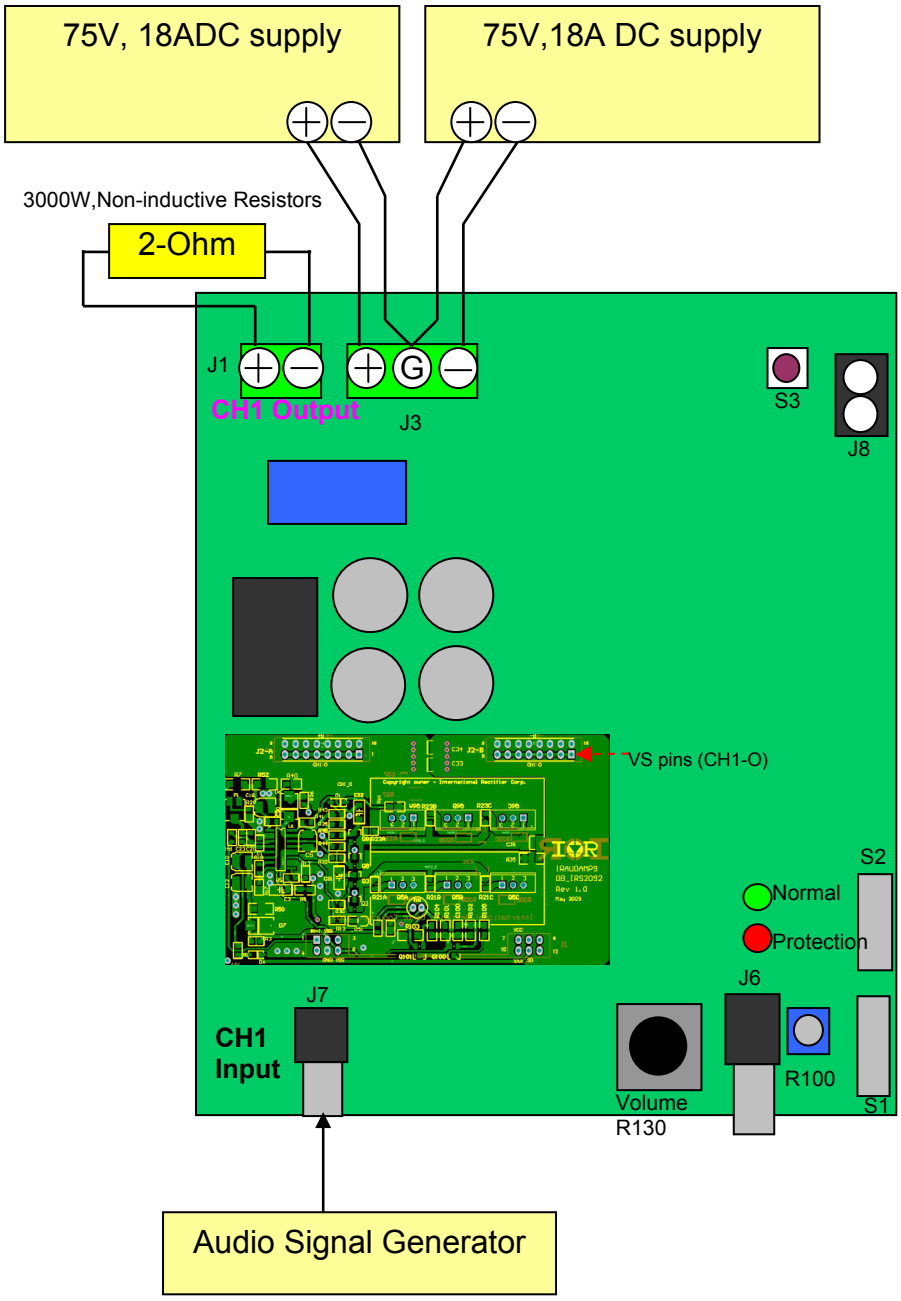


Figure 1 Typical Test Setup

Connector Description

CH1 IN	J7	Analog input for CH1
POWER	J3	Positive and negative supply (+B / -B)
CH1 OUT	J1	Output for CH1
EXT CLK	J6	External clock sync
DCP OUT	J8	DC protection relay output

Test Procedures

Test Setup:

1. Connect 2Ω - 3000 W dummy loads to the output connectors (J1 as shown on Figure 1).
2. Connect the Audio Precision Analyzer (AP) signal Generator output to J7.
3. Initially set the voltages of the dual power supplies to ±75V with current limits to 0.5 A.
4. Make sure to TURN OFF the dual power supplies before connecting to the unit under test (UUT).
5. Set switch S1 to middle position (self oscillating).
6. Set volume level knob R130 fully counter-clockwise (minimum volume).
7. Connect the dual power supply to J3 as shown in Figure 1.

Power up:

8. Turn ON the dual power supply. The ±B supplies must be applied and removed at the same time.
9. Red LED (Protection) should turn on almost immediately and turn off after about 3s.
10. Green LED (Normal) then turns on after the red LED is extinguished and should stay ON.
11. Note the quiescent current for the positive supply should be 67mA ±10mA at +75V.
12. Quiescent current for the negative supply should be 105mA ±15mA at –75V.
13. Push switch S3 (Trip and Reset push-button) to restart the LEDs sequence, which should be the same as noted above in steps 9 and 10.

Switching Frequency test

14. Monitor switching waveform at VS1/J4 (pins 9-12) of CH1 on Daughter Board using an oscilloscope.
15. For IRAUDAMP9, the self-oscillating switching frequency is pre-calibrated to 300 kHz. To modify the IRAUDAMP9 frequency, adjust the potentiometer P1 for CH1.

Audio Functional Tests:

16. Set the current limit of the dual power supplies to ~18A. Make sure the volume control potentiometer is turned to full counterclockwise position. Apply 1V rms @ 1 kHz from the Audio Signal Generator to the audio input connector J7.
17. Turn control volume, R130 clock-wise to obtain an output reading of 1.0 kW. For all the subsequent tests as shown on the Audio Precision graphs below, measurements are taken across J1 with an AES-17 Filter. Observe that a 1 V_{RMS} input generates an output voltage of ~44.8 V_{RMS}. Alternatively, a 100-mVrms input would give an output of ~ 10.03W that corresponds to 4.48Vrms across a 2-ohm load.
18. Using an oscilloscope monitor the output signals at J1 while sweeping the audio input signal from 10 mV_{RMS} to 2 V_{RMS}. The waveform must be a non distorted sinusoidal signal.

Test Setup using Audio Precision Analyzer (Ap):

19. Use an unbalanced-floating signal from the generator outputs.
20. Use balanced inputs taken across output terminal J1.
21. Connect Ap chasis ground to GND at terminal J7.
22. Select the AES-17 filter (pull-down menu) for all the testing except frequency response.
23. Use input signal ranging from 15 mV_{RMS} to 1 V_{RMS}.
24. Run Ap test programs for all subsequent tests as shown in Figure 2 below.

Performance and test graphs

±B Supply = ± 75V, 2 Ω Load

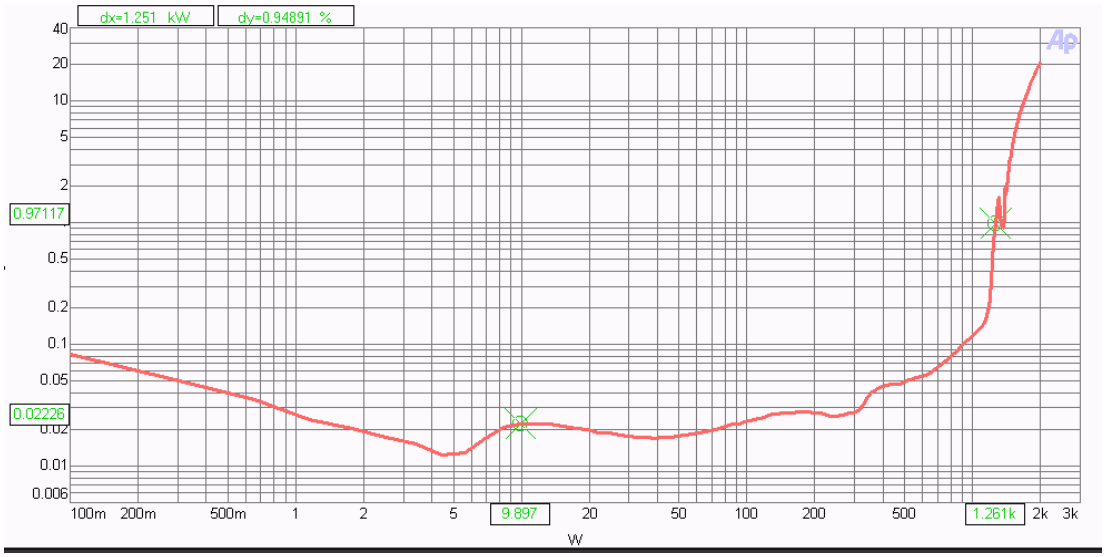


Figure 2 THD+N vs. Power

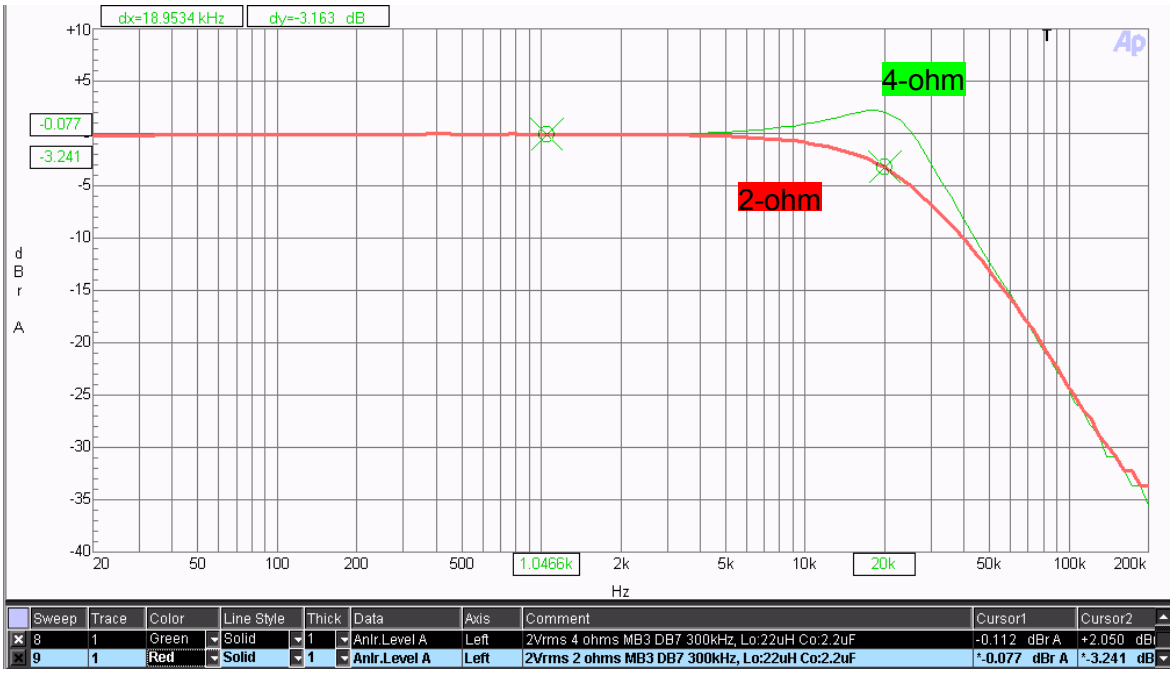


Figure 3 Frequency response

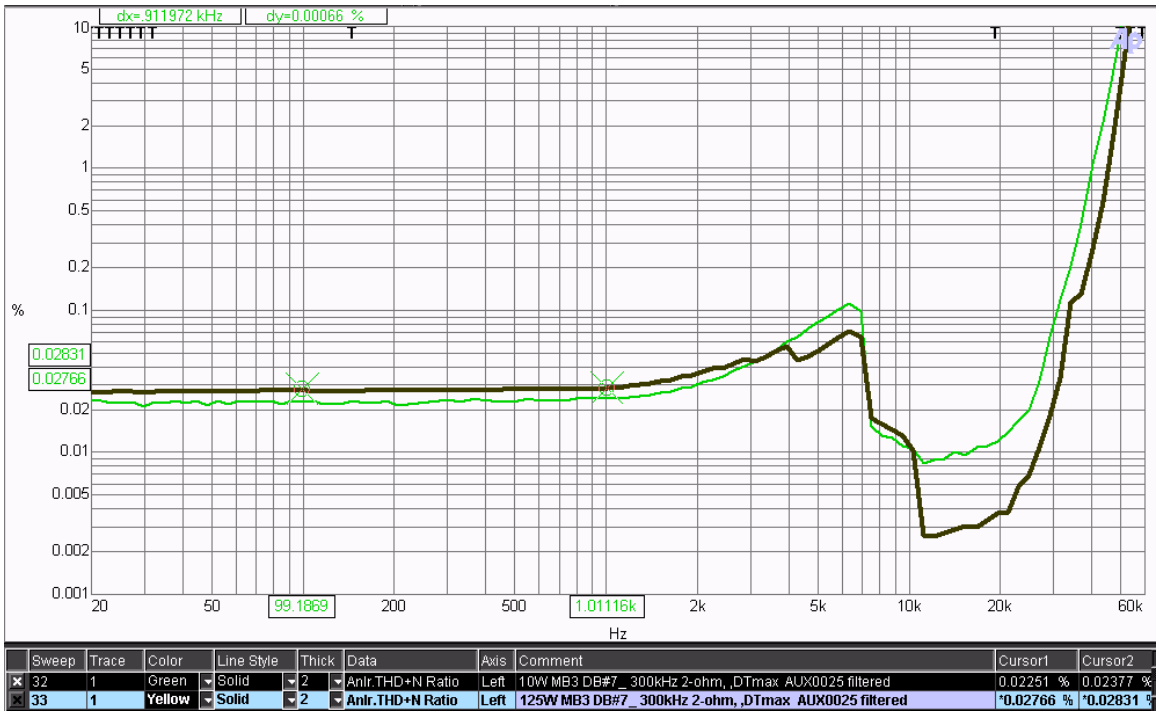
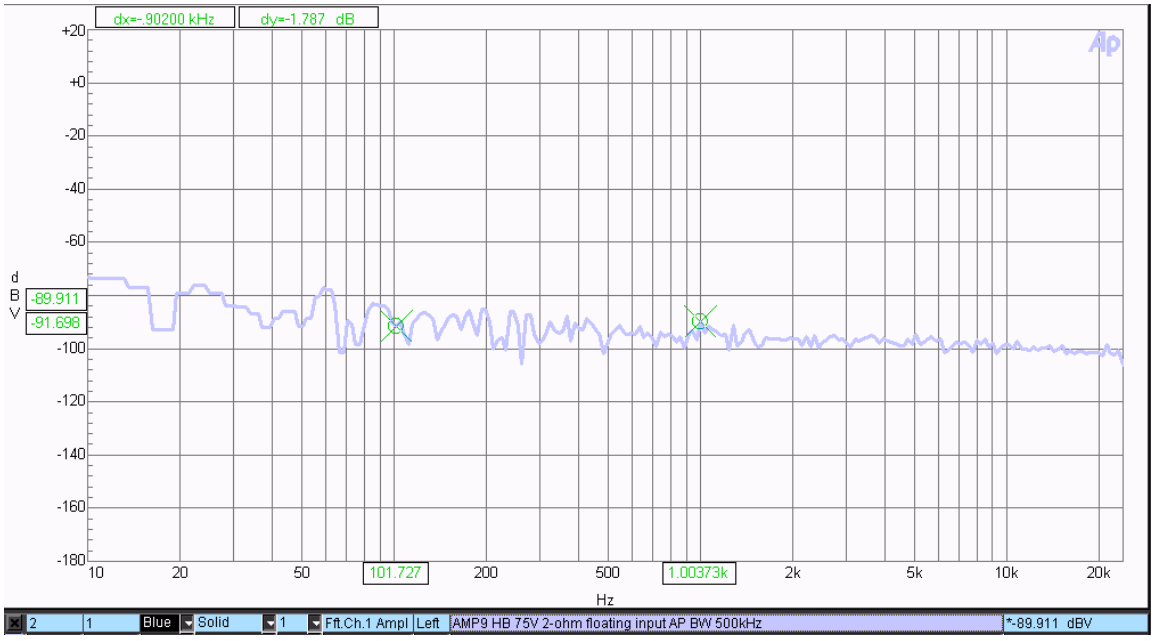


Figure 4 THD+N vs. Frequency at 10W and 125W



No signal, Self Oscillator @ 300kHz

Figure 5 Noise Floor

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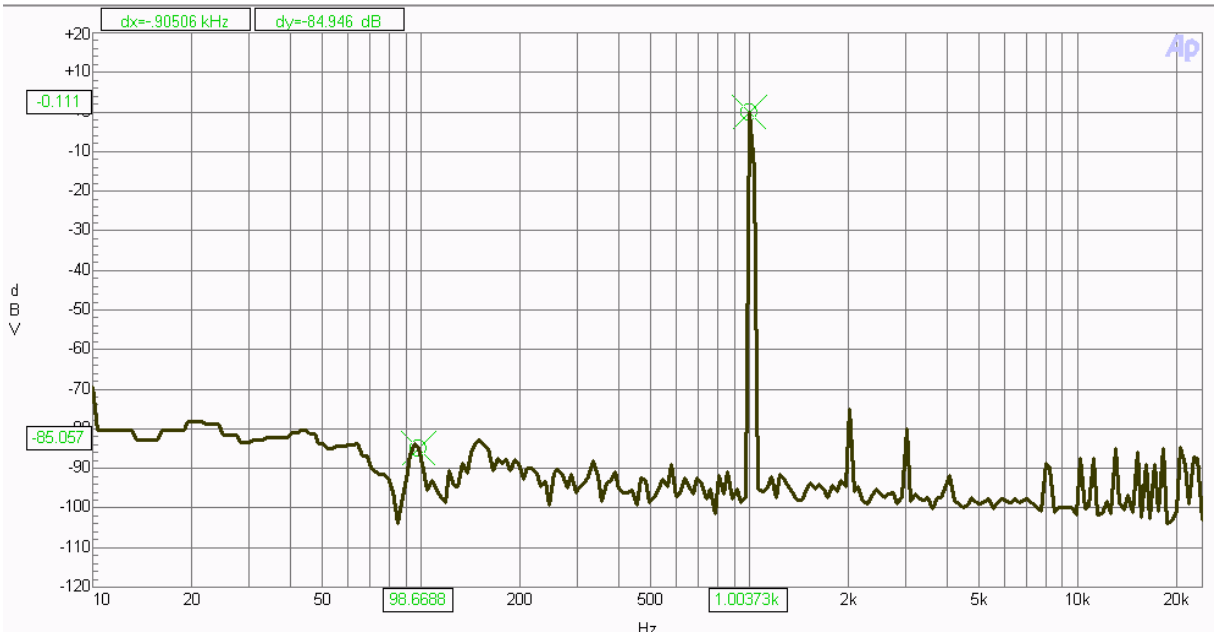

Figure 6. 1-V_{RMS} **output Frequency Spectrum**

IRAUDAMP9 Overview

The IRAUDAMP9 features a single-channel self-oscillating PWM modulator. This topology results in the lowest component count, highest performance and robust design. It represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of error correction.

The IRAUDAMP9 self-oscillating topology incorporates the following functional blocks.

- Front-end integrator
- PW Modulator and Level shifters
- Gate driver and buffer
- Power MOSFETs
- Output LPF

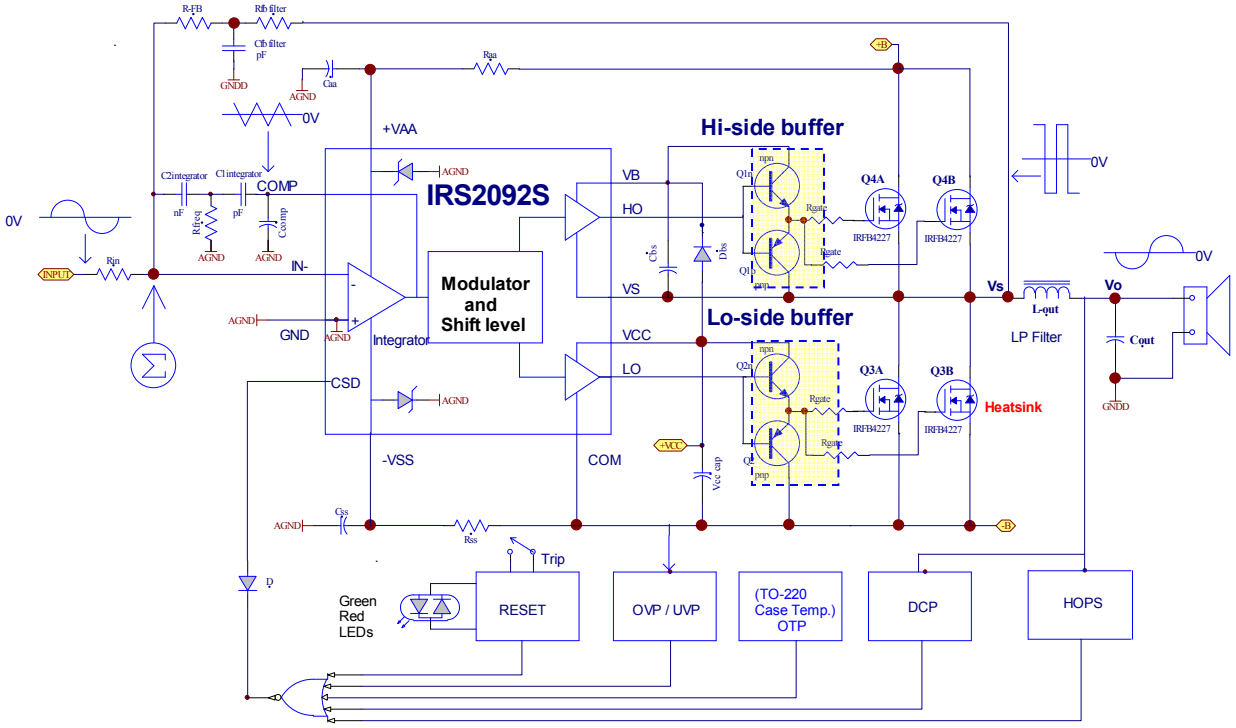

Fig. 7 Functional block diagram

Functional Description

Class-D Operation

The $C2_{integrator}$, $C_{1integrator}$, R21 + potentiometer P1 form a front-end second-order integrator. This integrator receives a rectangular feedback signal from the Class D switching stage and outputs a quadratic oscillatory waveform as a carrier signal. To create the modulated PWM signal, the input

signal shifts the average value of this quadratic waveform (through gain relationship between [(R38+R39) / (R154+R40)] ratio) so that the duty varies according to the instantaneous value of the analog input signal. The IRS2092S input comparator processes the signal to create the required PWM signal. This PWM signal is internally level-shifted down to the negative supply rail where it is split into two signals, with opposite polarity and added dead time, for high-side and low-side MOSFET gate signals, respectively. The IRS2092S drives 2 pairs of IRFB4227 TO-220 MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is re-created by demodulating the amplified PWM. This is done by means of the LC low-pass filter (LPF) formed by L4 and C34, which filters out the switching carrier signal.

Gate Driver Buffer Stage

High power designs such as IRAUDAMP9 that use multiple mosfets in parallel connection to handle large amount of switching current often require far more than +/-1A drive current even for a brief moment due to mosfets' gate drive requirement (high total gate charge, Qg). In order to facilitate this high drive current, a buffer stage is devised to source and sink this high gate charge. This stage consists of NPN-PNP BJT transistors in totem pole configuration. It serves as a high-speed buffer amplifier that receives input from IRS2092S HO / LO to drive the power mosfet stage through Rg (1A,1B,2A,2B) for low side mosfets Q4(A,B) and for high-side Q3 (A,B) mosfets. Theoretically, the switching time is reduced by such amount (hfe) as compared to that high-Qg design that uses the divided output current capacity of the driver IC. This buffering action is very necessary to speed-up the switching times of each mosfets in order not to exceed the OCP voltage monitor time. The IC commences drain-to-source voltage monitoring as soon as the HO / LO go to high state but after the leading edge blanking time.

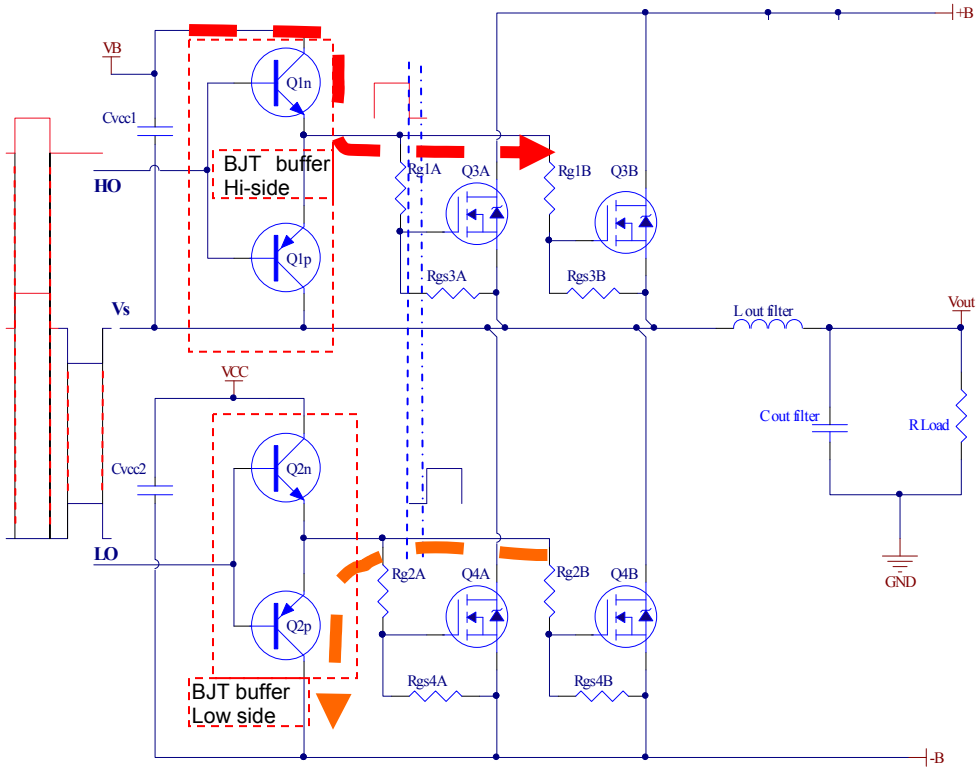

Fig. 8 Simplified diagram for gate-buffering of 2 x IRFB4227 mosfets

Power Supplies

The IRAUDAMP9 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from ±38 V to ±82 V (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a ±5 V supply for analog signal processing (preamp, etc.), and a +12 V supply (Vcc), referenced to –B, to supply the Class D gate-driver stage.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but not always necessary. The bus capacitors, C45 ~ C48 on the motherboard, along with high-frequency bypass-capacitors C19 ~ C26 on daughter board, address the high-frequency ripple current that result from switching action. In designs involving unregulated power supplies, the designer should place a set of bus capacitors, having enough capacitance to handle the audio-ripple current, externally. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP9 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP9 is excellent as shown in Figure 9 below.

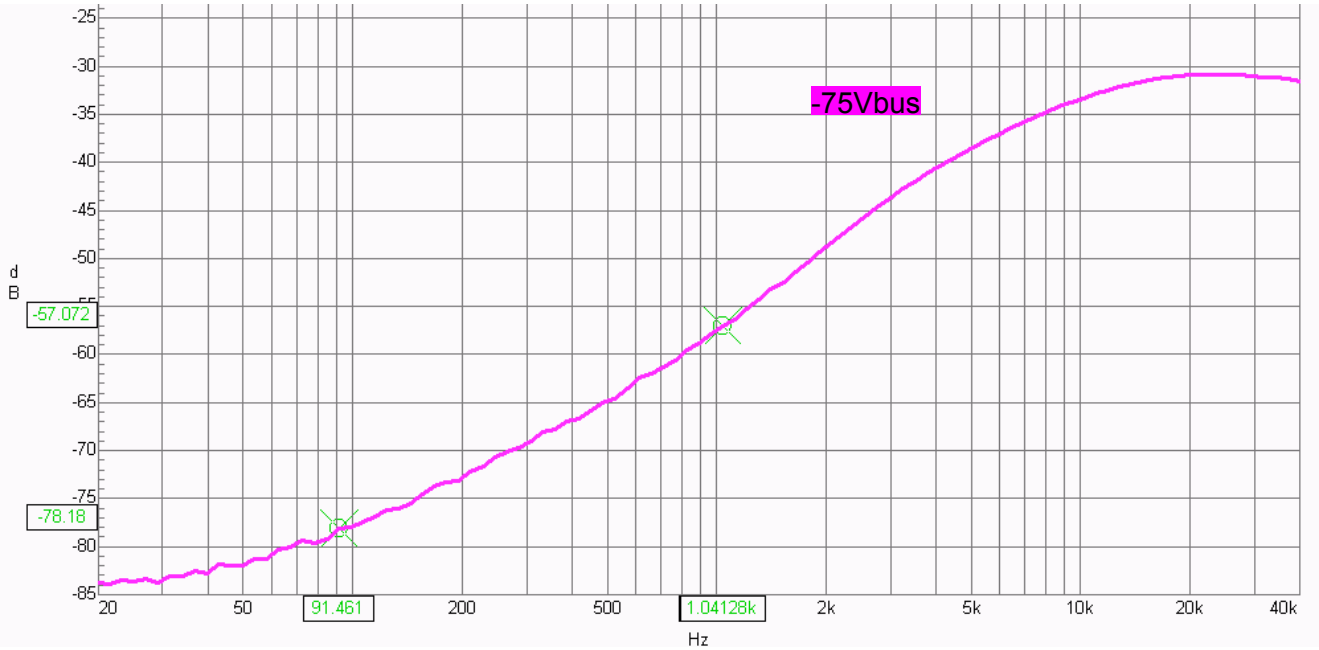

Fig. 9 IRAUDAMP9 Power Supply Rejection Ratio (PSRR)

Bus Pumping

Since the IRAUDAMP9 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.

The following conditions worsen bus pumping:

- Lower frequencies (bus-pumping duration is longer per half cycle)
- Higher power output voltage and/or lower load impedance (more energy transfers between supplies)
- Smaller bus capacitors (the same energy will cause a larger voltage increase)

The IRAUDAMP9 has protection features that will shutdown the switching operation if the bus voltage becomes too high (>82 V) or too low (<38 V). One brute countermeasure is to put a large electrolytic-capacitors between the power supply and the input terminals. Bus voltage detection is only done on the –B supply as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase).

House Keeping Power Supplies

The internally-generated power supplies include ±5V for analog signal processing, and +12V supply (Vcc) referred to the negative supply rail -B for TO-220 gate drive. The gate driver section of the IRS2092S uses Vcc to drive gates of the TO-220s. Vcc is referenced to –B (negative power supply). The D6, R26 and C5 form a bootstrap floating supply for the HO gate driver.

Input

Input signal is an analog signal ranging from 20Hz to 20kHz with up to 2 V_{RMS} amplitude with a source impedance of no more than 600 Ω. Input signal with frequencies around 20kHz may cause LC resonance in the output LPF and may result to a large reactive current flow through the switching stage, especially if the amplifier is not connected to any load - this can activate OC protection.

Output

The IRAUDAMP9 has single output and therefore have terminals labeled (+) and (-) with the (-) terminal connected to power ground. Each channel is optimized for a 2 Ω speaker load for a rated output power of 1200 W @ 1% THD+N.

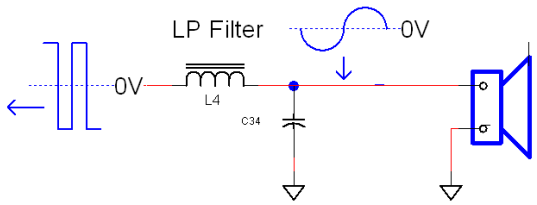

Figure 10 Output Low Pass Filter

High Output Peak Shutdown (HOPS) circuit

It is common in amplifier design to have a RC snubber called Zobel network that is used to damp the resonance and prevent peaking frequency response with high load impedance. Instead, the IRAUDAMP9 has a simple detection circuit in placed, which consist of a NPN transistor, blocking diode and a current limiting resistor to detect the output peak status from exceeding –B supply during resonance of the output LC filter. This circuit pulls the Cstart capacitor (C66) down to output (+) that sends a signal to IRS2092S to inhibit the power stage from switching. As the output returns to unclipped level, the base-to-emitter voltage is reduced and releases the CSD cap to start charging. This would allow the IRS2092S to resume driving operation of the power stage.

The HOPS function is not expected to be triggered in normal operating conditions. It is use to halt the output going too negative (< -B rail) during the natural resonance of output LC filter. The HOPS circuit is intended for higher than nominal impedance or open load conditions.

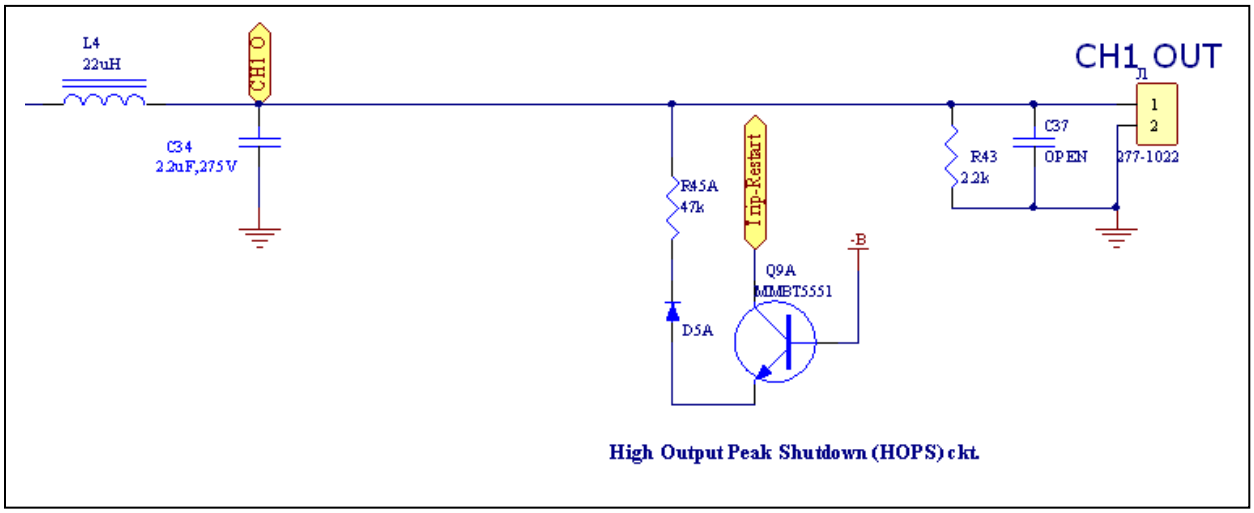

Fig. 11 Shutdown circuit diagram when output goes lower than negative rail.

Gain Setting / Volume Control

The IRAUDAMP9 has an internal volume control (potentiometer R130 labeled, “VOLUME”) for gain adjustment. Gain setting is tracked and controlled by the volume control IC (U_2) setting the gain from the microcontroller IC (U_3). The total gain is a product of the power-stage gain, which is constant (+33 dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100 dB with minimum volume setting to mute the system with an overall gain of less than -60 dB. For best performance in testing, the internal volume control should be set to 1 Vrms which results in rated output power (1 kW into 2 Ω).

Efficiency

Figure 12 shows efficiency characteristics of the IRAUDAMP9. The high efficiency is achieved by the following major factors:

1) Low conduction loss due to the low $R_{DS(ON)}$ of the IRFB4227 mosfets
2) Low switching loss due to the high gate drive output for fast rise and fall times
3) Secure dead-time provided by the IRS2092S, avoiding cross-conduction

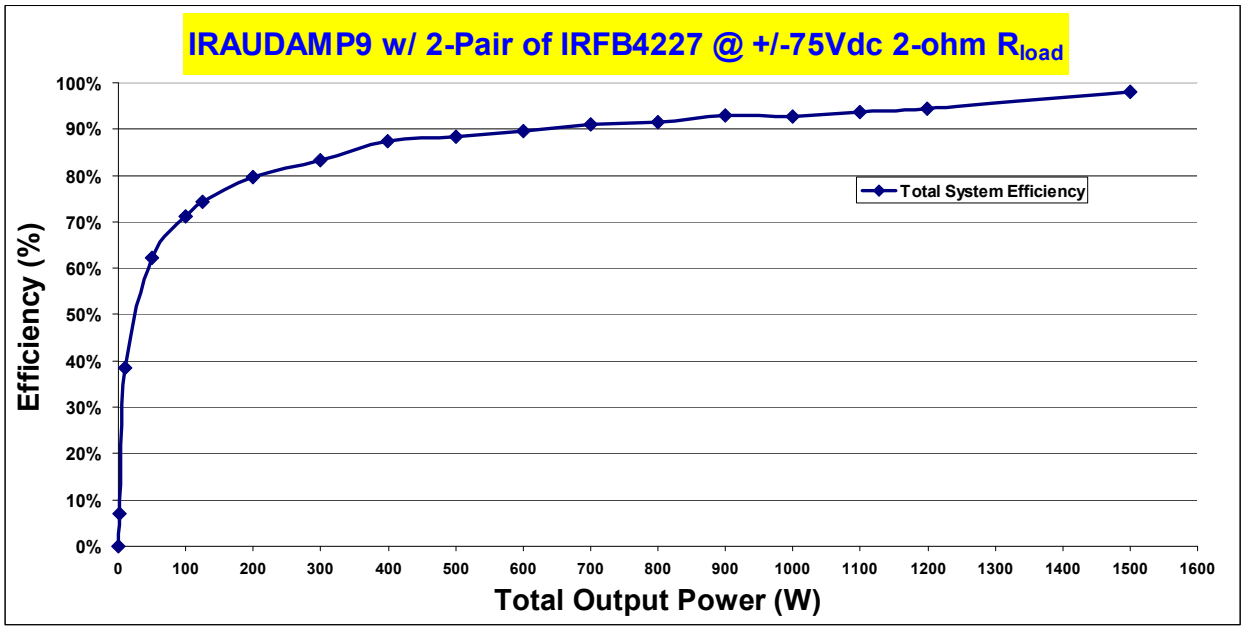

Fig.12 Efficiency plots.

Output Filter and Preamplifier

Output filter:

The amplified PWM output is reconstructed back to an analog signal by the output LC LPF.
This LPF is formed by L4 and C34, provides pass band for the audio frequencies while filtering out the switching carrier signal. A single stage output filter can be used with switching frequencies of around 300 kHz ; a design with a lower switching frequency may require an additional stage of filtering.

Since the output filter is not included in the control loop of the IRAUDAMP9, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to select filter components with the following characteristics in mind.

1) The DC resistance of the inductor should be minimized to 6 mΩ or less.
2) The linearity of the output inductor and capacitor should be high with respect to load current and voltage.

Preamplifier

The preamp allows partial gain of the input signal. It is possible to evaluate the performance without the preamp and volume control, by removing R154 and feeding the input signal directly through R46 resistors (IN-1). This effectively bypasses the preamp and connects the RCA inputs directly to the Class D power stage input. Improving the preamp noise performance and the output filter, will improve the overall system performance approaching that of the stand-alone Class D power stage.

Self-Oscillating PWM Modulator

The IRAUDAMP9 features a self-oscillating type PWM modulator for the lowest component count and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, propagation delay of IRS2092S gate-driver, delay caused by the external buffer, IRFB4227 (x 2 pairs) switching speed, time-constant of front-end integrator and variations in the supply voltages are critical factors of the self-oscillating frequency. Under normal conditions, the switching-frequency is around 300 kHz with no audio input signal and a +/-75 V supply.

Adjustments of Self-Oscillating Frequency

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies, distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. Most importantly, higher switching frequency results in higher switching loss of the power stage, hence the thermal performance degrades, especially with those that having a limited-size heatsink design.

Potentiometers for adjusting self-oscillating frequency
P1 potentiometer + R21 Switching frequency for CH1*
*Adjustments have to be done in idle condition with no input signal.

Switches and Indicators

There are two different indicators on the reference design:

- A red LED, signifying a fault / shutdown condition when lit.
- A green LED on the motherboard, signifying conditions are normal and no fault condition is present.

There are three switches on the reference design:

Switch S1 is an oscillator selector. This three-position switch is selectable for internal self-oscillator (middle position – “SELF”), or either internal (“INT”) or external (“EXT”) clock synchronization.

– Switch S3 is a trip and reset push-button. Pushing this button has the same effect of a fault condition. The circuit will restart about three seconds after the shutdown button is released.

Startup and Shutdown

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise on the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier. It is interesting to note that the audible noise of the relay opening and closing is not considered "click noise", although in some cases, it can be louder than the click noise of non-relay-based solutions.

The IRAUDAMP9 does not use any series relay to disconnect the speaker from the audible transient noise, but rather depends on IRS2092S's on-chip noise reduction circuit that yields audible noise levels that are far less than those generated by the relays they replace. This results in a more reliable, superior performance system.

Startup and Shutdown Sequencing

The IRAUDAMP9 sequencing is achieved through the charging and discharging of the C_{Start} capacitor C66. This, coupled to the charging and discharging of the voltage of CSD (C10 on daughter board for CH1) of the IRS2092S, is all that is required for complete sequencing. The conceptual startup and shutdown timing diagrams are show in Figure 13.

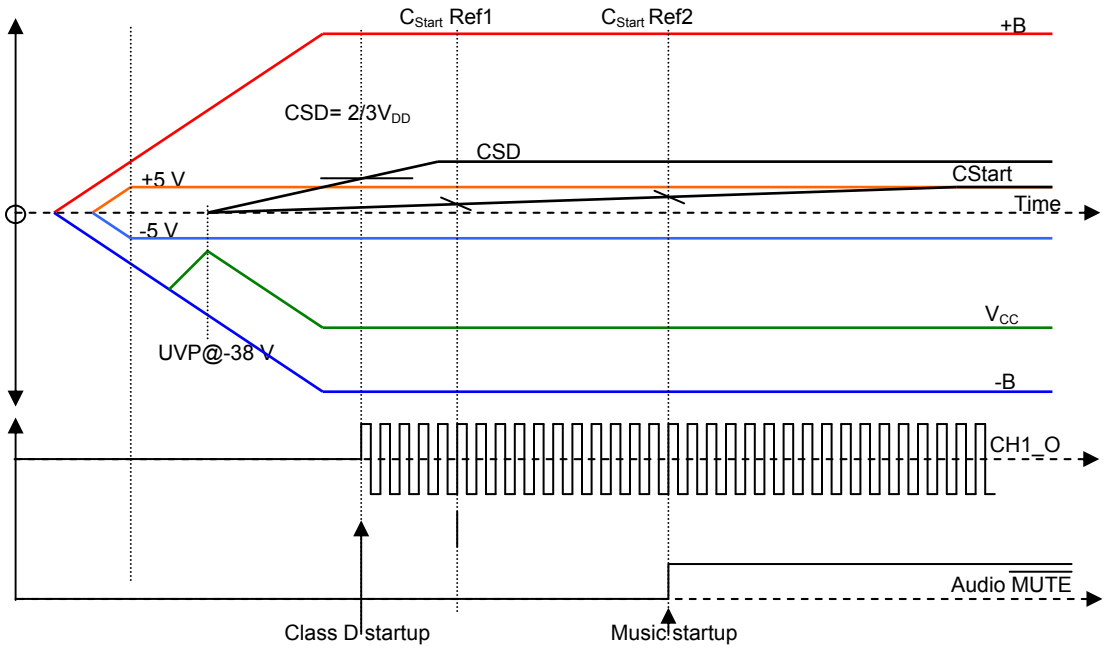

Figure 13, Conceptual Startup Sequencing of Power Supplies and Audio Section Timing

For startup sequencing, +/-B supplies startup at different intervals. As +/-B supplies reach +5 V (Vaa) and -5 V (Vss) respectively, the analog supplies (Vaa, Vss) start charging and, once +B

reaches ~16 V, Vcc charges. Once –B reaches -38 V, the UVP is released and CSD and C_{Start} start charging. As CSD reaches two-thirds V_{aa}, the Class D stage starts oscillating. The Class D amplifier is now operational, but the preamp output remains muted until C_{Start} reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

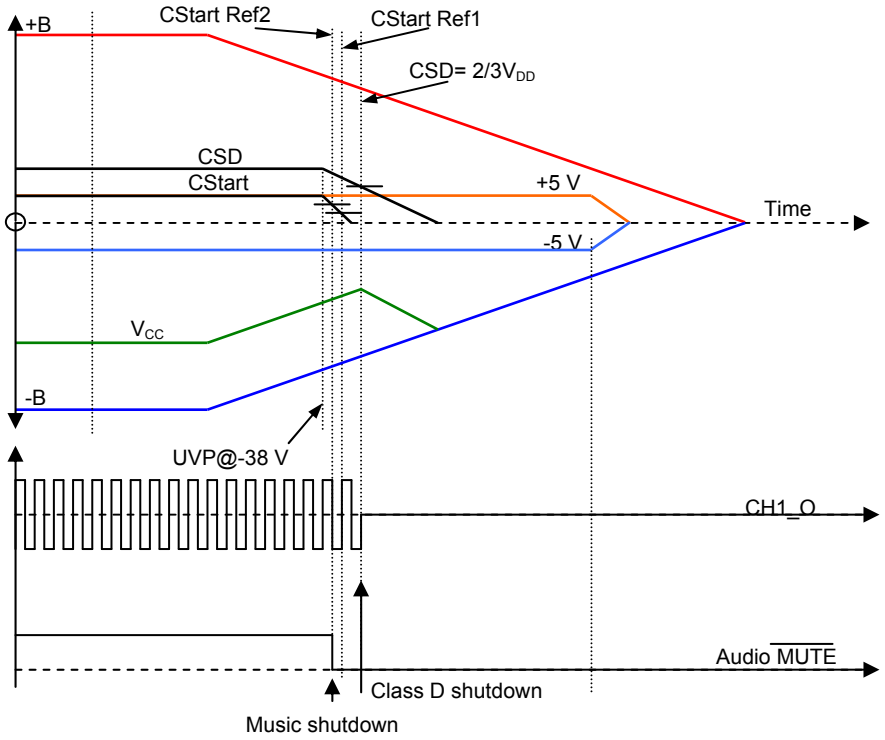

Figure 14. Conceptual Shutdown Sequencing of Power Supplies and Audio Section Timing.

Shutdown sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS2092S trips UVP. Once UVP is activated, CSD and C_{start} are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. Once C_{Start} reaches threshold Ref1, the click-noise reduction circuit is activated. It is then possible to shutdown the Class D stage (CSD reaches two-thirds V_{DD}). This process takes less than 200 ms.

For any external fault condition (OTP, OVP, UVP or DCP – see “Protection”) that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

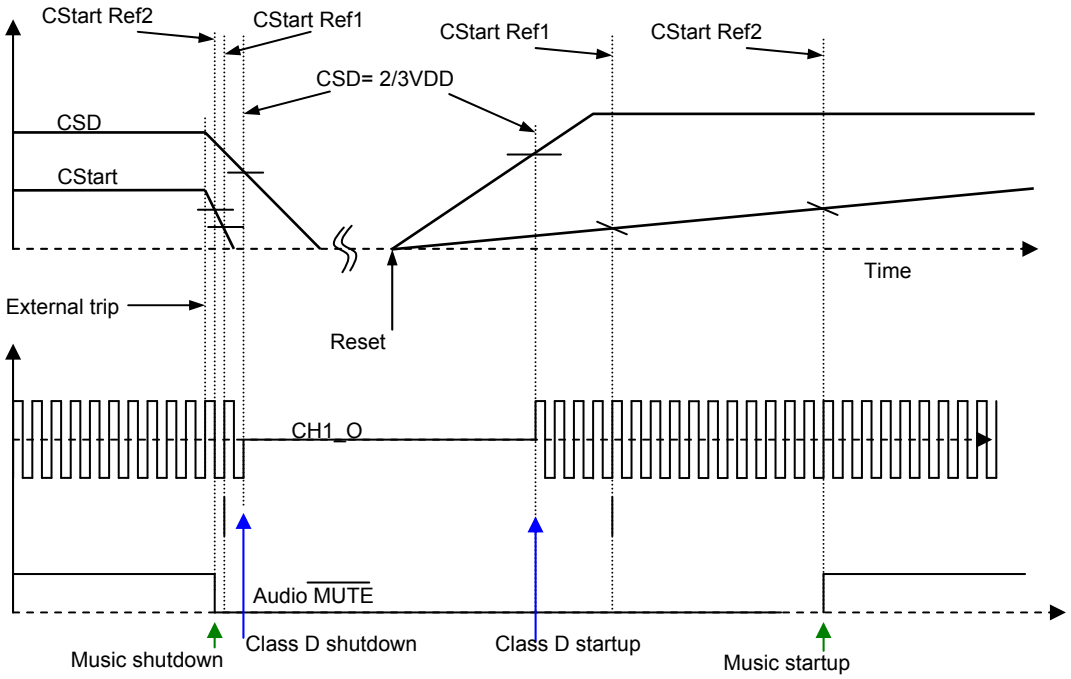

Figure 15. Conceptual Click Noise Reduction Sequencing at Trip and Reset

Protection System Overview

The IRS2092S integrates over current protection (OCP) inside the IC. The rest of the protections, such as over-voltage protection (OVP), under-voltage protection (UVP), and over temperature protection (OTP), are detected externally to the IRS2092S.

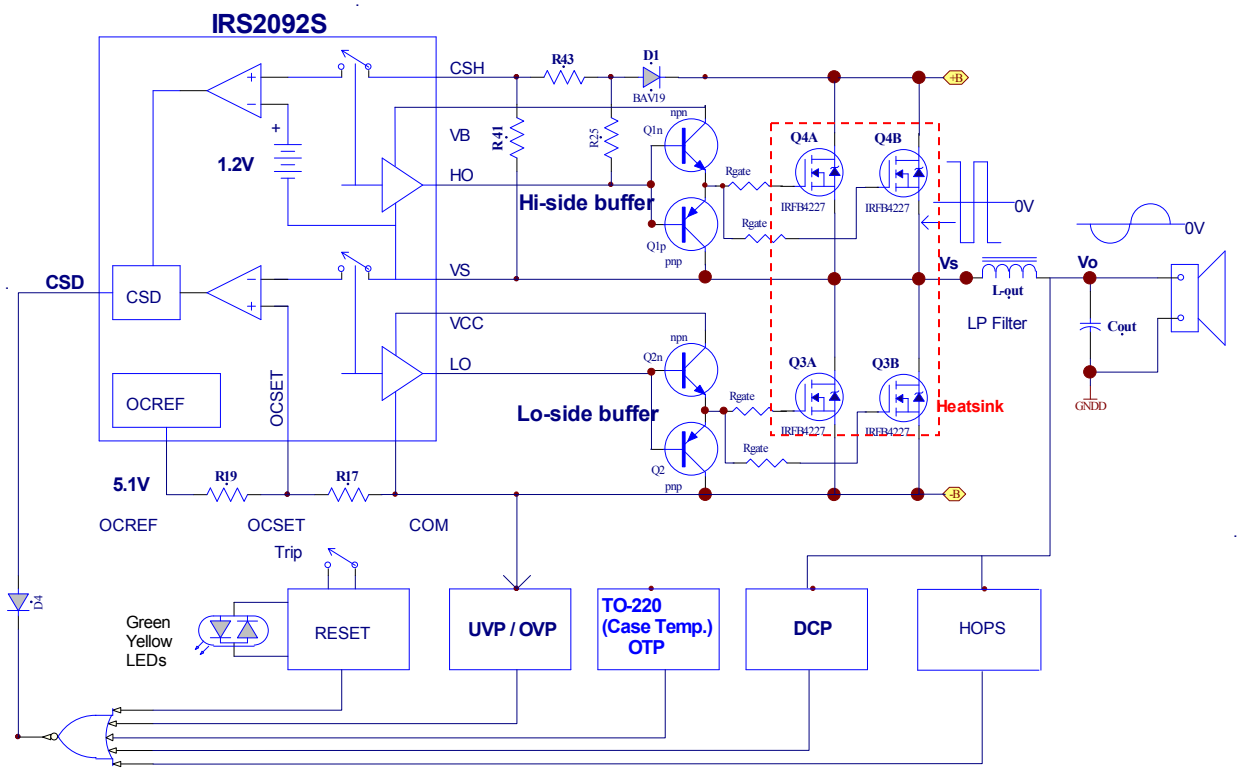

Figure 16. Functional Block Diagram of Protection Circuit Implementation

The external shutdown circuit will disable the output by pulling down CSD pins . If the fault condition persists, the protection circuit stays in shutdown until the fault is removed.

Over-Current Protection (OCP)

The OCP internal to the IRS2092S shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the application note AN1138. Here is a brief description:

Low-Side Current Sensing

The low-side current sensing feature protects the low side MOSFET from an overload condition from negative load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level. An external resistive divider R17 and R19 on the daughter board are used to program the low-side OCP trip point.

The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. When the VS voltage becomes higher than the OCSET voltage during low-side conduction, the IRS2092S turns the outputs OFF and pulls CSD down to -VSS.

High-Side Current Sensing

The high-side current sensing protects the high side MOSFET from an overload condition from positive load current by measuring drain-to-source voltage across $R_{DS(ON)}$ during its on state. OCP shuts down the switching operation if the drain-to-source voltage exceeds a preset trip level.

High-side over-current sensing monitors drain-to-source voltage of the high-side MOSFET during the on state through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of the CSH pin to trigger OC protection is internally fixed at 1.2V. An external resistive divider, R41 and R43 are used to program a hi-side OCP trip point. An external reverse blocking diode D8 is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D1, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source.

Input Bus Over-Voltage Protection (OVP)

OVP is provided externally to the IRS2092S. OVP shuts down the amplifier if the bus voltage between GND and -B exceeds 82V. The threshold is determined by a Zener diode Z9. OVP protects the board from harmful excessive supply voltages, such as due to bus pumping at very low frequency-continuous output in stereo mode.

Input Bus Under-Voltage Protection (UVP)

UVP is provided externally to the IRS2092S. UVP prevents unwanted audible noise output from unstable PWM operation during power up and down. UVP shuts down the amplifier if the bus voltage between GND and -B falls below a voltage set by Zener diode Z8.

Speaker DC-offset Protection (DCP)

DCP protects speakers against DC output current feeding to its voice coil. DC offset detection detects abnormal DC offset and shuts down PWM. If this abnormal condition is caused by a MOSFET failure because one of the high-side or low-side MOSFETs short circuited and remained in the on state, the power supply needs to be cut off in order to protect the speakers. Output DC offset greater than ±2.1V triggers DCP.

Offset Null (DC Offset) Adjustment

The IRAUDAMP9 is designed such that no output-offset nullification is required. DC offsets are tested to be less than ±50 mV.

Over-Temperature Protection (OTP)

An external NTC resistor is placed in close proximity to the low-side Q5A IRFB4227 TO-220 MOSFET. If the thermistor temperature rises above 100 °C, the OTP is activated. The OTP protection will shut down switching by pulling the CSD pin low and will recover once the temperature at the NTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the MOSFET of about 100 °C. This setting is limited by the PCB material and not by the operating range of the MOSFET.

Thermal Considerations

Due to limited heat sink size, the IRAUDAMP9 is designed for high efficiency to deliver 1 kW rated power for 1 minute at open-air room temperature (starting w/ Tamb: ~22 - 25C)
However, the IRAUDAMP9 requires larger heatsink design to handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards. If the user decides to increase the size of the heatsink or have a minimum forced air-cooling, the daughter board can handle continuous rated power.

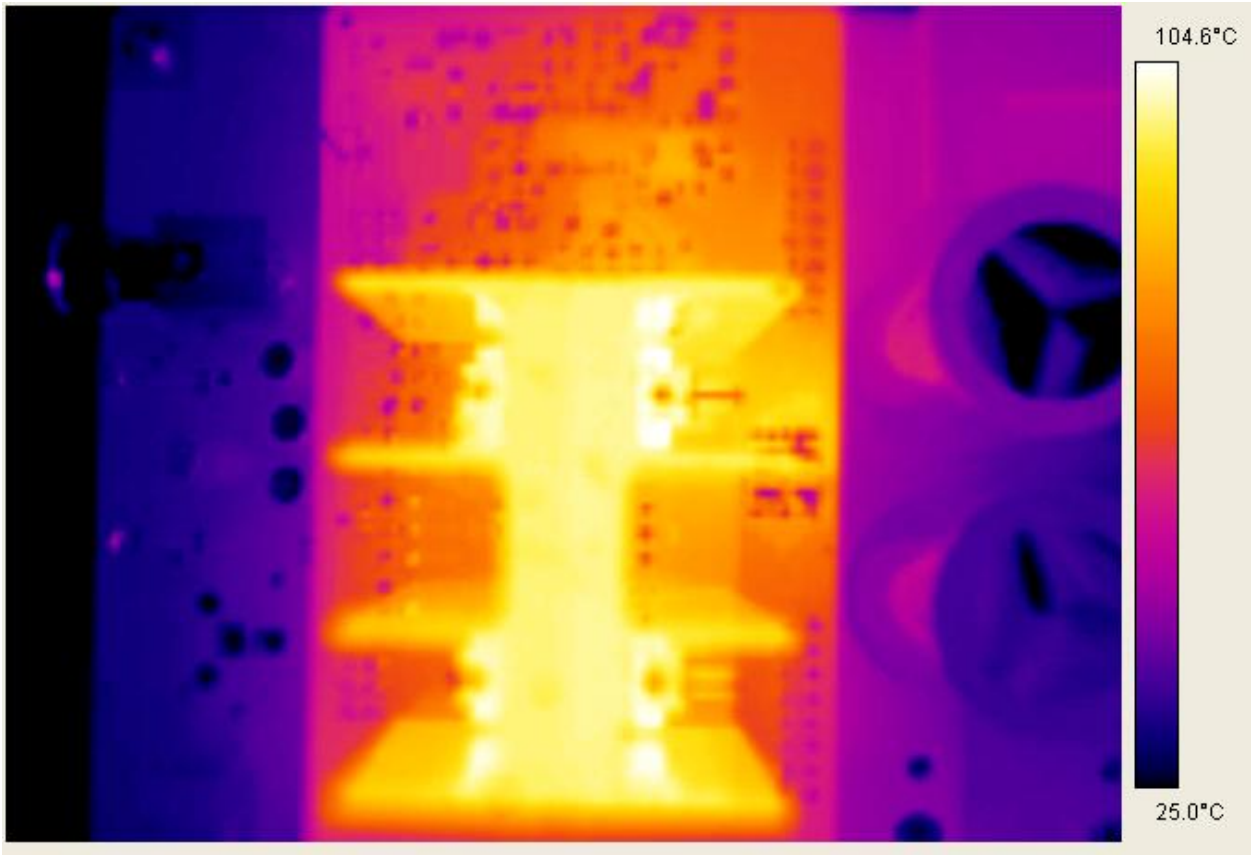

Figure 17. Thermal image of the heatsink assembly during 1/8 rated power burn-in test.

Short Circuit Protection Response

Figures 18-19 show over current protection reaction time of the IRAUDAMP9 in a short circuit event. As soon as the IRS2092S detects an over current condition, it shuts down PWM. After one second, the IRS2092S tries to resume the PWM. If the short circuit persists, the IRS2092S repeats try and fail sequences until the short circuit is removed.

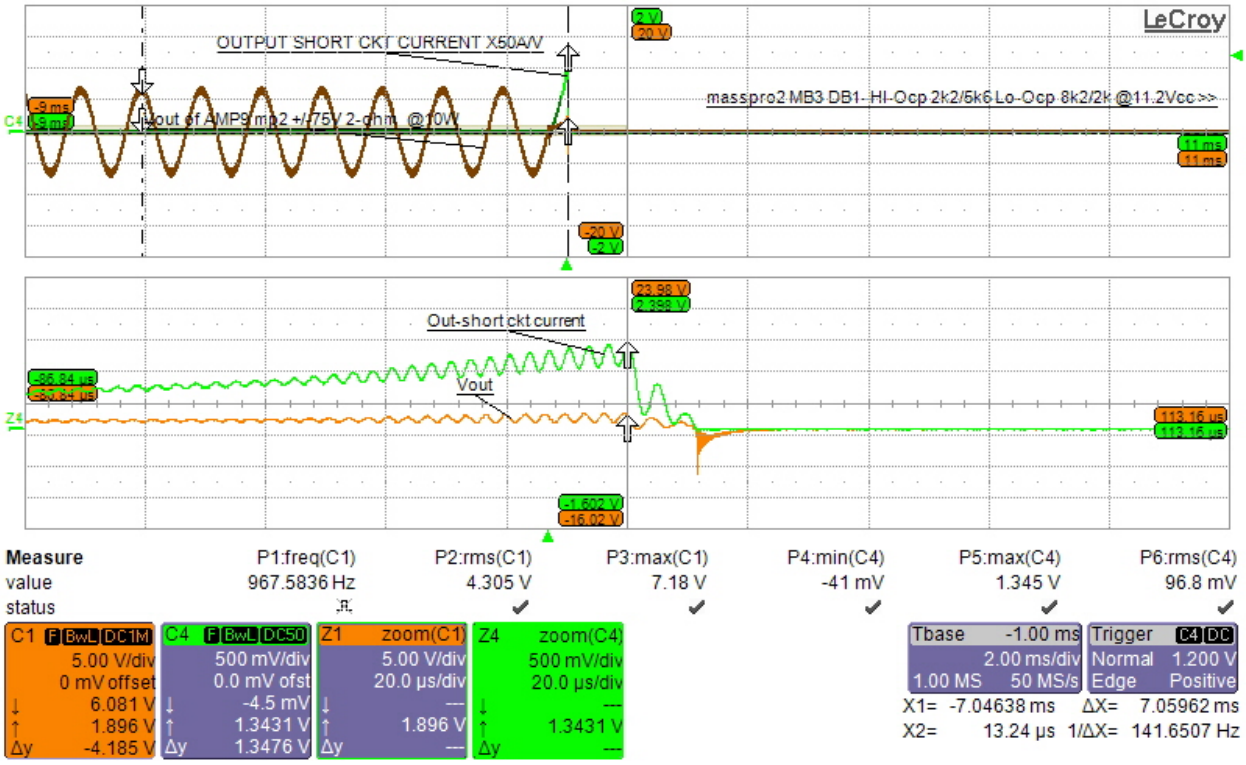

Figure 18. Positive-side OCP waveforms during short circuit test at 10W load condition.

High side OCP Calculation :

Given:

Vf = 0.7V, R_{dsON} : 9.85 mohm : 2 // IRFB4227

V_{dsON} = Idtrip * R_{dsON} = 0.985 V

Let R43 = 2.2 kohm, R41 = 5.6 kohm

$$I_{dtrip\_Hi-side} = \frac{(\frac{V_{thOCH} * (R41 + R43)}{R41}) - V_f)}{R_{dsON}}$$ **= Calculated OCP current limit: ~99 Apk**

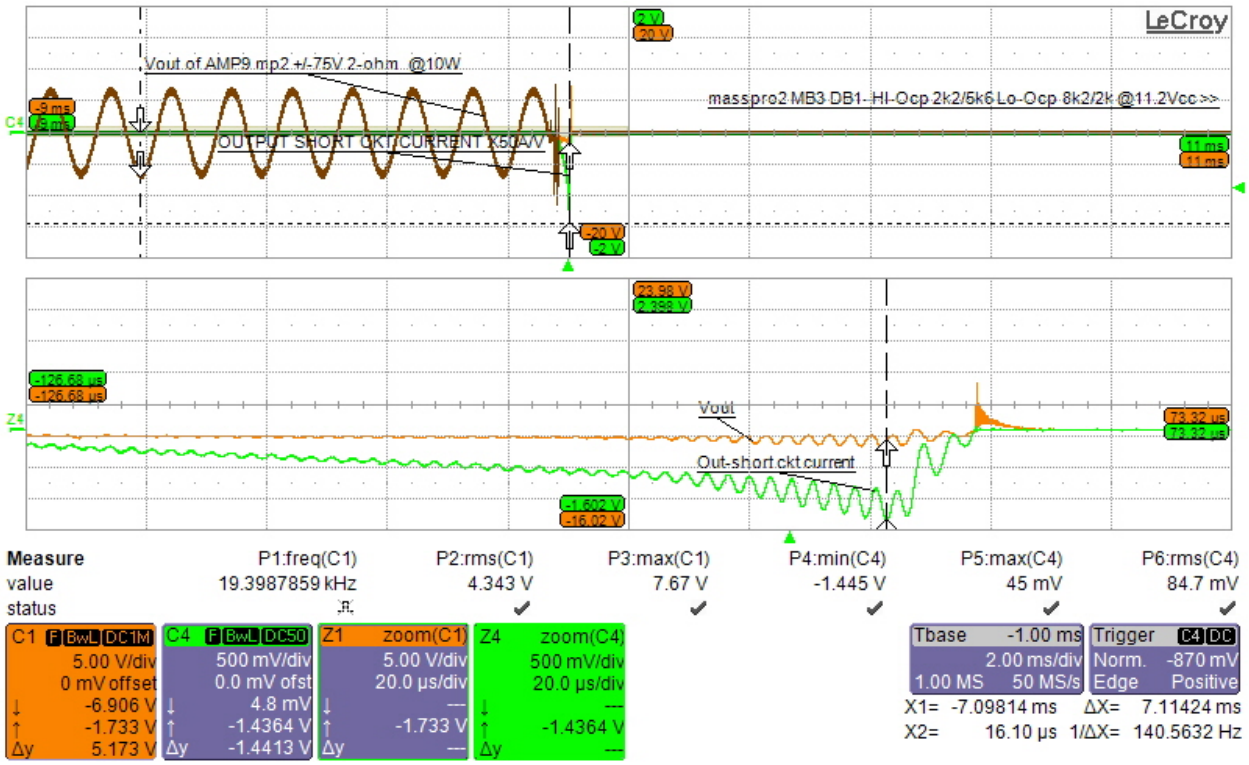

Figure 19 Negative-side OCP waveforms during short circuit test at clipping condition.

Lo- side OCP Calculation :

Given: Vref = 5.1V

R_{dsON} (for 2 // IRFB4227) : 9.85 mohm

Let R19 = 8.2 kohm, R17 = 2.0 kohm

$$V_{OCset} = Vref * R17 / (R17+R19)$$

$$I_{dtrip\_Lo\text{-}side} * R_{dsON} = V_{OCset}$$

$$I_{dtrip\_Lo-side} = \frac{Vref * (\frac{R17}{(R17+R19)})}{R_{dsON}}$$ **= Calculated OCP current limit: ~101 Apk**

Schematic Diagrams

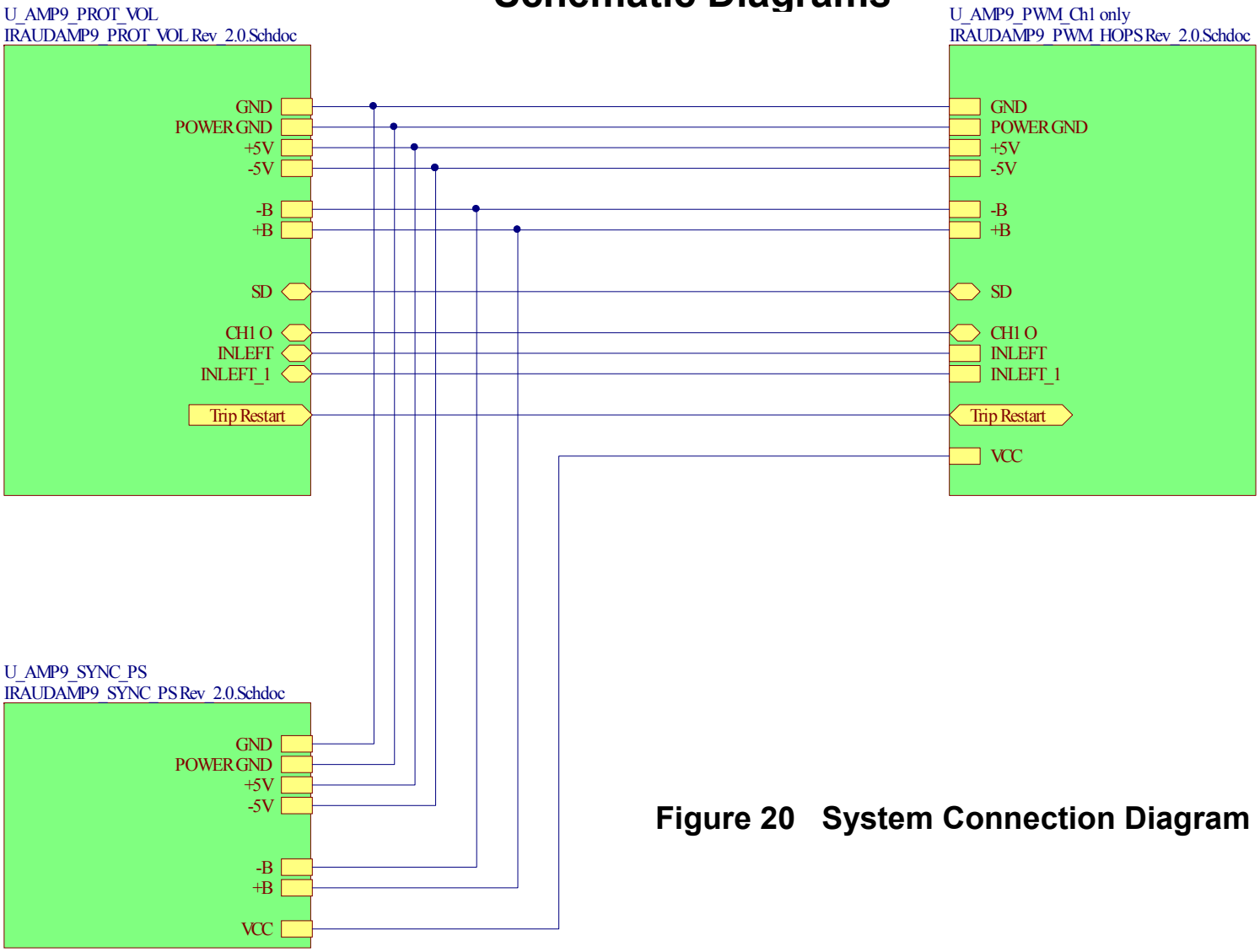

Figure 20 System Connection Diagram

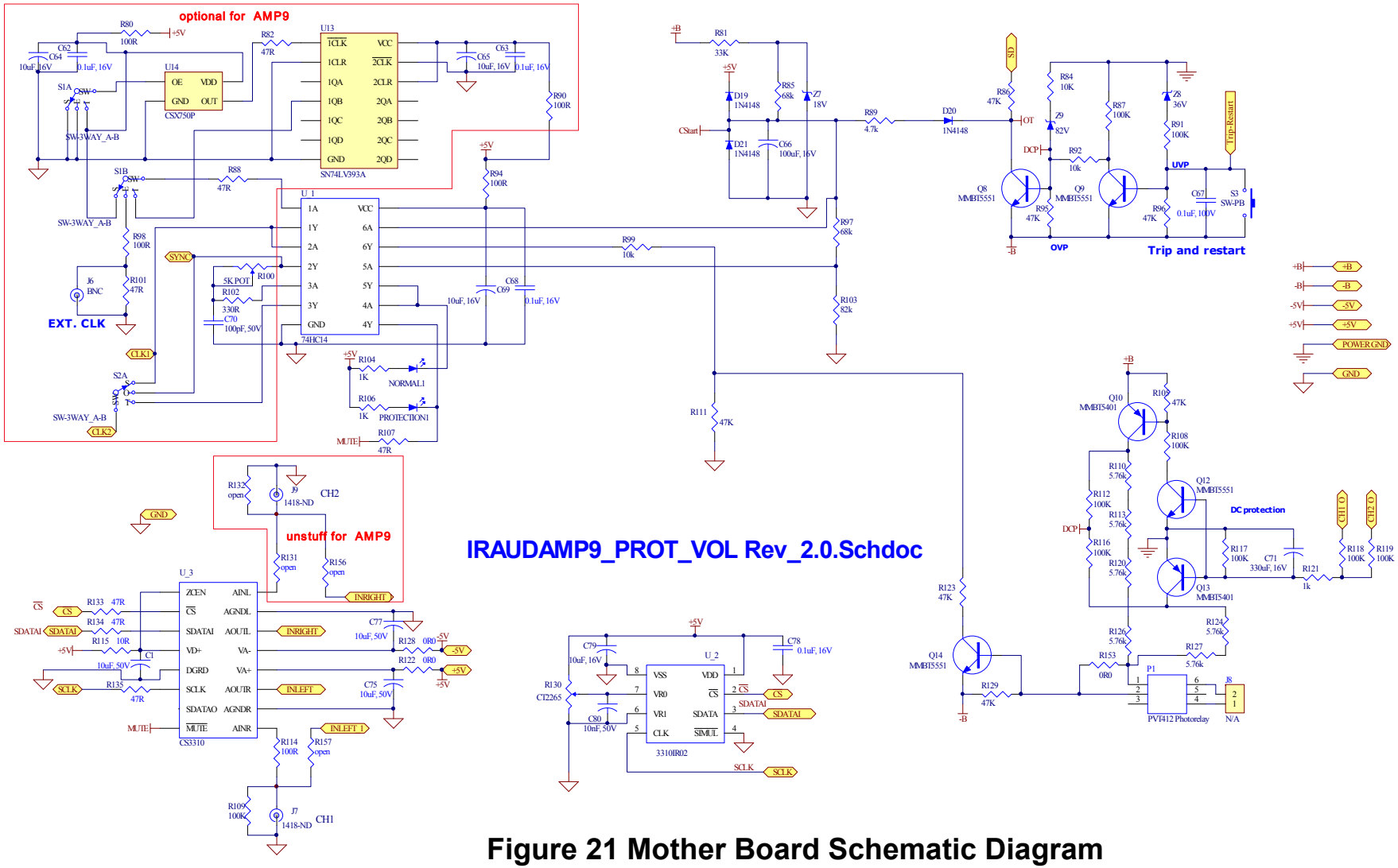

Figure 21 Mother Board Schematic Diagram
Housekeeping Protection and Volume Control Circuit

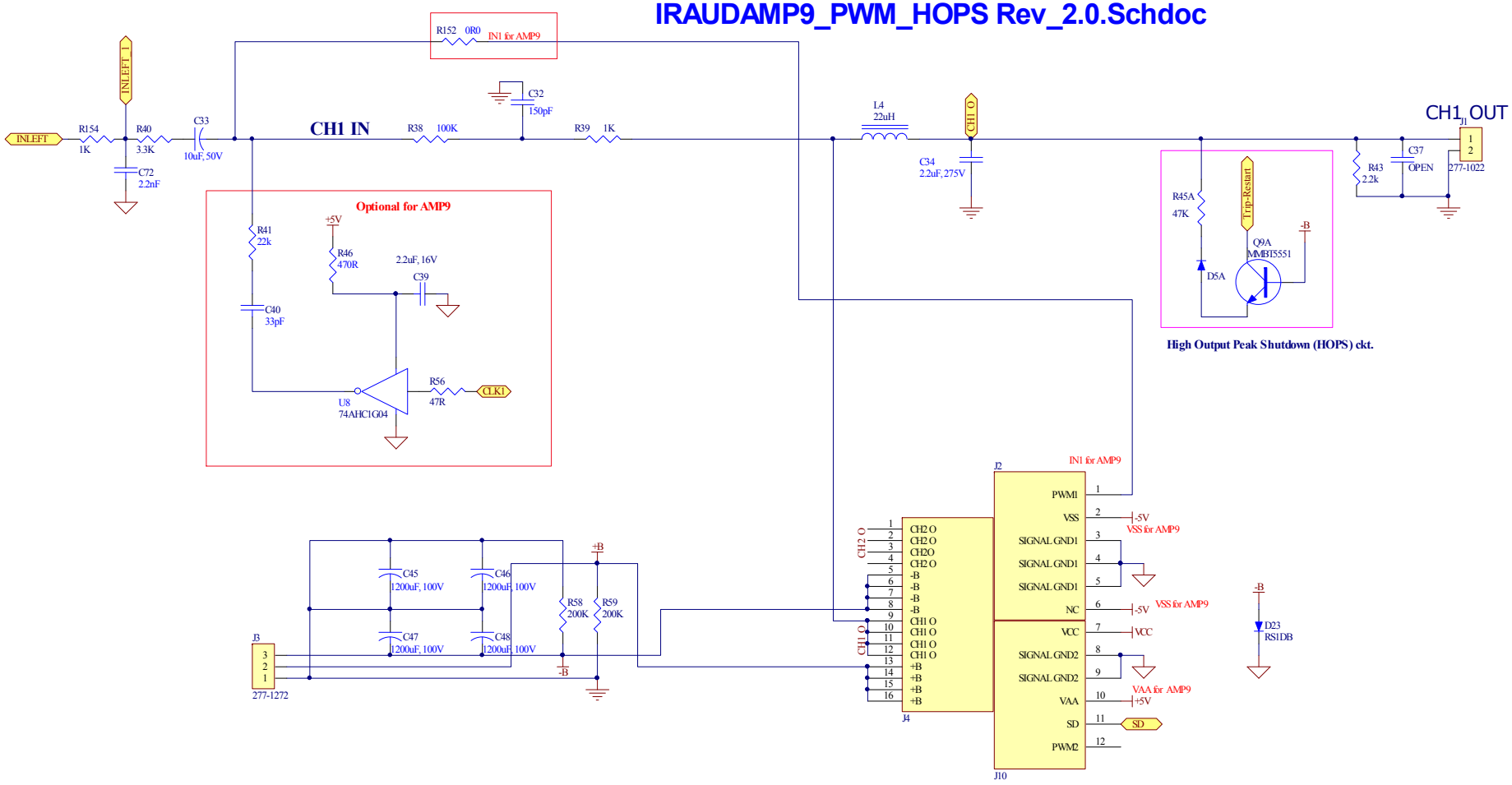

Figure 22 Mother Board Schematic Diagram
Input / Output Power Connection

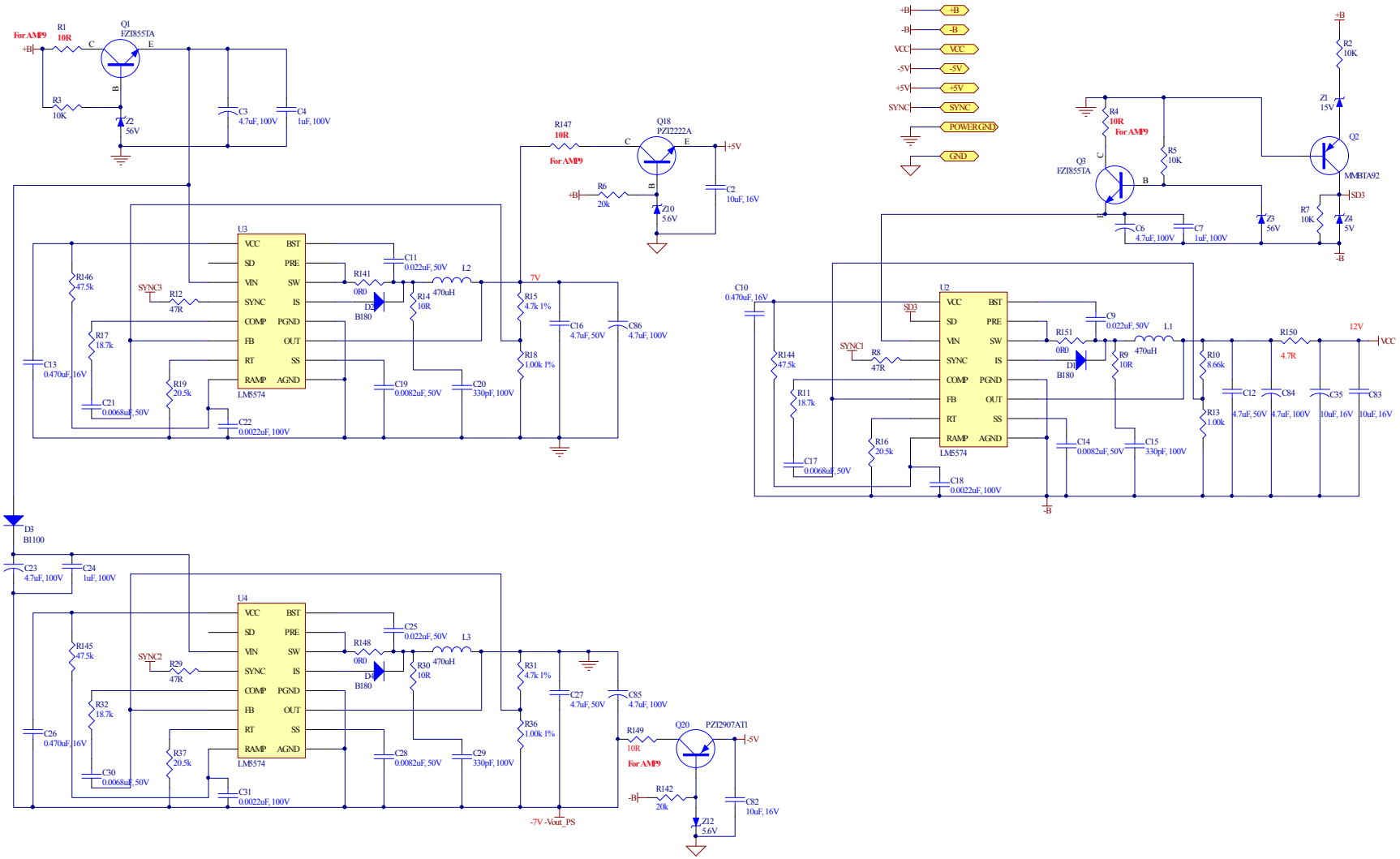

Figure 23 Mother Board Schematic Diagram
DCDC converter for Vaa, Vss and Vcc power supplies

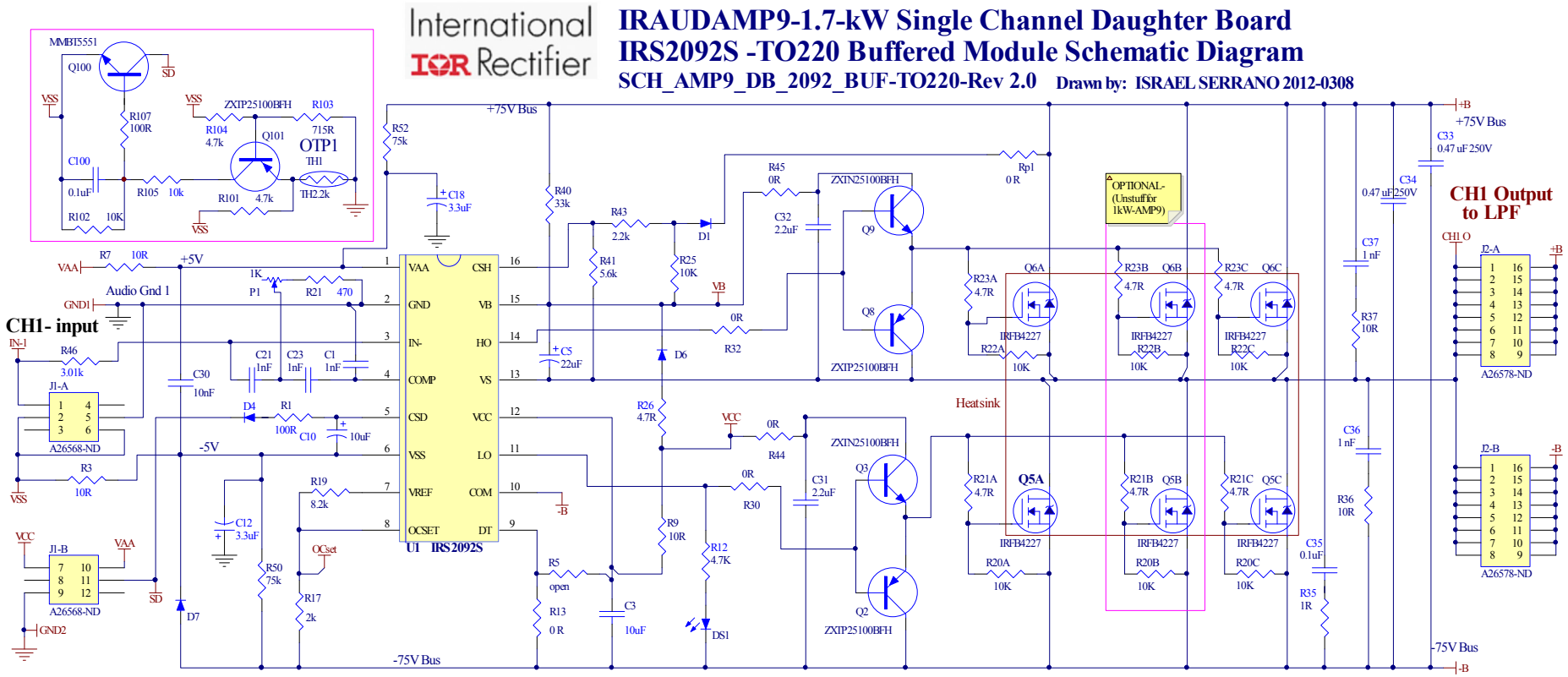

Figure 24 IRAUDAMP9 Schematic Diagram for Daughter Board

IRAUDAMP9 Fabrication Bill Of Materials (BOM)

Table 1 IRAUDAMP9 Mother Board's BOM

Item	PN	Designator	Qty	Description	Vendor
1	C1, C33, C75, C77	565-1106-ND	4	CAP 10UF 50V ELECT SMG RAD	DigiKey
2	C2, C82, C83	PCC13491CT-ND	3	CAP 10UF 16V CERAMIC X7R 1206	DigiKey
3	C3, C6, C23, C84, C85, C86	565-1147-ND	6	CAP 4.7UF 100V ELECT SMG RAD	DigiKey
4	C4, C7, C24	490-1857-1-ND	3	CAP CER 1.0UF 100V 10% X7R 1210	DigiKey
5	C9, C11, C25	490-1644-1-ND	3	CAP CER 22000PF 50V 5% C0G 0805	DigiKey
6	C10, C13, C26	478-1403-1-ND	3	CAP CERM .47UF 10% 16V X7R 0805	DigiKey
7	C12, C16, C27	490-1864-1-ND	3	CAP CER 4.7UF 50V 10% X7R 1210	DigiKey
8	C14, C19, C28	445-2685-1-ND	3	CAP CER 8200PF 50V C0G 5% 0805	DigiKey
9	C15, C20, C29	PCC1982CT-ND	3	CAP 330PF 100V CERAMIC X7R 0805	DigiKey
10	C17, C21, C30	478-3772-1-ND	3	CAP CERM 6800PF 5% 50V X7R 0805	DigiKey
11	C18, C22, C31	478-3746-1-ND	3	CAP CERM 2200PF 5% 100V X7R 0805	DigiKey
12	C32	445-2378-1-ND	1	CAP CER 150PF 3000V C0G 10% 1812	DigiKey
13	C34	399-5432-ND	1	CAP 2.2 uF 275/280VAC X2 METAL POLYPRO	DigiKey
14	C35, C64, C65, C69, C79	PCE3101CT-ND	5	CAP 10UF 16V ELECT FC SMD	DigiKey
15	C37, R8, R12, R29, R131, R132, R156, R157	open	8	Bypass vol ctrl, open	DigiKey
16	C39	PCC1931CT-ND	1	CAP 2.2UF 16V CERAMIC X7R 1206	DigiKey
17	C40	478-1281-1-ND	1	CAP CERM 33PF 5% 100V NP0 0805	DigiKey
18	C45, C46, C47, C48	565-1161-ND	4	CAP 1200UF 100V ELECT SMG RAD	DigiKey
19	C62, C63, C68, C78	PCC1812CT-ND	4	CAP .1UF 16V CERAMIC X7R 0805	DigiKey
20	C66	565-1037-ND	1	CAP 100UF 16V ELECT SMG RAD	DigiKey
21	C67	445-1418-1-ND	1	CAP CER .10UF 100V X7R 10% 0805	DigiKey
22	C70	PCC101CGCT-ND	1	CAP 100PF 50V CERM CHIP 0805 SMD	DigiKey
23	C71	493-1042-ND	1	CAP 330UF 16V ELECT VR RADIAL	DigiKey
24	C72	445-2322-1-ND	1	CAP CER 2200PF 100V C0G 5% 0805	DigiKey
25	C80	PCC103BNCT-ND	1	CAP 10000PF 50V CERM CHIP 0805	DigiKey
26	D1, D2, D4	B180DICT-ND	3	DIODE SCHOTTKY 80V 1A SMA	DigiKey
27	D3	B1100-FDICT-ND	1	DIODE SCHOTTKY 100V 1A SMA	DigiKey
28	D5A	BAV19WS-7-F	1	DIODE SWITCH 100V 200MW SOD323	DigiKey
29	D19, D20, D21	1N4148WTPMSCT-ND	3	DIODE SWITCH 100V 150MA SOD123	DigiKey
30	D23	RS1DB-FDICT-ND	1	DIODE FAST REC 200V 1A SMB	DigiKey
31	J1	277-1271-ND	1	CONN TERM BLOCK 2POS 9.52MM PCB	DigiKey
32	J2	A26453-ND	1	CONN RECEPT 6POS .100 VERT DUAL	DigiKey
33	J3	277-1272-ND	1	CONN TERM BLOCK 3POS 9.52MM PCB	DigiKey
34	J4	A26454-ND	1	CONN RECEPT 8POS .100 VERT DUAL	DigiKey
35	J6	A32248-ND	1	CONN JACK BNC R/A 50 OHM PCB TIN	DigiKey
36	J7, J9	CP-1418-ND	2	CONN RCA JACK R/A BLACK PCB	DigiKey

37	J8	ED1567	1	TERMINAL BLOCK 7.50MM VERT 2POS	DigiKey
38	J10	A26453-ND	1	CONN RECEPT 6POS .100 VERT DUAL	DigiKey
39	L1, L2, L3	513-1051-1-ND	3	INDUCTOR SHIELD PWR 470UH SMD	DigiKey
40	L4	7G31A-220M-R	1	22uH Power ferrite inductor	Sagami
41	NORMAL1, PROTECTION1	160-1140-ND, 160-1143-ND	2	LED 3MM GREEN TRANSPARENT, LED 3MM HI-EFF RED TRANSPARENT	DigiKey
42	P1	PVT412LPBF-ND	1	Power MOSFET Photovoltaic Relay	DigiKey
43	Q1, Q3	FZT855CT-ND	2	TRANS NPN 150V 4000MA SOT-223	DigiKey
44	Q2	MMBTA92DICT-ND	1	TRANSISTOR PNP -300V SOT-23	DigiKey
45	Q8, Q9, Q9A, Q12, Q14	MMBT5551-7DICT-ND	5	TRANS 160V 350MW NPN SMD SOT-23	DigiKey
46	Q10, Q13	MMBT5401DICT-ND	2	TRANS 150V 350MW PNP SMD SOT-23	DigiKey
47	Q18	PZT2222ACT-ND	1	TRANS AMP NPN GP 40V .5A SOT-223	DigiKey
48	Q20	PZT2907AT1GOSCT-ND	1	TRANS SS SW PNP 600MA 60V SOT223	DigiKey
49	R1, R4, R9, R14, R30	PT10XCT-ND	5	RES 10 OHM 1W 5% 2512 SMD	DigiKey
50	R2, R3, R5, R7, R84, R92, R99	P10KACT-ND	7	RES 10K OHM 1/8W 5% 0805 SMD	DigiKey
51	R6, R142	P20KACT-ND	2	RES 20K OHM 1/8W 5% 0805 SMD	DigiKey
52	R10	RHM8.66KCRCT-ND	1	RES 8.66K OHM 1/8W 1% 0805 SMD	DigiKey
53	R11, R17, R32	P18.7KCCT-ND	3	RES 18.7K OHM 1/8W 1% 0805 SMD	DigiKey
54	R13	P1.00KCCT-ND	1	RES 1.00K OHM 1/8W 1% 0805 SMD	DigiKey
55	R15, R31	P4.7KCCT-ND	2	RES 4.70K OHM 1/8W 1% 0805 SMD	DigiKey
56	R16, R19, R37	P20.5KCCT-ND	3	RES 20.5K OHM 1/8W 1% 0805 SMD	DigiKey
57	R18, R36	P1.00KCCT-ND	2	RES 1.00K OHM 1/8W 1% 0805 SMD	DigiKey
58	R38	PPC100KW-3JCT-ND	1	RES 100K OHM METAL FILM 3W 5%	DigiKey
59	R39	P1.0KECT-ND	1	RES 1.0K OHM 1/4W 5% 1206 SMD	DigiKey
60	R40	P3.3KZCT-ND	1	RES 3.3K OHM 1/10W .1% 0805 SMD	DigiKey
61	R41	P22KACT-ND	1	RES 22K OHM 1/8W 5% 0805 SMD	DigiKey
62	R43	PT2.2KXCT-ND	1	RES 2.2K OHM 1W 5% 2512 SMD	DigiKey
63	R45A, R86, R95, R96, R105, R111, R123, R129	P47KACT-ND	8	RES 47K OHM 1/8W 5% 0805 SMD	DigiKey
64	R46	311-470ARCT-ND	1	RES 470 OHM 1/8W 5% 0805 SMD	DigiKey
65	R56, R82, R88, R101, R107, R133, R134, R135	P47ACT-ND	8	RES 47 OHM 1/8W 5% 0805 SMD	DigiKey
66	R58, R59	P200KACT-ND	2	RES 200K OHM 1/8W 5% 0805 SMD	DigiKey
67	R80, R90, R94	P100ECT-ND	3	RES 100 OHM 1/4W 5% 1206 SMD	DigiKey
68	R81	P33KACT-ND	1	RES 33K OHM 1/8W 5% 0805 SMD	DigiKey
69	R85, R97	P68KACT-ND	2	RES 68K OHM 1/8W 5% 0805 SMD	DigiKey
70	R87, R91, R108, R109, R112, R116, R117, R118, R119	P100KACT-ND	9	RES 100K OHM 1/8W 5% 0805 SMD	DigiKey
71	R89	P4.7KACT-ND	1	RES 4.7K OHM 1/8W 5% 0805 SMD	DigiKey
72	R98, R114	P100ACT-ND	2	RES 100 OHM 1/8W 5% 0805 SMD	DigiKey
73	R100	3362H-502LF-ND	1	POT 5.0K OHM 1/4" SQ CERM SL ST	DigiKey
74	R102	P330ACT-ND	1	RES 330 OHM 1/8W 5% 0805 SMD	DigiKey
75	R103	P82KACT-ND	1	RES 82K OHM 1/8W 5% 0805 SMD	DigiKey
76	R104, R106, R121, R154	311-1.0KARCT-ND,	4	RES 1.0K OHM 1/8W 5% 0805 SMD	DigiKey

77	R110, R113, R120, R124, R126, R127	P5.76KFCT-ND	6	RES 5.76K OHM 1/4W 1% 1206 SMD	DigiKey
78	R115	P10ECT-ND	1	RES 10 OHM 1/4W 5% 1206 SMD	DigiKey
79	R122, R128, R152, R153	P0.0ECT-ND	4	RES ZERO OHM 1/4W 5% 1206 SMD	DigiKey
80	R130	P3G7103-ND	1	POT 10K OHM 9MM VERT MET BUSHING	DigiKey
81	R141, R148, R151	RMCF1/100RCT-ND	3	RES 0.0 OHM 1/8W 0805 SMD	DigiKey
82	R144, R145, R146	P47.5KCCT-ND	3	RES 47.5K OHM 1/8W 1% 0805 SMD	DigiKey
83	R147, R149	PT10XCT-ND	2	RES 10 OHM 1W 5% 2512 SMD	DigiKey
84	R150	PT4.7XCT-ND	1	RES 4.7 OHM 1W 5% 2512 SMD	DigiKey
85	S1, S2	EG1944-ND	2	SWITCH SLIDE DP3T .2A L=6MM	DigiKey
86	S3	P8010S-ND	1	6MM LIGHT TOUCH SW H=5	DigiKey
87	U2, U3, U4	LM5574MT-ND	3	IC REG BUCK 75V 0.5A 16-TSSOP	DigiKey
88	U8	296-1089-1-ND	1	IC SINGLE INVERTER GATE SOT23-5	DigiKey
89	U13	296-11643-1-ND	1	DUAL 4-BIT BINARY COUNTERS	DigiKey
90	U14	300-8001-1-ND	1	OSCILLATOR 1.5440 MHZ SMT	DigiKey
91	U_1	296-1194-1-ND	1	IC HEX SCHMITT-TRIG INV 14-SOIC	DigiKey
92	U_2	3310IR02	1	3310SO6S Digital IC	Tachyonix
93	U_3	598-1599-ND	1	Amplifiers - Audio Stereo Digital Volume Control	DigiKey
94	Z1	BZT52C15-7DICT-ND	1	DIODE ZENER 15V 500MW SOD-123	DigiKey
95	Z2, Z3	MMSZ5263BT1OSCT-ND	2	DIODE ZENER 500MW 56V SOD123	DigiKey
96	Z4	BZT52C5V1-7DICT-ND	1	DIODE ZENER 5.1V 500MW SOD-123	DigiKey
97	Z7	BZT52C18-FDICT-ND	1	DIODE ZENER 500MW 18V SOD123	DigiKey
98	Z8	BZT52C36-7DICT-ND	1	DIODE ZENER 36V 500MW SOD-123	DigiKey
99	Z9	MMSZ5268BT1GOSCT-ND	1	DIODE ZENER 82V 500mW SOD-123	DigiKey
100	Z10, Z12	BZT52C5V6-FDICT-ND	2	DIODE ZENER 5.6V 500MW SOD123	DigiKey

Table 2 IRAUDAMP9 Daughter Board's Bill of Materials

Item	Digikey / Mouser PN	Designator	Description	Qty
1	445-2325-1-ND	C1, C21, C23	CAP CER 1000PF 250V C0G 5% 0805	3
2	490-1867-1-ND	C3	CAP CER 10UF 25V 10% X7R 1210	1
3	T491A226K025AT	C5	CAP TANTALUM 22UF 25V 10% SMD	1
4	490-1867-1-ND	C10	CAP CER 10UF 25V 10% X7R 1210	1
5	445-1432-1-ND	C12, C18	CAP CER 3.3UF 50V X7R 20% 1210	2
6	PCC103BNCT-ND	C30	CAP 10000PF 50V CERM CHIP 0805	1
7	490-3368-1-ND	C31, C32	CAP CER 2.2UF 25V X7R 10% 1210	2
8	478-3988-1-ND	C33, C34	CAP CER 0.47UF 250V X7R 1812	2
9	399-4678-1-ND	C35	CAP CER 0.1UF 250V X7R 1206	1
10	478-5552-1-ND	C36, C37	CAP CER 1000PF 250V X7R 1206	2
11	445-2686-1-ND	C100	CAP CER 0.1UF 10V SL 5% 0805	1
12	BAV19WS-FDICT-ND	D1	DIODE SWITCH 100V 200MW SOD323	1
13	1N4148WS-FDICT-ND	D4	DIODE SWITCH 75V 200MW SOD323	1
14	MURA120T3GOSCT-ND	D6	DIODE ULTRA FAST 1A 200V SMA	1
15	ES1DFSCT-ND	D7	DIODE ULTRAFAST 200V 1A DO-214AC	1
16	160-1645-1-ND	DS1	LED 468NM BLUE CLEAR 0805 SMD	1
17	A26568-ND	J1-A, J1-B	CONN HEADER VERT 6POS .100 30AU	2
18	A26578-ND	J2-A, J2-B	CONN HEADER VERT .100 16POS 30AU	2
19	ST32ETB102CT-ND	P1	POT 1.0K OHM 3MM CERM SQ TOP SMD	1
20	ZXTP25100BFHCT-ND	Q2, Q8, Q101	TRANSISTOR PNP 100V 2A SOT23-3	3
21	ZXTN25100BFHCT-ND	Q3, Q9	TRANSISTOR NPN 100V 3A SOT23-	2
22	MMBT5551-7DICT-ND	Q100	TRANS 160V 350MW NPN SMD SOT23-3	
23	**IRFB4227PBF**	Q5A, Q5C, Q6A, Q6C	200V 65A N-Channel MOSFET TO 220	4
24	P100ACT-ND	R1, R107	RES 100 OHM 1/8W 5% 0805 SMD	2
25	P10ACT-ND	R3	RES 10 OHM 1/8W 5% 0805 SMD	1
26	open	R5	open	1
27	P10ECT-ND	R7	RES 10 OHM 1/4W 5% 1206 SMD	1
28	P10ACT-ND	R9	RES 10 OHM 1/8W 5% 0805 SMD	1
29	P4.7KACT-ND	R12	RES 4.7K OHM 1/8W 5% 0805 SMD	1
30	P0.0ACT-ND	R13, R30, R32, R44, R45, Rp1	RES 0 OHM 1/8W 5% 0805 SMD	6
31	P2.0KACT-ND	R17	RES 2.0K OHM 1/8W 5% 0805 SMD	1
32	P8.2KACT-ND	R19	RES 8.2K OHM 1/8W 5% 0805 SMD	1
33	P10KACT-ND	R20A, R20B, R20C, R22A, R22B, R22C, R25	RES 10K OHM 1/8W 5% 0805 SMD	7

34	RHM470CRCT-ND	R21	RES 470 OHM 1/8W 1% 0805 SMD	1
35	P4.7ACT-ND	R21A, R21B, R21C, R23A, R23B, R23C, R26	RESISTOR 4.7 OHM 1/8W 5% 0805	7
36	P1.0ACT-ND	R35	RESISTOR 1.0 OHM 1/8W 5% 0805	1
37	PT10XCT-ND	R36, R37	RES 10 OHM 1W 5% 2512 SMD	2
38	RHM33KARCT-ND	R40	RES 33K OHM 1/8W 5% 0805 SMD	1
39	P5.6KACT-ND	R41	RES 5.6K OHM 1/8W 5% 0805 SMD	1
40	P2.2KACT-ND	R43	RES 2.2K OHM 1/8W 5% 0805 SMD	1
41	RHM3.01KCCT-ND	R46	RES 3.01K OHM 1/8W 1% 0805 SMD	1
42	RT1206FRE0775KL-ND	R50, R52	RES 75.0K OHM 1/8W 1% SMD 1206	2
43	RHM4.7KARCT-ND	R101, R104	RES 4.7K OHM 1/8W 5% 0805 SMD	2
44	RHM10KARCT-ND	R102, R105	RES 10K OHM 1/8W 5% 0805 SMD	2
45	RT1206FRE07715RL-ND	R103	RES 715 OHM 1/8W .5% SMD 1206	1
46	**IRS2092S**	U1	High and Low Side Driver	1

Table 3 IRAUDAMP9 Mechanical Bill of Materials

No	P/N	Description	Quantity	Vendor
1	7-342-2PP-BA	To220 Heatsink 15W HTSNK assy 1	2	Digi-Key
2		Silpad insulator pad	4	
3		Lock Washer	4	
4		mounting screws / nuts	4 sets	
5		plastic TO220-bushing	4	
6		Standoff	6	
7	AMP9 PCB MB	IRAUDAMP9 Main Board	1	
8	AMP9 PCB DB	IRAUDAMP9 Daughter Board	1	

IRAUDAMP9 PCB Specifications:

1. Two Layers SMT PCB with through holes
2. 1/16 thickness
3. 2/0 OZ Cu
4. FR4 material
5. 10 mil lines and spaces
6. Solder Mask to be Green enamel EMP110 DBG (CARAPACE) or Enthone Endplate DSR-3241or equivalent.
7. Silk Screen to be white epoxy non conductive per IPC–RB 276 Standard.
8. All exposed copper must finished with TIN-LEAD Sn 60 or 63 for 100u inches thick.
9. Tolerance of PCB size shall be 0.010 –0.000 inches
10. Tolerance of all Holes is -.000 + 0.003”
11. PCB acceptance criteria as defined for class II PCB’S standards.

Gerber Files Apertures Description:
All Gerber files stored in the attached CD-ROM were generated from Protel Altium Designer Altium Designer 6.

1. .gtl Top copper, top side
2. .gbl Bottom copper, bottom side
3. .gto Top silk screen
4. .gbo Bottom silk screen
5. .gts Top Solder Mask
6. .gbs Bottom Solder Mask
7. .gko Keep Out,
8. .gm1 Mechanical1
9. .gd1 Drill Drawing
10. .gg1 Drill locations
11. .txt CNC data
12. .apr Apertures data

Additional files for assembly that may not be related with Gerber files:

13. .pcb PCB file
14. .bom Bill of materials
15. .cpl Components locations
16. .sch Schematic
17. .csv Pick and Place Components
18. .net Net List
19. .bak Back up files
20. .lib PCB libraries

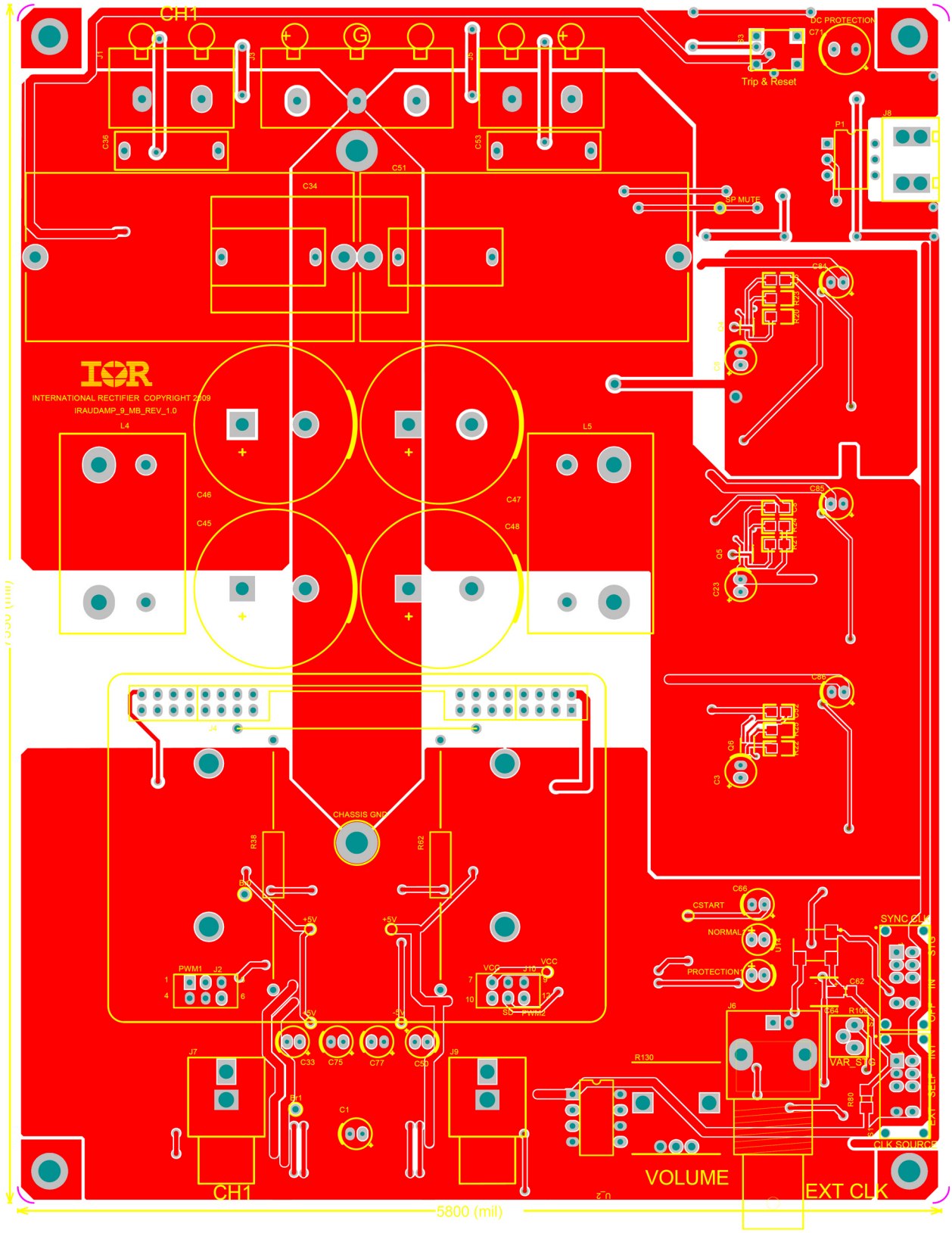

Figure 25 IRAUDAMP9 Mother board PCB Top Overlay (Top View)

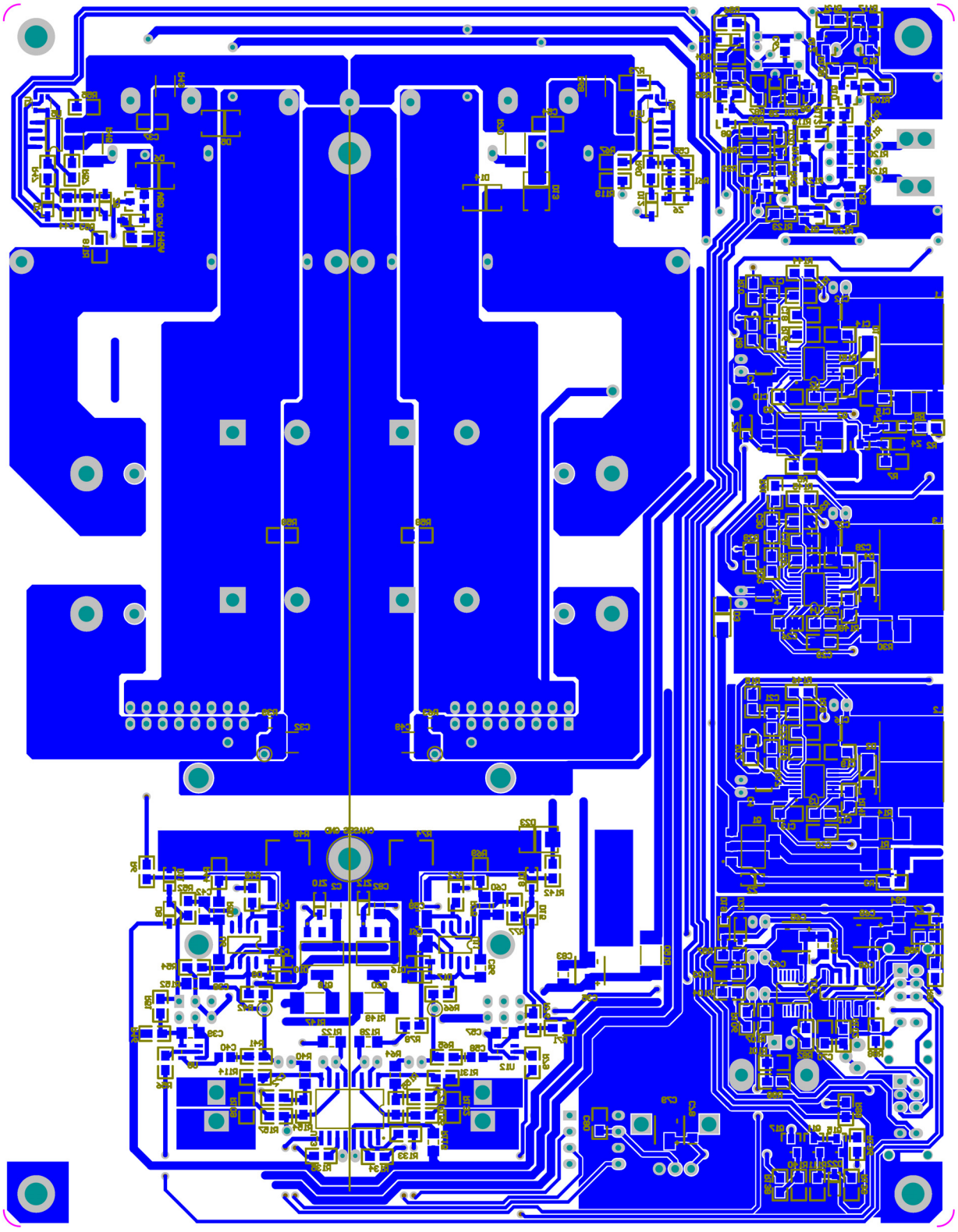

Figure 26 IRAUDAMP9 Mother board PCB Bottom Layer (Top View)

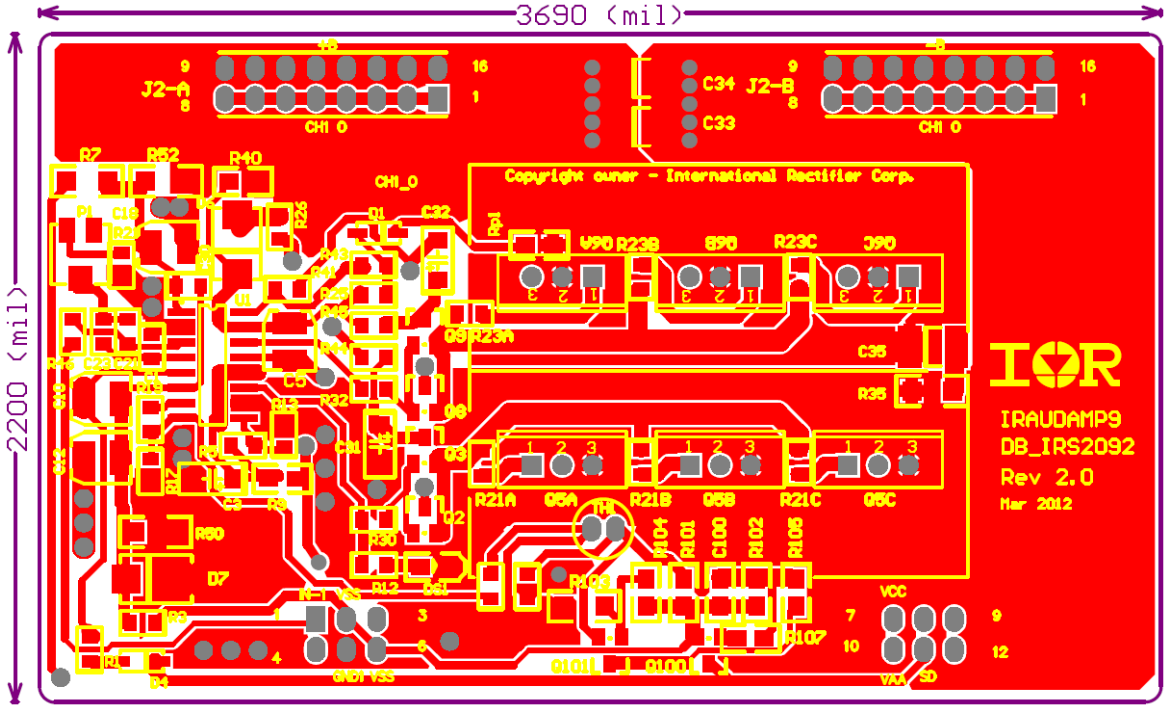

Figure 27 IRAUDAMP9 Daughter board PCB Top Overlay (Top View)

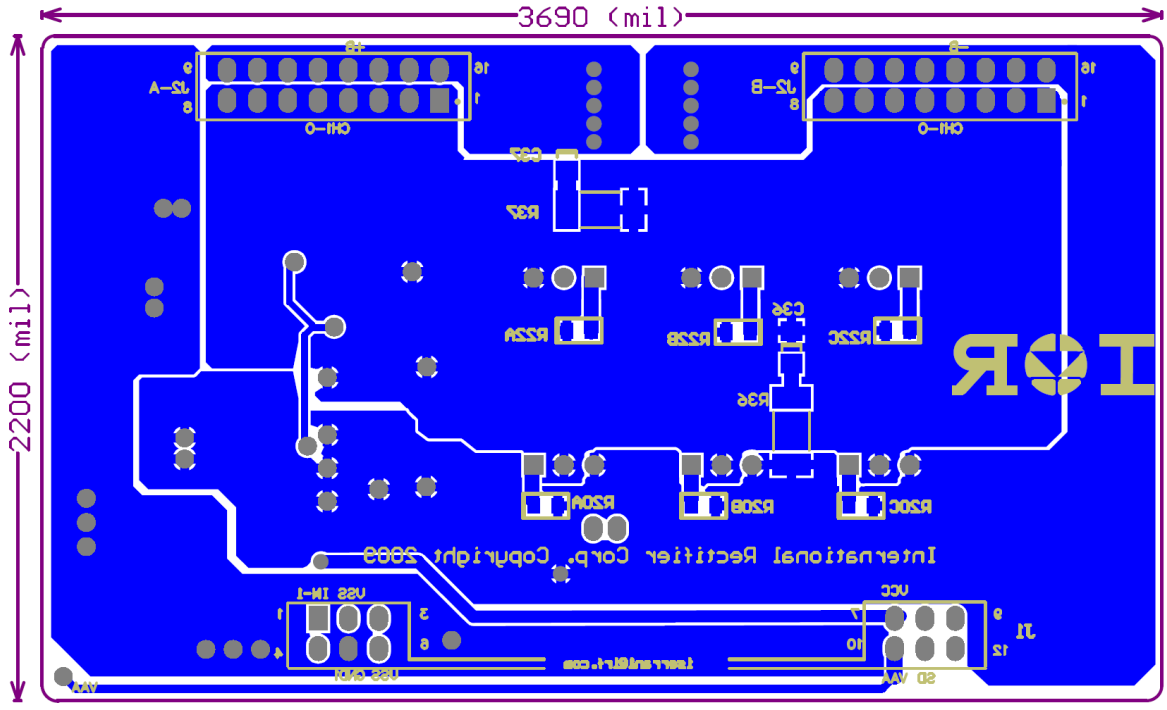

Figure 28 IRAUDAMP9 Daughter board PCB Bottom Layer (Top View)

Revision changes descriptions

Revision	Changes description	Date
Rev D2	Release for pre-production.	Aug, 18 2011
Rev E3	Release for pre-production.	Mar. 18, 2011
Rev 1.0	Release for production.	Mar. 25, 2011
Rev 2.A	1. Preliminary update on Figures 18-24 (pages 23-29). 2. Preliminary updates on Mother board BOM and Daughter board Schematic diagrams & BOM.	Feb. 08, 2012
Rev 2.0	1. Update Figures 18-28 (pages 23-39) and add text for OCP calculation. 2.1 Change values in Daughter Board Schematic Diagram and BOM (DT :R5, R13, Hi-OCP R43/R41, Lo-OCP R17). 2.2. Add R107 on Daughter Board's OTP circuit. 2.3 Updates on Mother board BOM and Daughter board Schematic diagrams & BOM.	Mar. 18, 2012

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03/25/2011