HVLED002

High performance current mode LED controller

Datasheet - production data

SO-8

Features

- Trimmed oscillator for precise frequency control
- Oscillator frequency guaranteed at 250 kHz
- Current mode operation to 500 kHz
- Latching PWM for cycle-by-cycle current limiting
- Internally trimmed reference with undervoltage lockout
- High current totem pole output
- Undervoltage lockout with hysteresis
- Low start-up and operating current

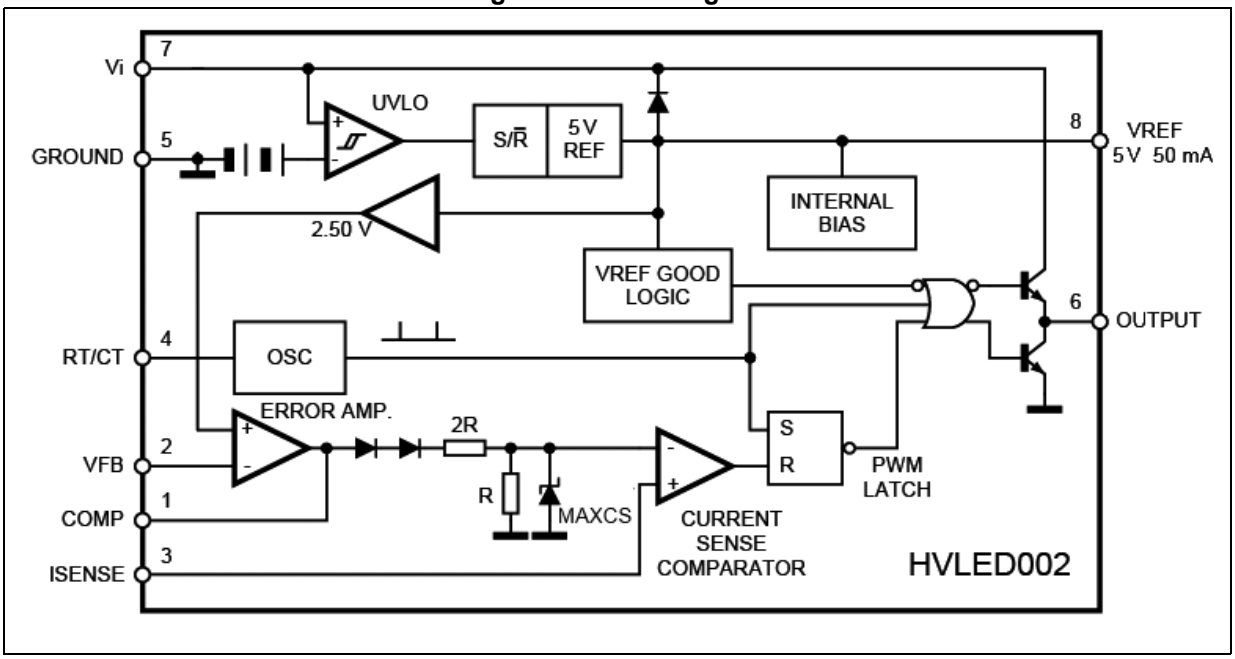
Description

The HVLED002 control IC provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes to implement LED drivers. Internally implemented circuits include a trimmed oscillator for the precise duty cycle control, undervoltage lockout, a precision reference trimmed for accuracy at the error amplifier input, a PWM comparator which also provides current limit control and a totem pole output stage designed to the source or sink high peak current. The output stage, suitable for driving N-channel MOSFETs, is low in the off-state.

Table 1. Device summary

Order codes	Package	Packaging
HVLED002	SO8	Tube
HVLED002TR		Tape and reel

Figure 1. Block diagram



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1 Absolute maximum ratings

Table 2. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_i	Supply voltage	30	V
I_O	Output current	± 1	A
E_O	Output energy (capacitive load)	5	µJ
	Analog inputs (pins 2, 3)	- 0.3 to 5.5	V
	Error amplifier output sink current	10	mA

1. All voltages are with respect to the pin 5, all currents are positive into the specified terminal.

2 Pin connection and functions

Figure 2. Pin connection (top view)

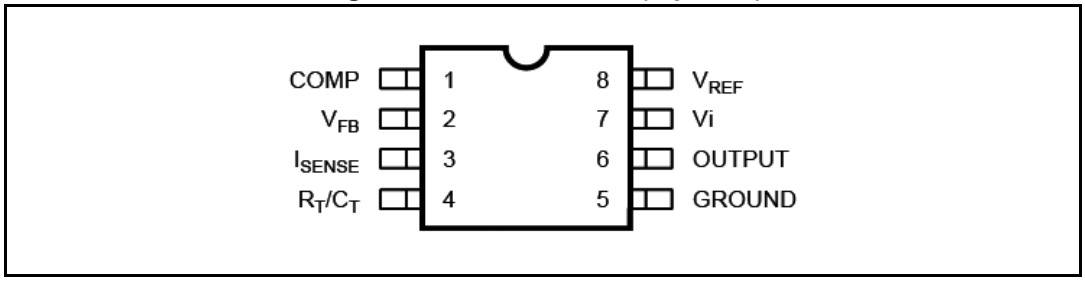


Table 3. Pin functions

No.	Function	Description
1	COMP	This pin is the error amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the error amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum output duty cycle are programmed by the connecting resistor R_T to V_{REF} and the capacitor C_T to ground. An operation to 500 kHz is possible.
5	GROUND	This pin is the ground reference of the device.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
7	V_i	This pin is the positive supply of the control IC.
8	V_{REF}	This is the reference output. It provides the charging current for the capacitor C_T through the resistor R_T.

3 Thermal data

Table 4. Thermal data

Symbol	Description	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	150	°C/W
T_{stg}	Storage temperature range	-65 to 150	°C
T_J	Junction operating temperature	-40 to 150	°C
T_L	Lead temperature (soldering 10 s)	300	°C

4 Electrical characteristics

Unless otherwise stated, these specifications apply for 0 ≤ T_{amb} ≤ 85 °C; V_i = 15 V; R_T = 10 KΩ; C_T = 3.3 nF[a].

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V_i	Max. operative volt.				25	V
REFERENCE SECTION						
V_{REF}	Output voltage	T_J = 25 °C, I_o = 1 mA	4.95	5.00	5.05	V
ΔV_{REF}	Line regulation	12 V ≤ Vi ≤ 25 V		2	20	mV
ΔV_{REF}	Load regulation	1 ≤ I_o ≤ 20 mA		3	25	mV
$\Delta V_{REF}/\Delta T$	Temperature stability	(1)		0.2		mV/°C
	Total output variation	Line, load, temperature	4.82		5.18	V
e_N	Output noise voltage	10 Hz ≤ f ≤ 10 KHz, T_j = 25 °C(1)		50		µV
	Long term stability	T_{amb} = 125 °C, 1000 hrs(1)		5	25	mV
I_{SC}	Output short-circuit		-30	-100	-180	mA
OSCILLATOR SECTION						
f_{OSC}	Frequency	T_J = 25 °C T_A = 0 to 85 °C T_J = 25 °C (R_T = 6.2 kΩ, C_T = 1 nF)	49 48 225	52 - 250	55 56 275	KHz
$\Delta f_{OSC}/\Delta V$	Frequency change with volt.	V_{CC} = 12 V to 25 V	-	0.2	1	%
$\Delta f_{OSC}/\Delta T$	Frequency change with temp.	T_{amb} = 0 °C to 85 °C	-	0.5	-	%
V_{OSC}	Oscillator voltage swing	Peak-to-peak	-	1.6	-	V
I_{dischg}	Discharge current (V_{OSC} = 2 V)	T_J = 25 °C	7.8	8.3	8.8	mA
		T_A = 0°C to 85°C	7.6	-	8.8	mA
ERROR AMPLIFIER SECTION						
$V_{REF,EA}$	Input voltage	$V_{(COMP)}$ = 2.5 V	2.42	2.50	2.58	V
I_b	Input bias current	V_{FB} = 5 V		-0.1	-2	µA
	A_{VOL}	2 V ≤ V_o ≤ 4 V	65	90		dB
BW	Unity gain bandwidth	T_J = 25 °C(1)	0.7	1		MHz
PSRR	Power supply reject. ratio	12 V ≤ V_i ≤ 25 V	60	70		dB
I_o	Output sink current	$V_{(VFB)}$ = 2.7 V, $V_{(COMP)}$ = 1.1 V	2	12		mA

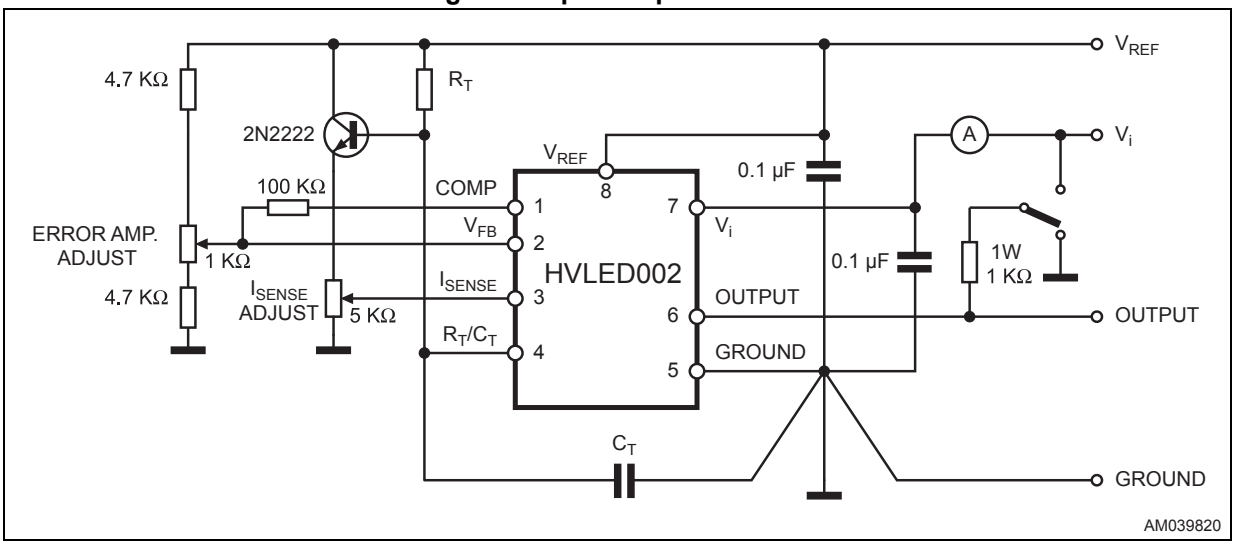
a. Max. package power dissipation limits must be respected; low duty cycle pulse techniques are used during the test maintaining T_J as close to T_{amb} as possible.

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Io	Output source current	$V_{(VFB)}$ = 2.3 V, $V_{(COMP)}$ = 5 V	-0.5	-1		mA
	V_{COMP} high	$V_{(VFB)}$ = 2.3 V; R_L = 15 KΩ between COMP and ground	5	6.2		V
	VCOMP low	$V_{(VFB)}$ = 2.7 V; R_L = 15 KΩ between COMP and VREF		0.8	1.1	V
CURRENT SENSE SECTION						
G_V	Gain	(2), (3)		3		V/V
MAXCS	Maximum input signal	$V_{(COMP)}$ = 5.6 V	258	267	276	mV
SVR	Supply voltage rejection	12 ≤ Vi ≤ 25 V(1)		70		dB
I_b	Input bias current			-2	-10	µA
	Delay to output			150	300	ns
OUTPUT SECTION						
V_{OL}	Output low level	I_{SINK} = 20 mA		0.1	0.4	V
		I_{SINK} = 200 mA		1.6	2.2	V
V_{OH}	Output high level	I_{SOURCE} = 20 mA	13	13.5		V
		I_{SOURCE} = 200 mA	12	13.5		V
V_{OLS}	UVLO saturation	VCC = 6 V; I_{SINK} = 1 mA		0.1	1.1	V
t_r	Rise time	T_J = 25 °C; C_L = 1 nF(1)		50	150	ns
t_f	Fall time	T_J = 25 °C; C_L = 1 nF(1)		50	150	ns
UNDERVOLTAGE LOCKOUT SECTION						
V_{ON}	Start threshold	Increasing voltage	7.8	8.4	9.0	V
V_{OFF}	Min. operating voltage after turn-on	Decreasing voltage	7.0	7.6	8.2	V
PWM SECTION						
	Maximum duty cycle		94	96	100	%
	Minimum duty cycle				0	%
TOTAL STANDBY CURRENT						
I_{st}	Start-up current			0.3	0.5	mA
I_i	Operating supply current	$V_{(VFB)}$ = $V_{(COMP)}$ = 0 V		12	17	mA

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at the trip point of the latch with $V_{(VFB)}$ = 0.
3. Gain defined as : A = $\Delta V_{(COMP)}/\Delta V_{(ISENSE)}$; 0 ≤ $V_{(ISENSE)}$ ≤ 267 mV.

Figure 3. Open loop test circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to the pin 3.

Figure 4. Timing resistor vs. oscillator frequency

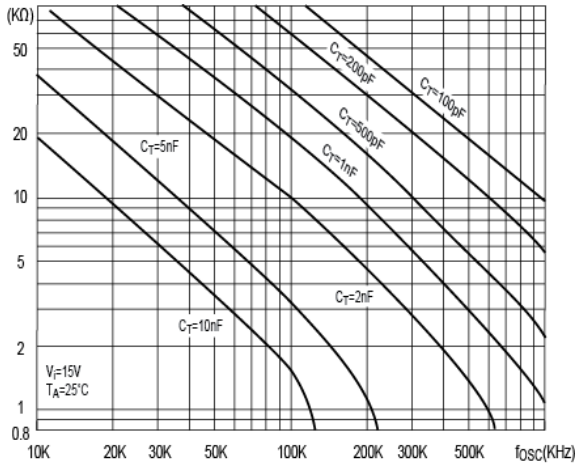


Figure 5. Output deadtime vs. oscillator frequency

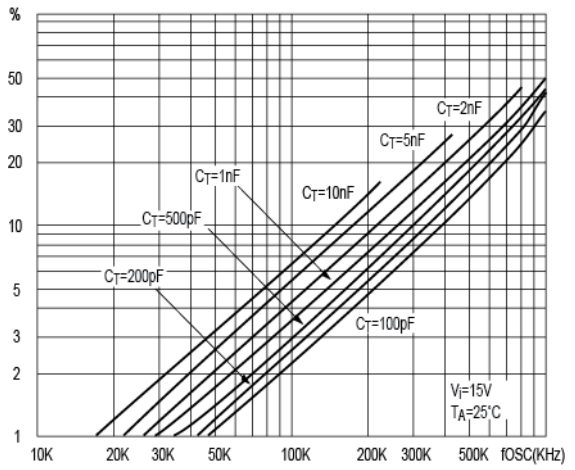


Figure 6. Oscillator discharge current vs. temperature

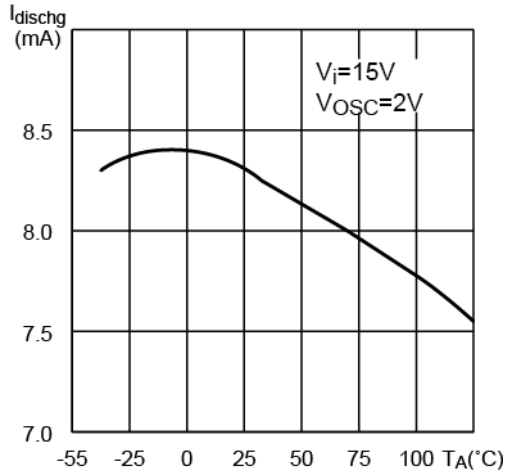


Figure 7. Maximum output duty cycle vs. timing resistor

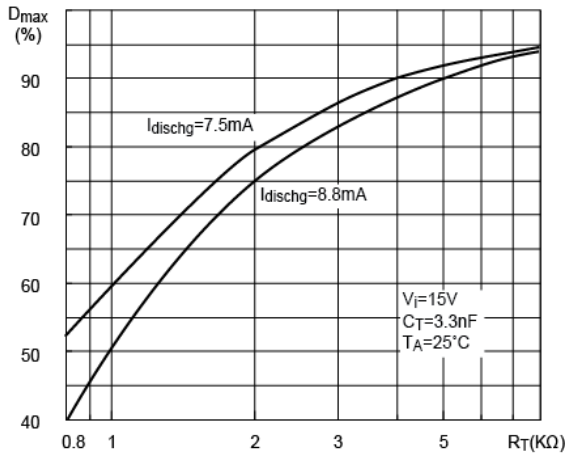


Figure 8. Error amplifier open loop gain and phase vs. frequency

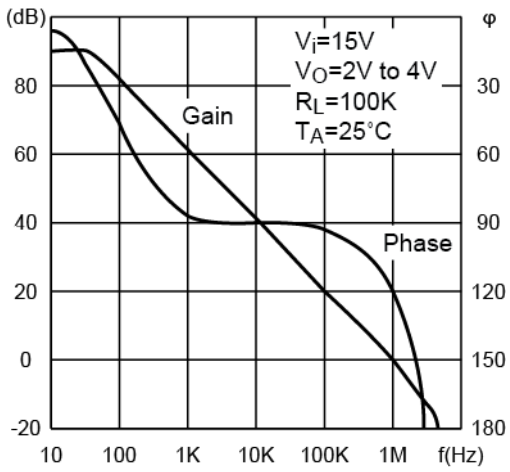


Figure 9. Current sense input threshold vs. error amplifier output voltage

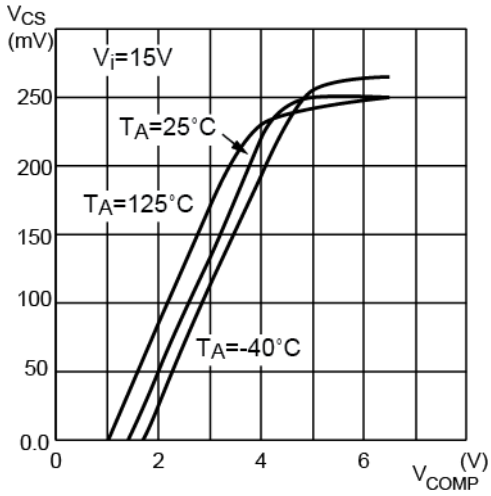


Figure 10. Reference voltage change vs. source current

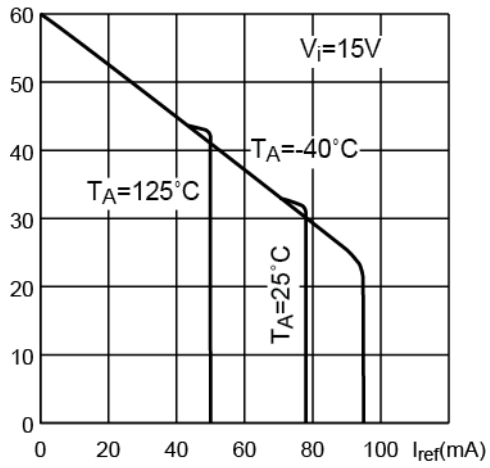


Figure 11. Reference short-circuit current vs. temperature

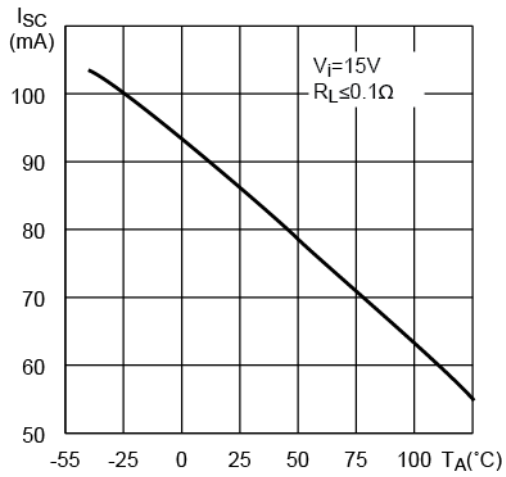


Figure 12. Output saturation voltage vs. load current

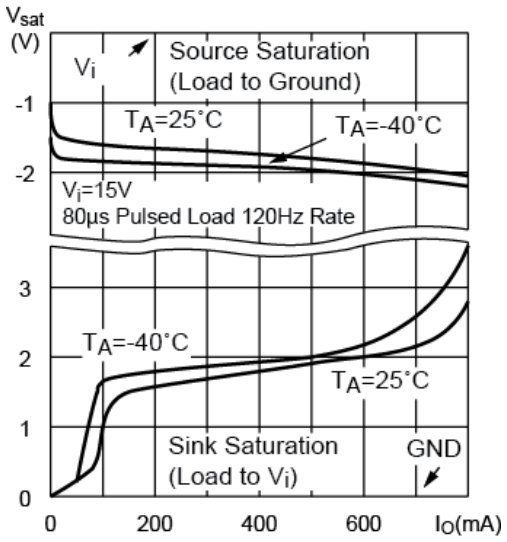


Figure 13. Supply current vs. supply voltage

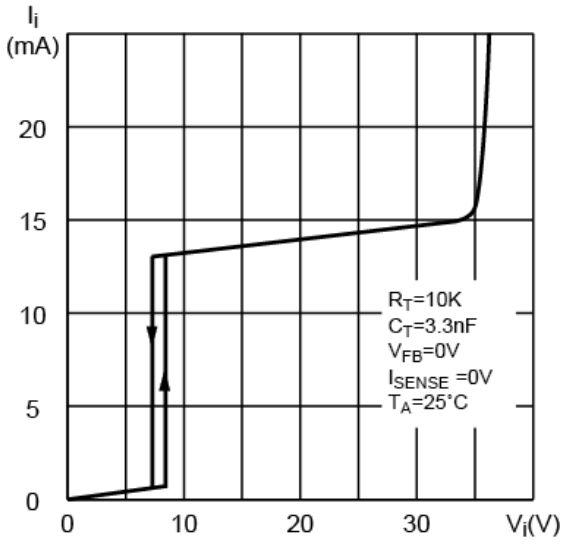


Figure 14. Oscillator and output waveforms

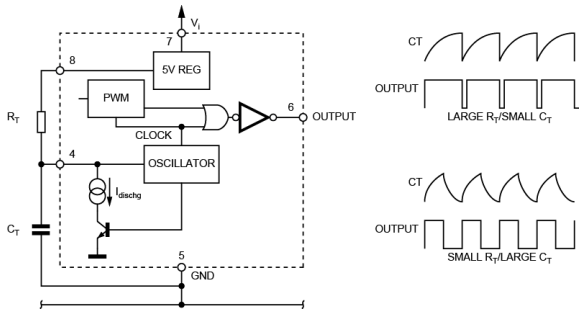


Figure 15. Error amplifier configuration

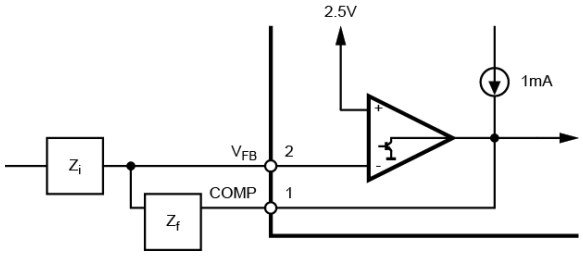


Figure 16. Undervoltage lockout

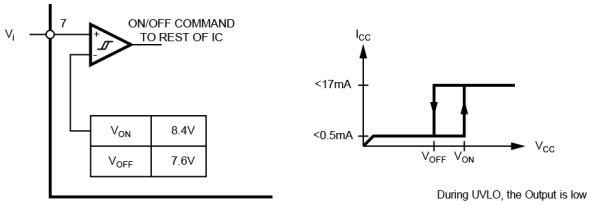


Figure 17. Current sense circuit

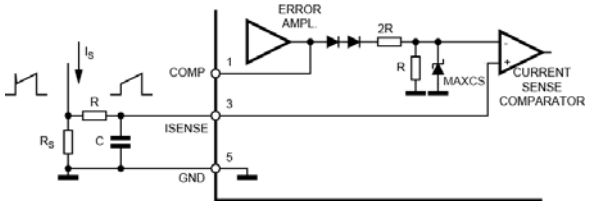


Figure 18. Soft-start circuit

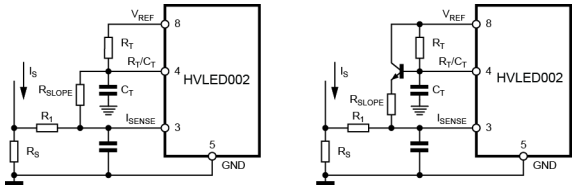
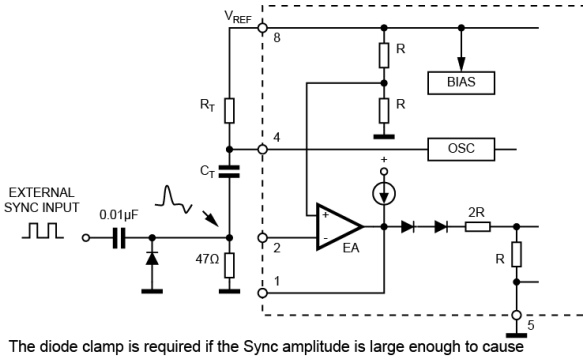
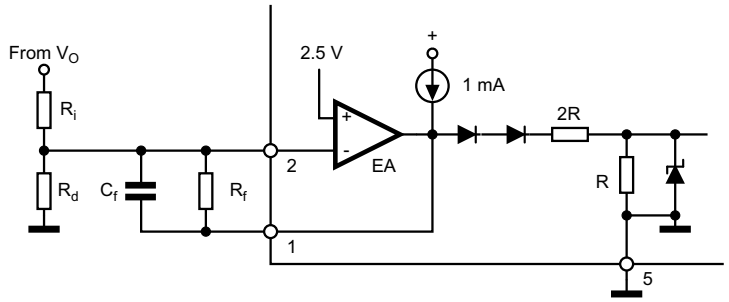


Figure 19. External clock synchronization

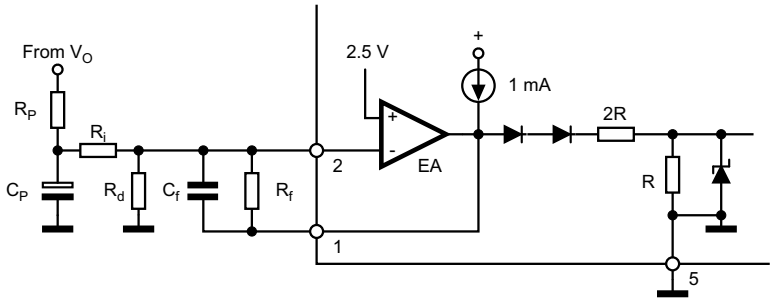


The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300mV below ground

Figure 20. Error amplifier compensation



Error amplifier compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error amplifier compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

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5 Application information

5.1 Supply voltage and undervoltage lockout

The HVLED002 device is able to operate with a very wide range of supply voltage between 8.4 V and 30 V. The UVLO circuit insures that VCC is adequate to make the HVLED002 fully operational before enabling the output stage. *Figure 16* shows that the UVLO turn-on and turn-off thresholds are fixed internally at 8.4 V and 7.6 V respectively. The hysteresis prevents V_{CC} oscillations during power sequencing and the start-up current is less than 1 mA.

During UVLO, the output driver is in a low state and it can easily sink 1 mA, enough to insure the MOSFET is held off.

5.2 Reference voltage

The HVLED002 contains a precision reference voltage (5 V) that generates all the internal reference voltages such as the error amplifier's reference (connected to its non-inverting input), current sense clamp limit (MAXCS) and oscillator's internal bias currents and thresholds.

The reference voltage is also available on the VREF pin that, thanks to its high output current capability (over 20 mA), is able to supply not only nearby passive circuitries but also auxiliary microcontrollers.

The pin must be bypassed with at least a 0.1 µF ceramic capacitor placed as close as possible to the respective VREF and GND pins.

5.3 Oscillator

The HVLED002 oscillator is programmed as shown in *Figure 14*. The timing capacitor CT is charged from a reference voltage (e.g.: VREF) through the timing resistor RT, and discharged by an internal current source.

The MOSFET is turned on (GD pin high) when the oscillator starts the charge of the CT. As soon as the voltage of the CT reaches an upper threshold the internal discharge current is activated until the CT voltage reaches a lower threshold. This occurrence initiates a new oscillator cycle.

The difference between the upper and the lower thresholds (Vosc) determines the duration of charging and discharging time. During the discharging time (also called deadtime) the MOSFET is off and any spurious GD triggering is avoided. The deadtime also limits the maximum obtainable duty cycle.

The oscillator can be differently connected to external circuitry to obtain different operating schemes. Connecting the RT to VREF a very accurate fixed frequency operation is achieved: the RT,CT combinations are plot into *Figure 5 on page 8*, *Figure 6* and *Figure 8* for a quick reference, or calculated as follows:

Equation 1

$$FOSC\ (kHz) = 1.72 / [RT\ (k\Omega) \times CT\ (\mu F)]$$

Connecting the RT to a variable voltage, dependency of the operating frequency on said voltage is introduced. A pull-down switch can be used to reset the CT during the MOSFET's on time, for example to operate in fixed off time. A synchronous operation is also possible using circuitries like the one proposed as an example in *Figure 19*. The HVLED002 oscillator can be used to a maximum of 500 kHz.

5.4 Current sense

The peak current mode operation of the HVLED002 is made by the embedded current sense comparator: the said element turns off the MOSFET as soon as the current sense input voltage is greater than the internal threshold derived by the COMP pin voltage (*Figure 17*).

The current sense pin (ISENSE) is normally connected to a shunt resistor, put in series with the main switch, but different connections are also possible.

Under the normal operation the threshold voltage (VCS) is controlled by the E/A according to the following relation:

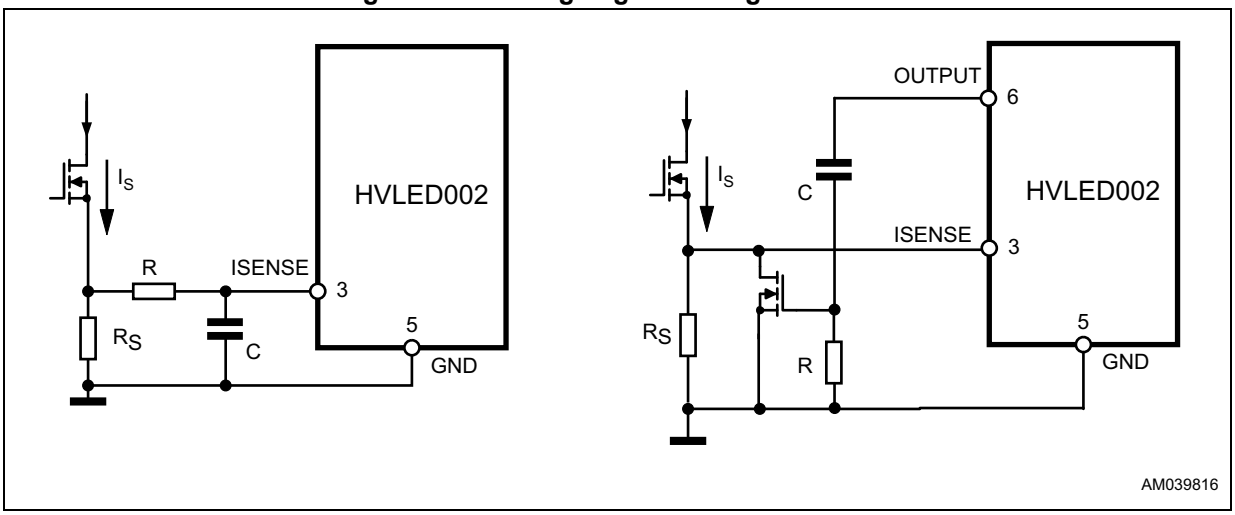
Equation 2

$$VCS = 1/3 * (VCOMP - 1.4\ V)$$

VCS is upper limited to MAXCS to reduce the shunt resistor power dissipation without the need of current transformers or offsets circuitries. This parameter is beneficial in those applications where both the peak current accuracy and the operating power dissipation are critical aspects (e.g.: LED secondary side LED current regulators).

When the sensing current resistor is in series with the power switch, the current waveform will often have a large spike at its leading edge due to parasitic capacitances and gate driver charging currents. A very simple leading edge blanking (LEB) circuit consists on an RC filter, but more effective active circuitries are also possible.

Figure 21. Leading edge blanking circuitries

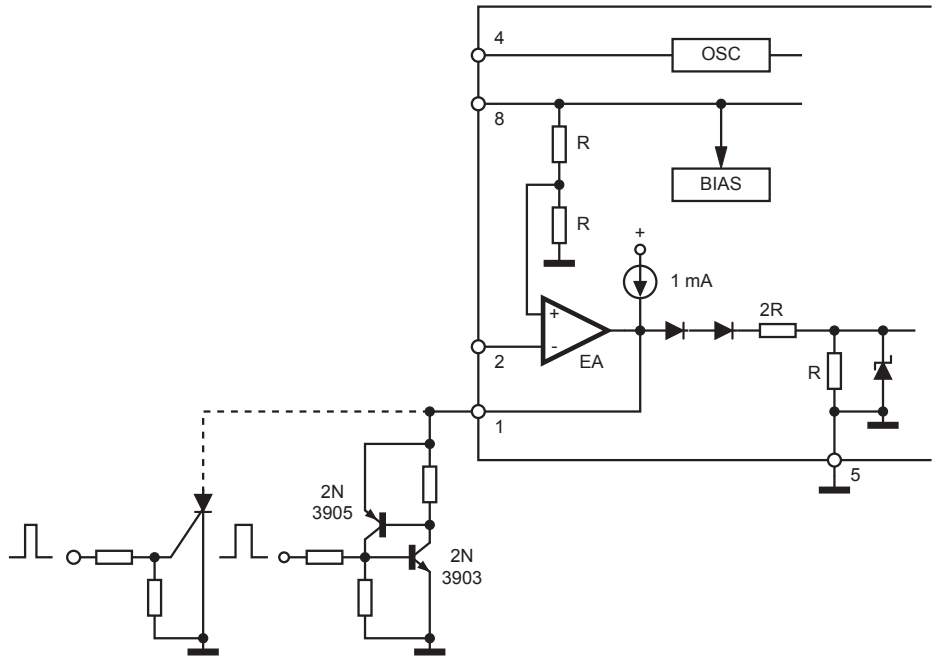


5.5 Error amplifier

An error amplifier (E/A) structure is present in the HVLED002 (*Figure 15 on page 10*). The non-inverting input is internally connected to a very precise reference voltage (2.5 V ± 2%). The E/A output and inverting pin are connected respectively to the pin 1 and 2, available for external compensation. The E/A output will source at least 0.5 mA and sink 2 mA. *Figure 8 on page 9* shows the open loop frequency response of the E/A.

The output of the error amplifier can be forced to ground in different ways to shut down the application as shown in *Figure 22*.

Figure 22. Shutdown circuitries



The SCR must be selected for a holding current of less than 0.5 mA at $T_{A(min)}$.
The simple two-transistor circuit can be used in place of the SCR as shown. All resistors are 10 KΩ.

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5.6 Totem pole output

The HVLED002 has a single totem pole output which can be operated to the ± 1 Amp peak current for driving MOSFET gates, and a + 200 mA average current for bipolar power transistors.

Cross conduction between the driver's output transistors is minimal, the average added power with VIN = 30 V is around 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem pole output and the gate of the MOSFET. Without this resistor, the peak current is limited only by the dV/dT rate of the totem pole switching and the FET gate capacitance.

An additional discharging diode can be put in parallel with the said limiting resistor to quickly turn off the MOSFET, reducing the switching losses and the control to output delay.

5.7 Typical application

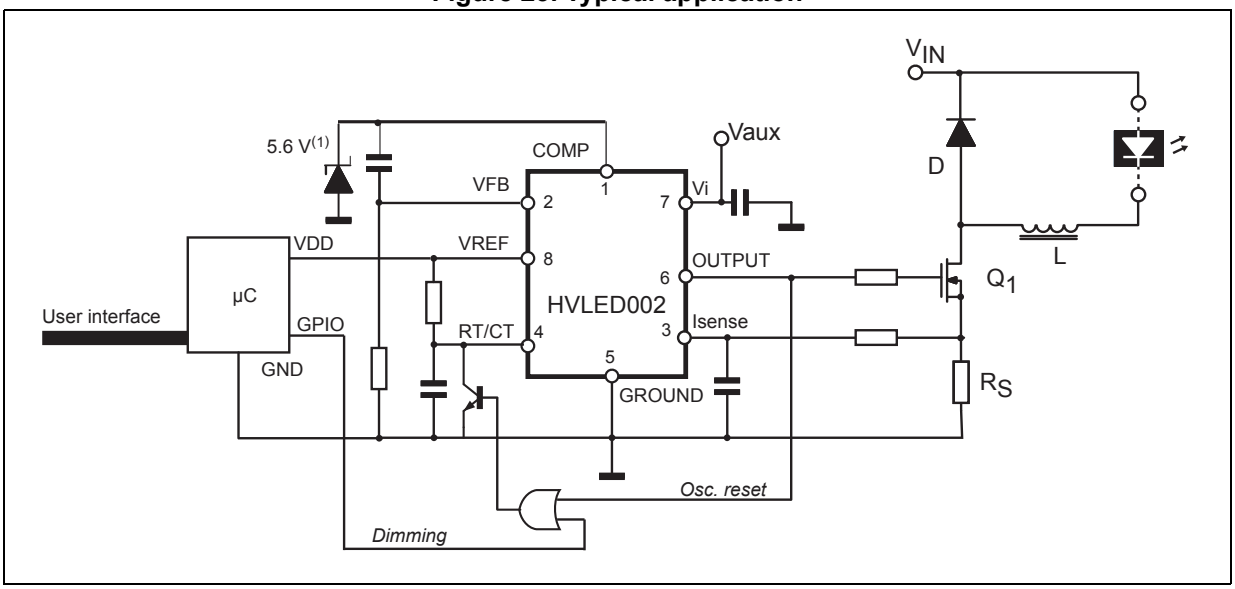
The HVLED002 device can be used as a secondary side step-down current regulator in the multiple staged LED driver - see *Figure 23*. It is easy to configure the device to drive an inverse (or modified) buck topology based on the fixed off-time (FOT) algorithm.

The MOSFET remains on until the current sense threshold is reached; during the on time, the oscillator remains reset to ground. The current sense threshold is set by the saturation of the E/A to MAXCS to guarantee the higher precision as possible.

The MOSFET is then turned off and the oscillator is released: the resulting off time is fixed by the charging of the CT by RT, connected to VREF.

An optional auxiliary microcontroller, supplied by VREF itself can be used to dim the LED current according to the information sent to the application by a remote controller.

Figure 23. Typical application



1. Optional for better performances.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 SO-8 package information

Figure 24. SO-8 package outline

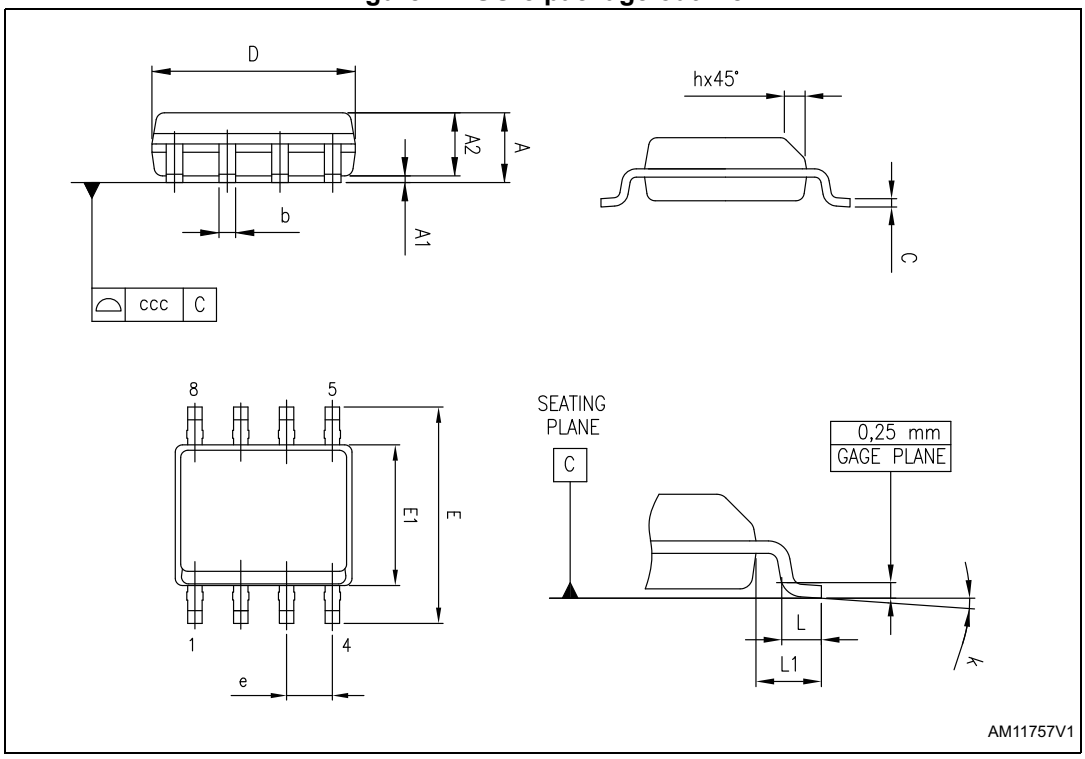


Table 6. SO-8 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D(1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.10			0.0039

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. Dimension “E1” does not include interlead Flash or protrusions. Interlead Flash or protrusions shall not exceed 0.25 mm per side.

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
15-Dec-2015	1	Initial release.