



# BUK965R8-100E

N-channel TrenchMOS logic level FET

28 July 2016

Product data sheet

## 1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{Gst(th)}$  rating of greater than 0.5V at 175 °C

## 3. Applications

- 12V, 24V and 48V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

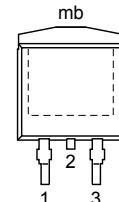
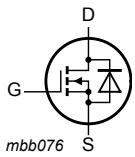
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$		-	-	100	V
$I_D$	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>		-	-	349	W
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>		-	4.62	5.8	$\text{m}\Omega$
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 80 \text{ V}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	51	-	nC

[1] Continuous current is limited by package.

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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain	 D2PAK (SOT404)	

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK965R8-100E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK965R8-100E	BUK965R8-100E

## 8. Limiting values

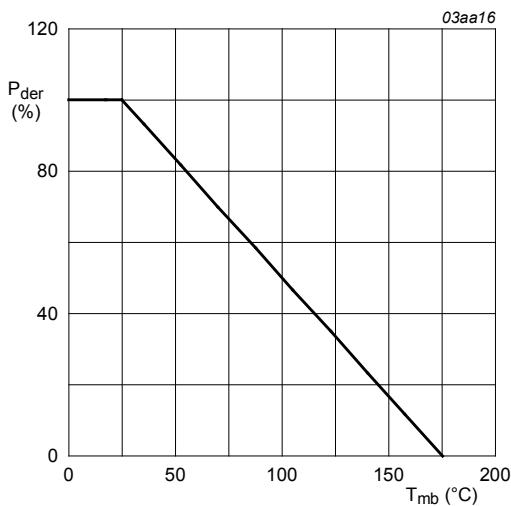
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}$ ; $T_j \leq 175^\circ\text{C}$		-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	100	V
$V_{GS}$	gate-source voltage	$T_j \leq 175^\circ\text{C}$ ; DC		-10	10	V
		$T_j \leq 175^\circ\text{C}$ ; Pulsed	[1][2]	-15	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; Fig. 1		-	349	W
$I_D$	drain current	$T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 2	[3]	-	120	A
		$T_{mb} = 100^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 2		-	105	A
$I_{DM}$	peak drain current	$T_{mb} = 25^\circ\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 3		-	591	A
$T_{stg}$	storage temperature			-55	175	°C

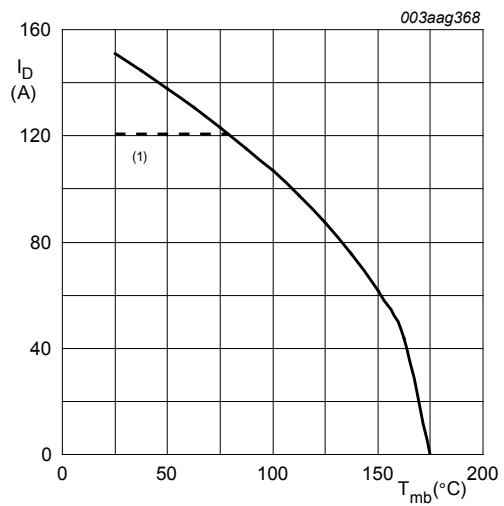
Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[3]	-	120	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 µs; T <sub>mb</sub> = 25 °C		-	591	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; Fig. 4	[4][5]	-	385	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}C)} \times 100 \%$$



**Fig. 2. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 5 \text{ V}$$

(1) Capped at 120 A due to package.

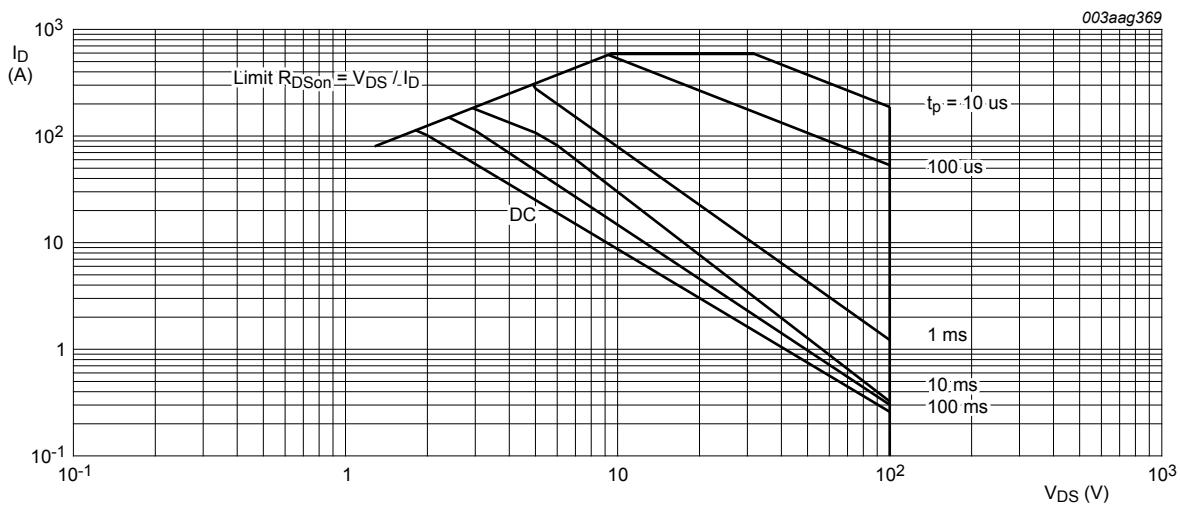


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is a single pulse

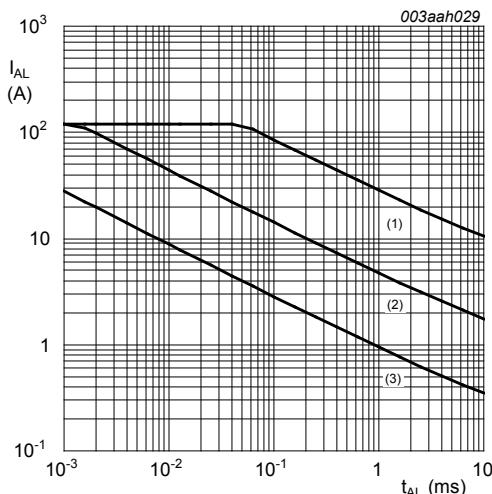


Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

(1)  $T_j(\text{init}) = 25^\circ\text{C}$ ; (2)  $T_j(\text{init}) = 150^\circ\text{C}$ ; (3) Repetitive Avalanche

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	0.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

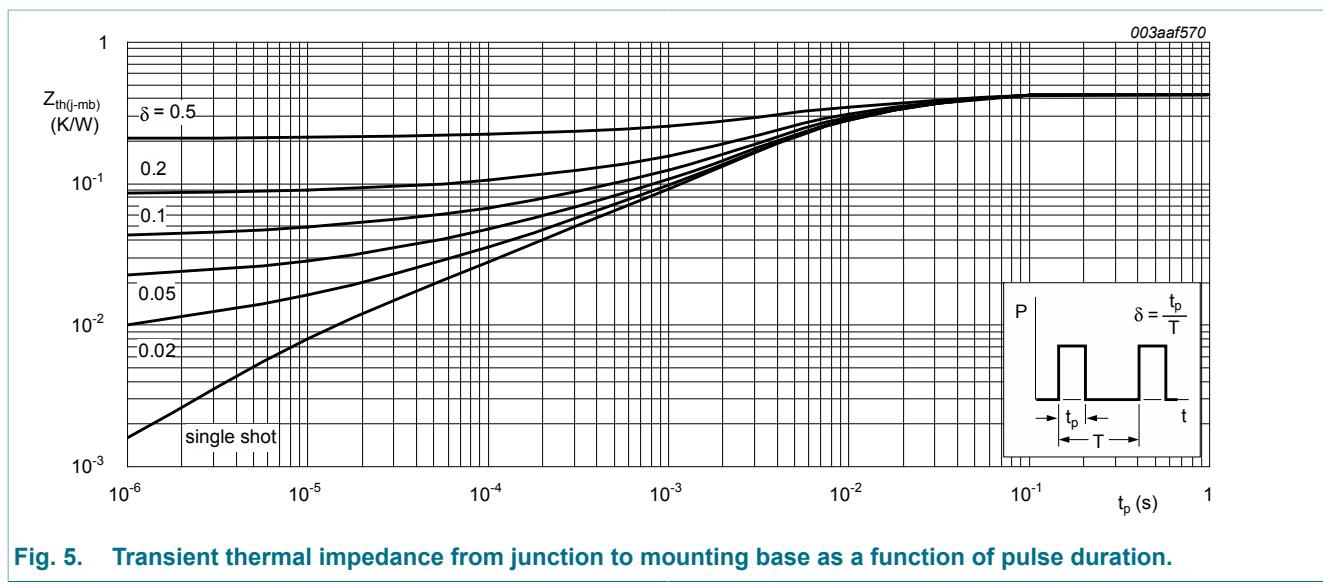


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 10. Characteristics

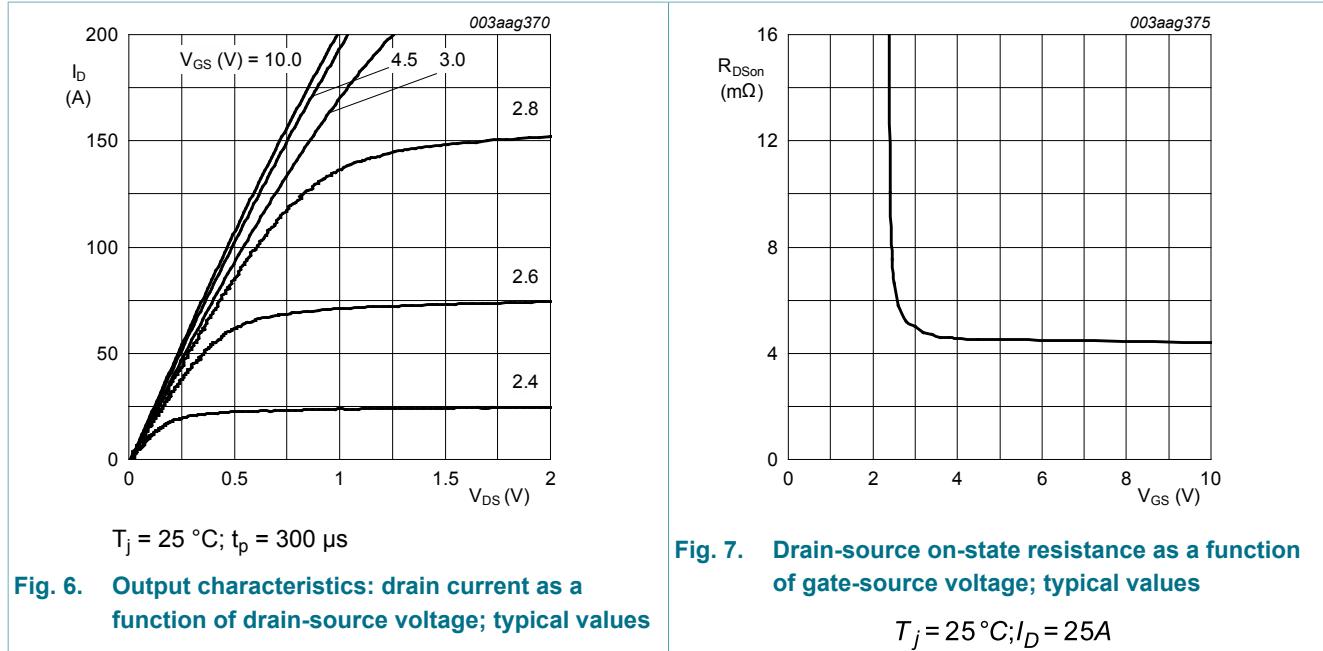
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		100	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>		-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>		0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	0.05	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$		-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>		-	4.62	5.8	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>		-	4.45	5.6	$\text{m}\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 11</a>		-	-	16	$\text{m}\Omega$
<b>Dynamic characteristics</b>							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	133	-	nC
$Q_{GS}$	gate-source charge			-	23	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GD}$	gate-drain charge			-	51	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25^\circ \text{C}$ ; <a href="#">Fig. 15</a>		-	13100	17460	pF
$C_{oss}$	output capacitance			-	725	870	pF
$C_{rss}$	reverse transfer capacitance			-	450	620	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80 \text{ V}; R_L = 3.2 \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 5 \Omega$		-	81	-	ns
$t_r$	rise time			-	168	-	ns
$t_{d(off)}$	turn-off delay time			-	237	-	ns
$t_f$	fall time			-	148	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH

**Source-drain diode**

$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ \text{C}$ ; <a href="#">Fig. 16</a>		-	0.77	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}$		-	70	-	ns
$Q_r$	recovered charge			-	202	-	nC



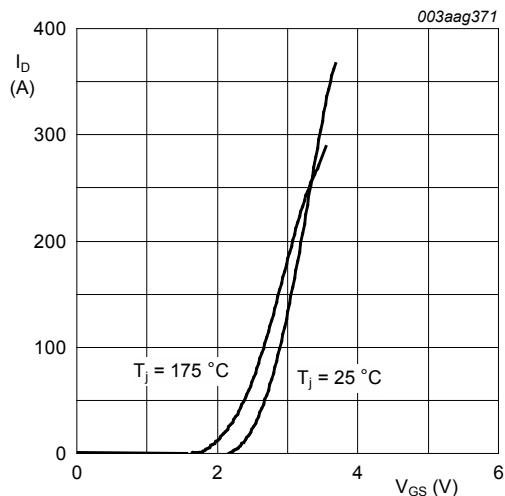


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 12\text{V}$

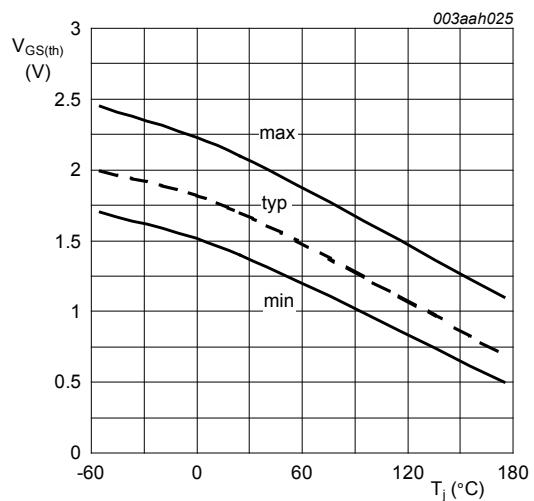


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

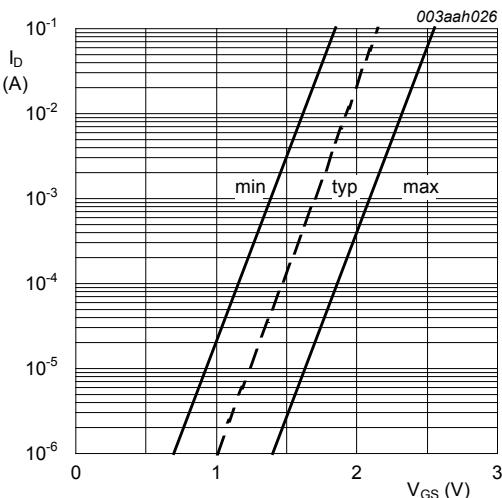
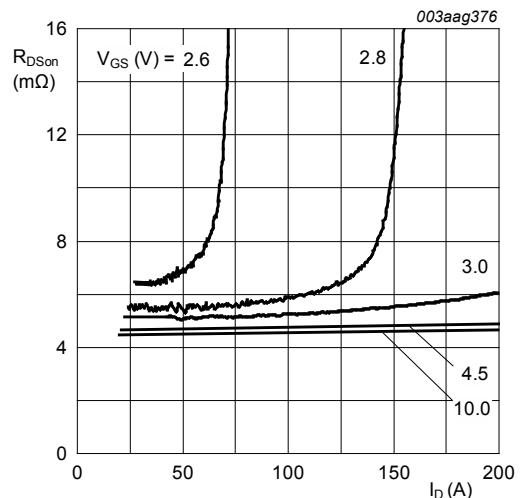


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}$ ;  $V_{DS} = 5\text{V}$



$T_j = 25^\circ\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

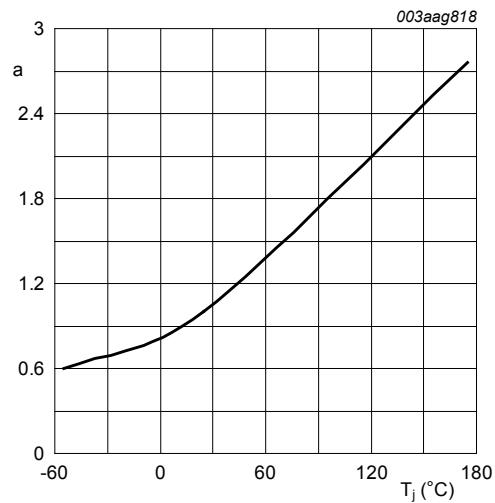
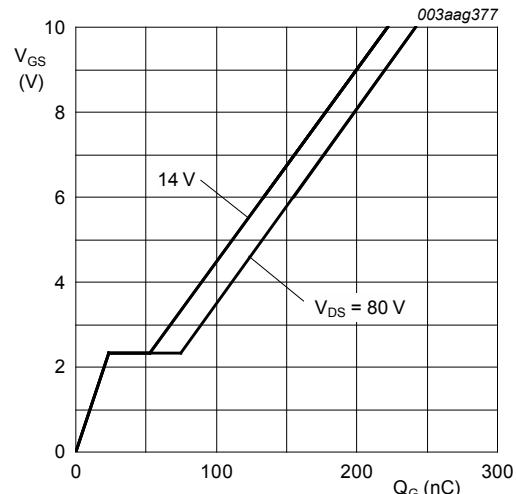


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$



$T_j = 25^{\circ}\text{C}$ ;  $I_D = 25$  A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

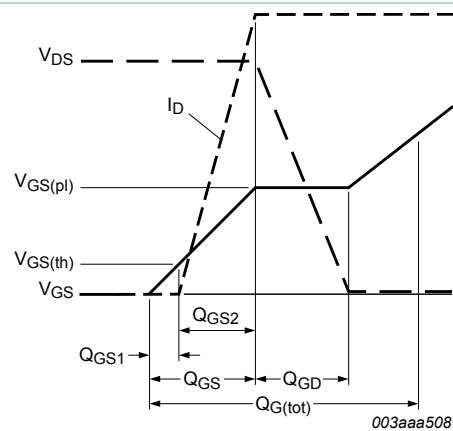
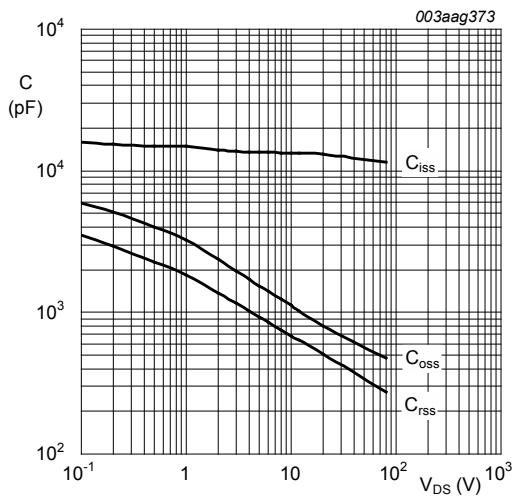
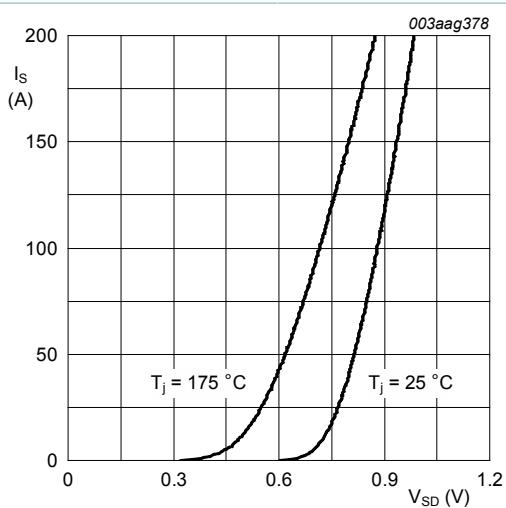


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0$  V;  $f = 1$  MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 11. Package outline

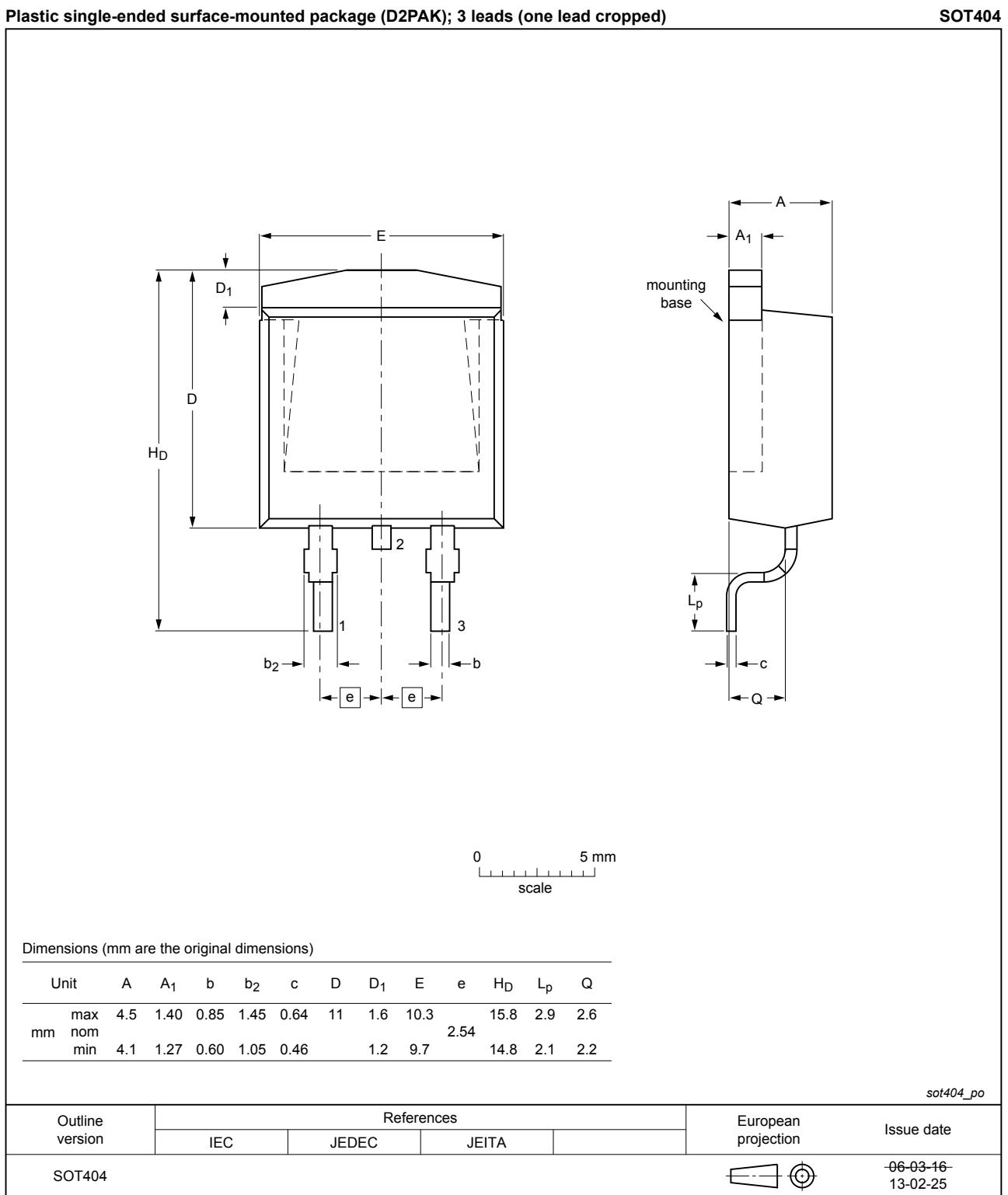


Fig. 17. Package outline D2PAK (SOT404)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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## 13. Contents

1	General description .....	1
2	Features and benefits .....	1
3	Applications .....	1
4	Quick reference data .....	1
5	Pinning information .....	2
6	Ordering information .....	2
7	Marking .....	2
8	Limiting values .....	2
9	Thermal characteristics .....	4
10	Characteristics .....	5
11	Package outline .....	10
12	Legal information .....	11
12.1	Data sheet status .....	11
12.2	Definitions .....	11
12.3	Disclaimers .....	11
12.4	Trademarks .....	12

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