LTC2185, LTC2184, LTC2183, LTC2182, LTC2181, LTC2180, LTC2188, LTC2145-14/-12, LTC2144-14/-12, LTC2143-14/-12, LTC2142-14/-12, LTC2141-14/-12, LTC2140-14/-12, LTC2270: 16-/14-/12-Bit, 20Msps to 125Msps Dual ADCs

DESCRIPTION

Demonstration circuit 1620A supports a family of 16-/14-/12-bit, 20Msps to 125Msps ADCs. Each assembly features one of the following devices: LTC®2185, LTC2184, LTC2183, LTC2182, LTC2181, LTC2180, LTC2188, LTC2145-14, LTC2144-14, LTC2143-14, LTC2142-14, LTC2141-14, LTC2140-14, LTC2145-12, LTC2144-12, LTC2143-12, LTC2142-12, LTC2141-12, or LTC2140-12, LTC2270 high speed, high dynamic range ADCs.

Demonstration circuit 1620A supports the LTC2185/ LTC2145 family DDR LVDS output mode.

The versions of the 1620A demo board supporting the LTC2185 and LTC2145 series of A/D converters are listed in Table 1. Depending on the required resolution and sample rate, the DC1620A is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 70MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

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Table 1. DC1620 Variants

DC1620 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1620A-A	LTC2185	16-Bit	125Msps	5MHz to 140MHz
1620A-B	LTC2184	16-Bit	105Msps	5MHz to 140MHz
1620A-C	LTC2183	16-Bit	80Msps	5MHz to 140MHz
1620A-D	LTC2182	16-Bit	65Msps	5MHz to 140MHz
1620A-E	LTC2181	16-Bit	40Msps	5MHz to 140MHz
1620A-F	LTC2180	16-Bit	25Msps	5MHz to 140MHz
1620A-G	LTC2145-14	14-Bit	125Msps	5MHz to 140MHz
1620A-H	LTC2144-14	14-Bit	105Msps	5MHz to 140MHz
1620A-I	LTC2143-14	14-Bit	80Msps	5MHz to 140MHz
1620A-J	LTC2142-14	14-Bit	65Msps	5MHz to 140MHz
1620A-K	LTC2141-14	14-Bit	40Msps	5MHz to 140MHz
1620A-L	LTC2140-14	14-Bit	25Msps	5MHz to 140MHz
1620A-M	LTC2145-12	12-Bit	125Msps	5MHz to 140MHz
1620A-N	LTC2144-12	12-Bit	105Msps	5MHz to 140MHz
1620A-O	LTC2143-12	12-Bit	80Msps	5MHz to 140MHz
1620A-P	LTC2142-12	12-Bit	65Msps	5MHz to 140MHz
1620A-Q	LTC2141-12	12-Bit	40Msps	5MHz to 140MHz
1620A-R	LTC2140-12	12-Bit	25Msps	5MHz to 140MHz
1620A-S	LTC2188	16-Bit	20Msps	5MHz to 140MHz
1620A-T	LTC2270	16-Bit	20Msps	5MHz to 140MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage—DC1620A	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 500mA	Optimized for 4.5V [4.5V □ 6.0V Min/Max]
Analog Input Range	Depending on SENSE Pin Voltage	$1V_{P-P}$ to $2V_{P-P}$
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode)	350mV/1.25V Common Mode
	Minimum Logic Levels (100Ω Load, 3.5mA Mode)	247mV/1.25V Common Mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	Single-Ended Encode Mode (ENC– Tied to GND)	0V to 3.6V
	Differential Encode Mode (ENC– Not Tied to GND)	0.2V to 3.6V
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1620A is easy to set up to evaluate the performance of the LTC2185/LTC2145 A/D converter family. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC890 USB data acquisition and collection system was supplied with the DC1620A demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1620A and to a PC.

DC1620A Demonstration Circuit Board Jumpers

The DC1620A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

JP2-PAR/SER: Selects Parallel or Serial programming mode. (Default: Serial)

JP3-Duty Cycle Stabilizer: Enables/Disable Duty Cycle Stabilizer. (Default: Enable)

JP4-SHDN: Enables and disables the LTC2185/LTC2145. (Default: Enable)

JP5-NAP: Enables and disables NAP mode (Default: disable)

JP6-LVDS/CMOS: Selects between LVDS and CMOS output signaling. (Default: LVDS)

Applying Power and Signals to the DC1620A Demonstration Circuit

If a DC890 is used to acquire data from the DC1620A, the DC890 must **first** be connected to a powered USB port or provided an external 6V to 9V **before** applying +4.5V to +6.0V across the pins marked V+ and GND on the DC1620A. DC1620A requires 4.5V for proper operation. Regulators on the board produce the voltages required for the ADC. The DC1620A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC890 data collection board is powered by the USB cable and does require an external power supply when collecting data from an LVDS demo board. It must be supplied from an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

QUICK START PROCEDURE

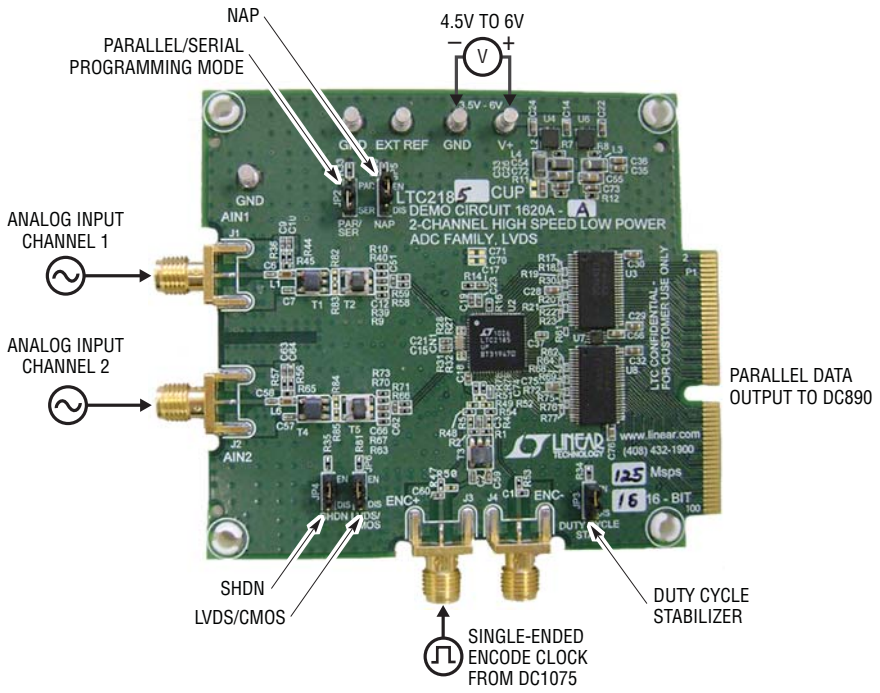


Figure 1. DC1620 Setup (Zoom for Detail)

Analog Input Network

For optimal distortion and noise performance, the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the respective ADC data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz or above 140MHz.

In almost all cases, filters will be required on both analog the input and encode clock to provide data sheet SNR. In the case of the DC1620A a bandpass filter used for the clock should be used prior to the DC1075 clock divider board.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide gain block prior to the final filter. This is particularly true at higher frequencies where IC-based operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Encode Clock

Note: Apply an encode clock to the SMA connector on the DC1620A demonstration circuit board marked J3. As a default, the DC1620A is populated to have a single-ended input.

For the best noise performance, the encode input must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075 that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2185/LTC2145.

QUICK START PROCEDURE

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1620A a bandpass filter used for the clock should be used prior to the DC1075. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

Apply the analog input signal of interest to the SMA connectors on the DC1620A demonstration circuit board marked J5 AIN+. These inputs are capacitive coupled to Balun transformers ETC1-1-13 (lead free part number: MABA007159-000000).

An internally generated conversion clock output is available on J1 which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval™-II data acquisition board using PScope™ software.

Software

The DC890 is controlled by the PScope system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "PScope.exe" is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1620A demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1620A, and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.

Under the Configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options, see Figure 2:

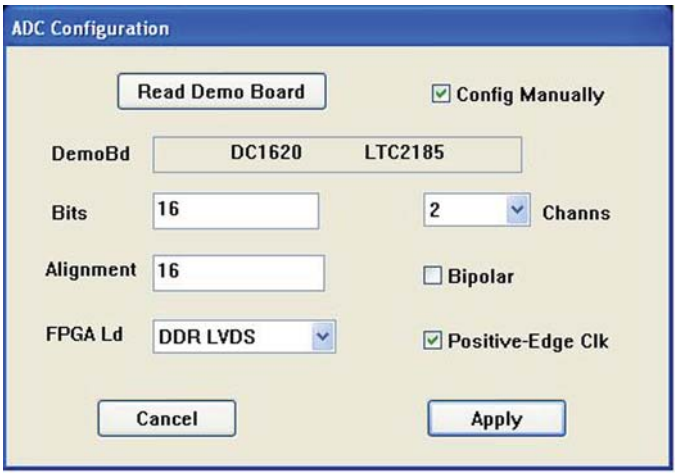


Figure 2: ADC Configuration

Manual configuration settings:

Bits: 16

Alignment: 16

FPGA Ld: DDR LVDS

Channs: 2

Bipolar: Unchecked

Positive-Edge Clk: Checked

If everything is hooked up properly, powered, and a suitable convert clock is present, clicking the Collect button will result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

Serial Programming

PScope has the ability to program the DC1620A board serially through the DC890. There are several options available in the LTC2185 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

QUICK START PROCEDURE

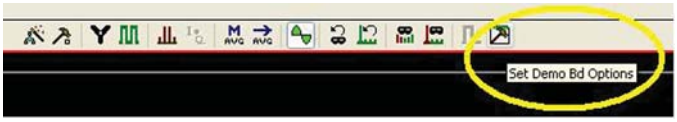


Figure 3: PScope Toolbar

This will bring up the menu shown in Figure 4.

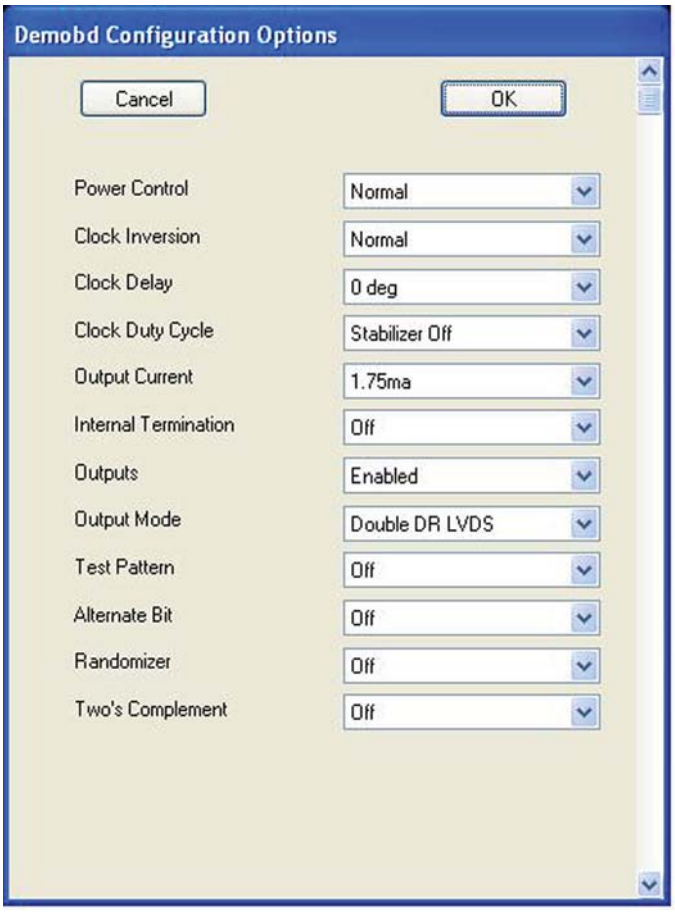


Figure 4: Demobd Configuration Options

This menu allows any of the options available for the LTC2185/LTC2145 family to be programmed serially. The LTC2185/LTC2145 family has the following options:

Power Control: Selects between normal operation, nap and sleep modes.

- Normal (Default) – Entire ADC is powered, and active
- Ch1 Normal Ch2 Nap – Channel 1 remains active while channel 2 is put into nap mode
- Nap – ADC core powers down while references stay active
- Shutdown – The entire ADC is powered down

Clock Inversion: Selects the polarity of the CLKOUT signal.

- Normal (Default) – Normal CLKOUT polarity
- Inverted – CLKOUT polarity is inverted

Clock Delay: Selects the phase delay of the CLKOUT signal.

- None (Default) – No CLKOUT delay
- 45° – CLKOUT delayed by 45°
- 90° – CLKOUT delayed by 90°
- 135° – CLKOUT delayed by 135°

Clock Duty Cycle: Enable or disables Duty Cycle Stabilizer.

- Stabilizer off (Default) – Duty cycle stabilizer disabled
- Stabilizer on – Duty cycle stabilizer enabled

Output Current: Selects the LVDS output drive current.

- 1.75mA (Default) - LVDS output driver current
- 2.1mA – LVDS output driver current
- 2.5mA – LVDS output driver current
- 3.0mA – LVDS output driver current
- 3.5mA – LVDS output driver current
- 4.0mA – LVDS output driver current
- 4.5mA – LVDS output driver current

Internal Termination: Enables LVDS internal termination.

- Off (Default) – Disables internal termination
- On – Enables internal termination

Outputs: Enables digital outputs.

- Enabled (Default) – Enables digital outputs
- Disabled – Disables digital outputs

Output Mode: Selects digital output mode.

- Full Rate – Full rate CMOS output mode (This mode is not supported by the DC1620A)

QUICK START PROCEDURE

- Double LVDS (Default) – double data rate LVDS output mode
- Double CMOS – double data rate CMOS output mode (This mode is not supported by the DC1620A)

Test Pattern: Selects Digital output test patterns.

- Off (Default) – ADC data presented at output
- All out =1 – All digital outputs are 1
- All out = 0 – All digital outputs are 0
- Checkerboard - OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples
- Alternating – Digital outputs alternate between all 1's and all 0's on alternating samples

Alternate Bit: Alternate bit polarity (ABP) Mode.

- Off (Default) – Disables alternate bit polarity
- On – Enables alternate bit polarity (before enabling ABP, be sure the part is in offset binary mode)

Randomizer: Enables data output randomizer.

- Off (Default) – Disables data output randomizer
- On – Enables data output randomizer

Two's complement: Enables two's complement mode.

- Off (Default) – Selects offset binary mode
- On – Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1620A demo board.

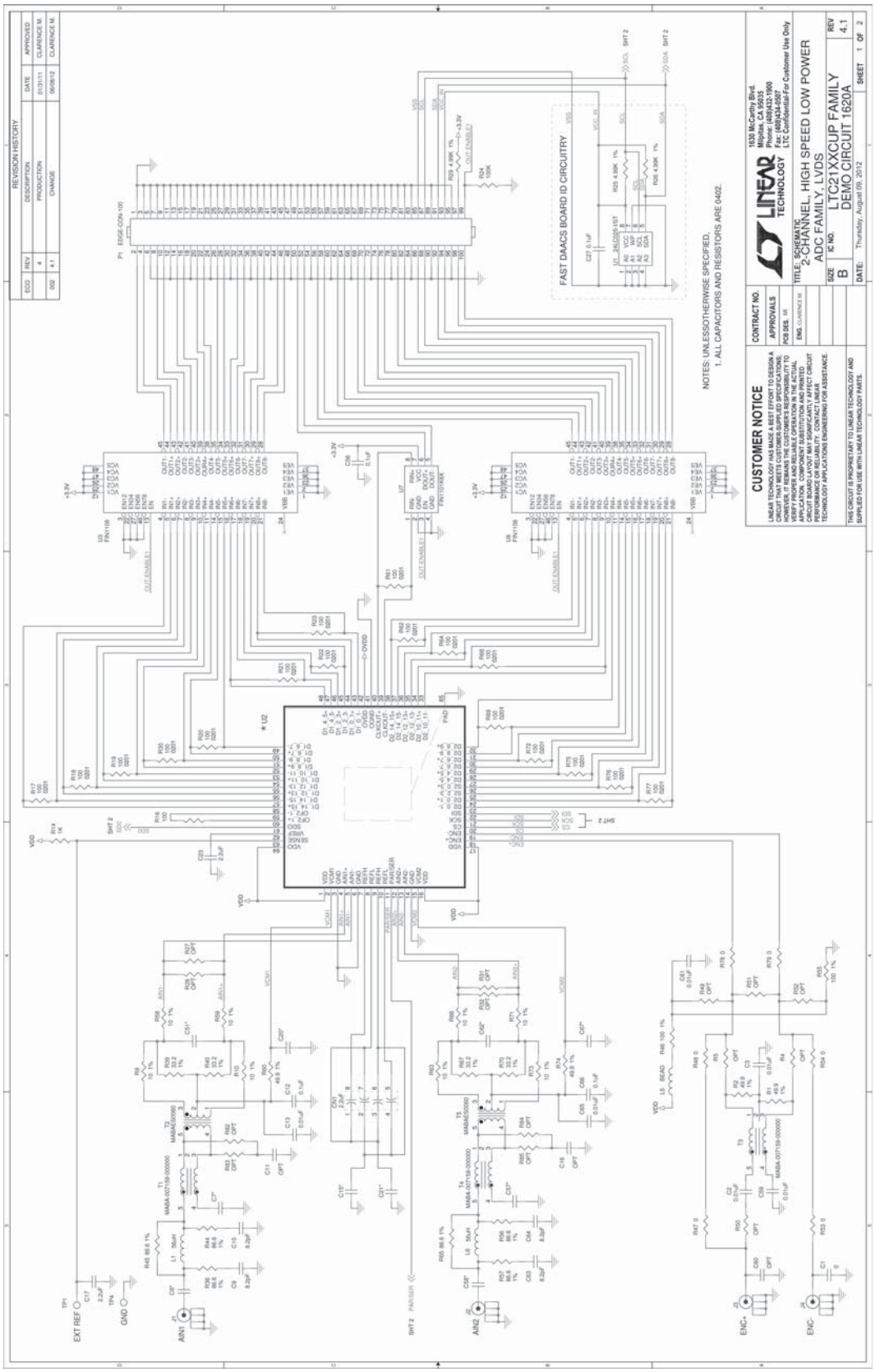
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	CN1	CAP, ARRAY, 0508 2.2µF 20% 10V X5R	AVX W0508L8ZD225MAT1A
2	7	R47, R48, R53, R54, R78, R79	RES, 0402 0Ω JUMPER	NIC NRC04Z0TRF
3	11	C1, C2, C3, C6, C7, C13, C57-C61, C65	CAP, 0402 0.01µF 10% 16V X7R	AVX 0402YC103KAT
4	4	C9, C10, C63, C64	CAP, 0402 8.2pF 5% 50V COG	AVX 04025A8R2JAT2A
5	0	C11, C16	CAP, 0402 OPTION	OPTION
6	9	C12, C15, C18-C21, C37, C66, C67	CAP, 0402 0.1µF 10% 10V X5R	TDK C1005X5R1A104K
7	4	C14, C22, C72, C73	CAP, 0603 1µF 10% 16V X7R	TDK C1608X7R1C105K
8	2	C17, C23	CAP, 0402 2.2µF 20% 6.3V X5R	TAIYO YUDEN JMK105BJ225MV-T
9	1	C24	CAP, 0603 4.7µF 20% 6.3V X5R	TDK C1608X5R0J475MT
10	13	C26-C32, C34-C36, C56, C75, C76	CAP, 0603 0.1µF 10% 50V X7R	TDK C1608X7R1H104K
11	0	C33, C70, C71	CAP, 0603 OPTION	OPTION
12	2	C51, C62	CAP, 0402 4.7pF ±0.25pF 50V NPO	AVX 04025A4R7CAT2A
13	2	C54, C55	CAP, 0805 10µF 10% 16V X5R	MURATA GRM21BR61C106KE15L
14	3	C68, C69, C74	CAP, 0402 22pF 5% 16V NPO	AVX 0402YA220JAT2A
15	5	JP2, JP3, JP4, JP5, JP6	HEADER, 3-PIN, 2mm	SAMTEC TMM-103-02-L-S
16	4	J1, J2, J3, J4	CONN, BNC, SMA 50-OHM EDGE-LANCH	E.F JOHNSON, 142-0701-851
17	2	L1, L6	IND, 0603 56µH 5%	MURATA LQP18MN56NG02D
18	3	L2, L3, L4	FERRITE BEAD, 1206	MURATA BLM31PG330SN1L
19	0	L5	IND, 0603 BEAD	TBD

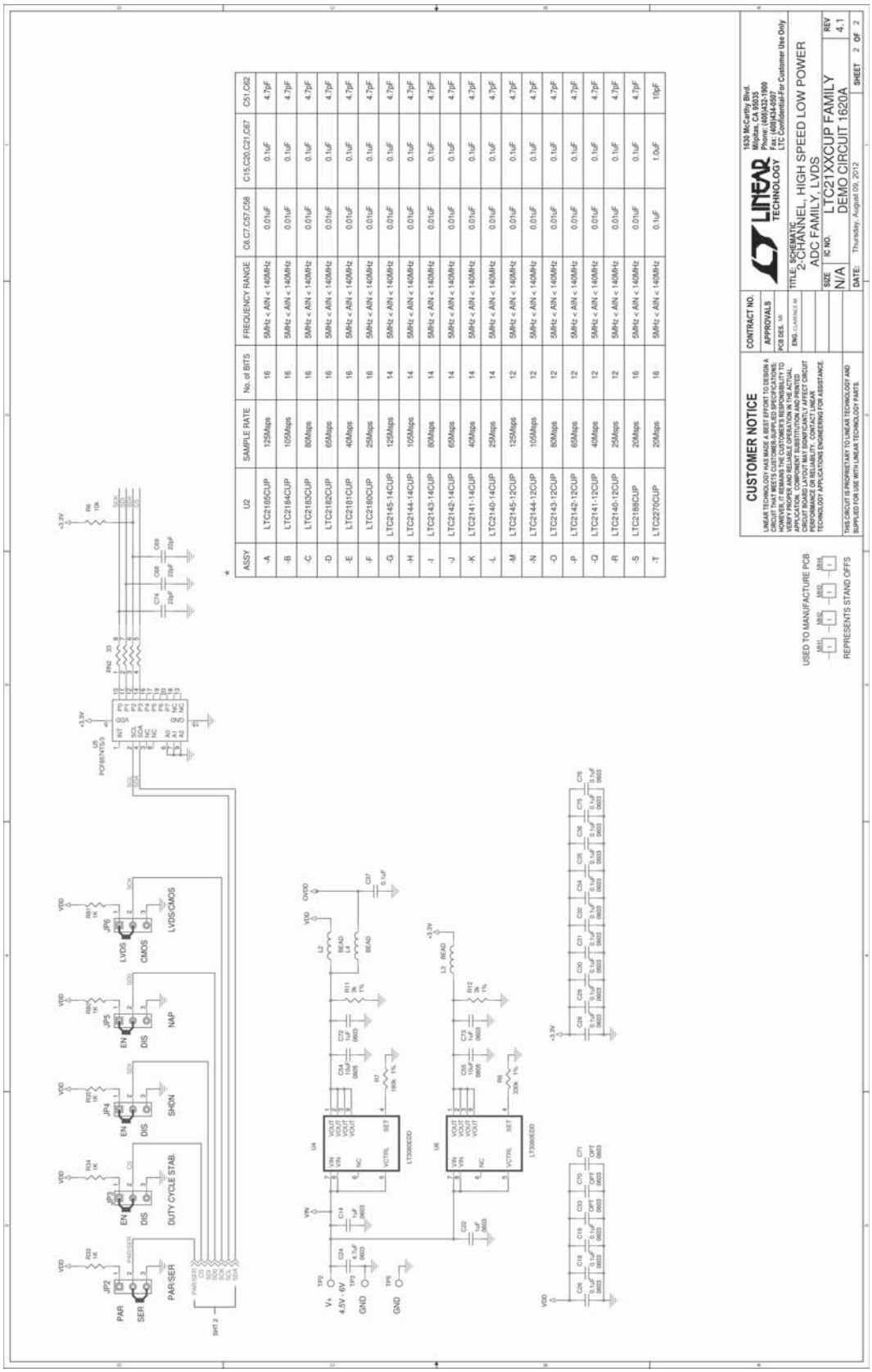
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
20	1	RN2	RES ARRAY, 33Ω	VISHAY CRA04SS08333R0JTD
21	4	R1, R2, R60, R74	RES, 0402 49.9Ω 1% 1/16W	YAGEO RC0402FR-0749R9L
22	0	R4, R5, R49-R52, R82, R83-R85	RES, 0402 OPTION	OPTION
23	1	R6	RES, 0402 10k 5% 1/16W	VISHAY CRCW040210K0JNED
24	1	R7	RES, 0402 180k 1% 1/16W	VISHAY CRCW0402180KFKED
25	1	R8	RES, 0402 330k 1% 1/16W	VISHAY CRCW0402330KFKEA
26	8	R9, R10, R58, R59, R63, R66, R71, R73	RES, 0402 10Ω 1% 1/16W	NIC NRC04F10R0TR
27	2	R11, R12	RES, 0402 3k 1% 1/16W	VISHAY CRCW04023K00FKED
28	6	R14, R33, R34, R35, R80, R81	RES, 0402 1k 5% 1/16W	VISHAY CRCW04021K00JNTDE3
29	1	R16	RES, 0402 100Ω 5% 1/16W	VISHAY CRCW0402100RJNED
30	17	R17-R23, R30, R61, R62, R64, R68, R69, R72, R75, R76, R77	RES, 0201 100Ω 1% 1/16W	NIC NRC02F1000TRF
31	1	R24	RES, 0402 100k 5% 1/16W	VISHAY CRCW0402100KJNED
32	3	R25, R26, R29	RES, 0603 4.99k 1% 1/16W	AAC CR16-4991FM
33	4	R27, R28, R31, R32	RES, 0201 OPTION	OPTION
34	6	R36, R44, R45, R56, R57, R65	RES, 0402 86.6Ω 1% 1/16W	VISHAY CRCW040286R6FKED
35	4	R39, R40, R67, R70	RES, 0402 33.2Ω 1% 1/16W	VISHAY CRCW040233R2FKED
36	2	R46, R55	RES, 0402 100Ω 1% 1/16W	NIC NRC04F1000TRF
37	5	TP1, TP2, TP3, TP4, TP5	TURRETS	MILLMAX 2501-2-00-80-00-00-07-0
38	3	T1, T3, T4	XFMR, 1:1	MACOM MABA-007159-000000
39	2	T2, T5	XFMR, 1:1 CT	M/A-COM MABAES0060
	0	T2, T5 - ALTERNATE	XFMR, 1:1 CT	COILCRAFT WBC1-1LB
40	1	U1	IC, EEPROM	MICROCHIP TECH. 24LC025-I/ST
41	1	U2	REFER TO SCHEMATIC TABLE	LINEAR TECH.
42	2	U3, U8	IC, FIN1108	FAIRCHILD FIN1108
43	2	U4, U6	IC, SINGLE RESISTOR LOW DROPOUT REGULATOR	LINEAR TECH. LT3080EDD
44	1	U5	IC, 8-BIT I/O EXPANDER	PHILIPS SEMI PCF8574TS/3
45	1	U7	IC, LVDS SINGLE PORT HIGH SPEED REPEATER	FAIRCHILD FIN1101K8X
46	5	JP2, JP3, JP4, JP5, JP6	SHUNT, 2mm	SAMTEC 2SN-BK-G
47	4		STANDOFF, SNAP ON	KEYSTONE_8831

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



ASSY	U2	SAMPLE RATE	No. of BITS	FREQUENCY RANGE	C6,C7,C57,C58	C15,C20,C21,C67	C51,C62
-A	LTC2185CUP	125Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-B	LTC2184CUP	105Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-C	LTC2183CUP	80Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-D	LTC2182CUP	65Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-E	LTC2181CUP	40Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-F	LTC2180CUP	25Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-G	LTC2145-14CUP	125Msps	14	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-H	LTC2144-14CUP	105Msps	14	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-I	LTC2143-14CUP	80Msps	14	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-J	LTC2142-14CUP	65Msps	14	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-K	LTC2141-14CUP	40Msps	14	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-L	LTC2140-14CUP	25Msps	14	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-M	LTC2145-12CUP	125Msps	12	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-N	LTC2144-12CUP	105Msps	12	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-O	LTC2143-12CUP	80Msps	12	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-P	LTC2142-12CUP	65Msps	12	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-Q	LTC2141-12CUP	40Msps	12	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-R	LTC2140-12CUP	25Msps	12	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-S	LTC2188CUP	20Msps	16	5MHz < AIN < 140MHz	0.01uF	0.1uF	4.7pF
-T	LTC2270CUP	20Msps	16	5MHz < AIN < 140MHz	0.1uF	1.0uF	10pF

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APPROVALS
PCB DES.
ENG.

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LTC Confidential-For Customer Use Only

TITLE: SCHEMATIC
2-CHANNEL, HIGH SPEED LOW POWER ADC FAMILY, LVDS
SIZE: N/A | I/C NO.: LTC21XXCUP FAMILY DEMO CIRCUIT 1620A | REV: 4.1
DATE: Thursday, August 09, 2012 | SHEET 2 OF 2

USED TO MANUFACTURE PCB
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