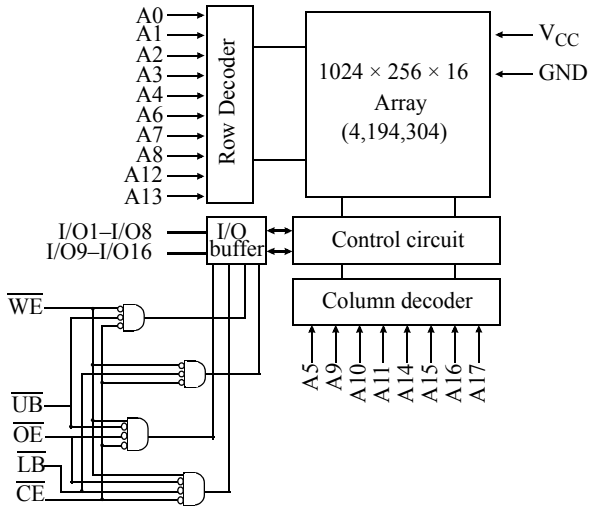
# 5.0 V 256 K × 16 CMOS SRAM

## Features

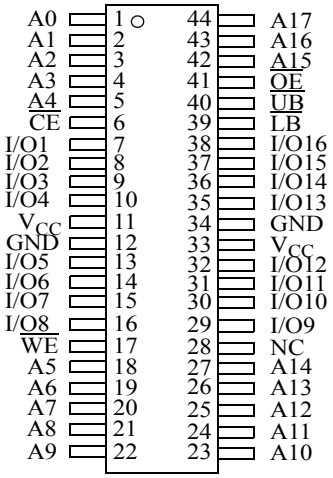
- Pin compatible with AS7C4098
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 5/6 ns output enable access time
- Low power consumption: ACTIVE
  - 990mW/max @ 10 ns
- Low power consumption: STANDBY
  - 55mW/max CMOS
- Individual byte read/write controls
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL- and CMOS-compatible, three-state I/O
- 44-pin JEDEC standard packages
  - 400-mil SOJ
  - TSOP 2
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

## Logic block diagram




## Pin arrangement for SOJ and TSOP 2

44-pin (400 mil) SOJ
TSOP2




## Selection guide

| | –10 | –12 | –15 | –20 | Unit |
|---|---|---|---|---|---|
| Maximum address access time | 10 | 12 | 15 | 20 | ns |
| Maximum output enable access time | 5 | 6 | 6 | 6 | ns |
| Maximum operating current | 180 | 160 | 140 | 120 | mA |
| Maximum CMOS standby current | 10 | 10 | 10 | 10 | mA |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## Functional description

The AS7C4098A is a high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ($t_{AA}$, $t_{RC}$, $t_{WC}$) of 10/12/15/20 ns with output enable access times ($t_{OE}$) of 5/6 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. The device is guaranteed not to exceed 55mW power consumption in CMOS standby mode. A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O16 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O1–I/O8, and $\overline{UB}$ controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is for 5.0V (AS7C4098A) supply. The device is available in the JEDEC standard 400-mL, 44-pin SOJ, TSOP 2 packages.

### Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Voltage on $V_{CC}$ relative to GND | $V_{t1}$ | –0.50 | +7.0 | V |
| Voltage on any pin relative to GND | $V_{t2}$ | –0.50 | $V_{CC}$ +0.50 | V |
| Power dissipation | $P_D$ | – | 1.5 | W |
| Storage temperature (plastic) | $T_{stg}$ | –65 | +150 | °C |
| Ambient temperature with $V_{CC}$ applied | $T_{bias}$ | –55 | +125 | °C |
| DC current into outputs (low) | $I_{OUT}$ | – | ±20 | mA |

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Truth table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O1–I/O8 | I/O9–I/O16 | Mode |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | High Z | Standby ($I_{SB}$, $I_{SB1}$) |
| L | H | H | X | X | High Z | High Z | Output disable ($I_{CC}$) |
| L | X | X | H | H | | | |
| L | H | L | L | H | $D_{OUT}$ | High Z | Read ($I_{CC}$) |
| | | | H | L | High Z | $D_{OUT}$ | |
| | | | L | L | $D_{OUT}$ | $D_{OUT}$ | |
| L | L | X | L | H | $D_{IN}$ | High Z | Write ($I_{CC}$) |
| | | | H | L | High Z | $D_{IN}$ | |
| | | | L | L | $D_{IN}$ | $D_{IN}$ | |

Key: X = Don't care, L = Low, H = High.

## Recommended operating conditions

| Parameter | | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ (10/12/15/20) | 4.5 | 5.0 | 5.5 | V |
| Input voltage | | $V_{IH}$* | 2.2 | – | $V_{CC}$ + 0.5 | V |
| | | $V_{IL}$** | –0.5 | – | 0.8 | V |
| Ambient operating temperature | commercial | $T_A$ | 0 | – | 70 | °C |
| | industrial | $T_A$ | –40 | – | 85 | °C |

*$V_{IH}$ max = $V_{CC}$ + 1.5V for pulse width less than 5 nS.

**$V_{IL}$ min = –1.0V for pulse width less than 5 nS.

## DC operating characteristics (over the operating range)[1]

| Parameter | Symbol | Test conditions | –10 | | –12 | | –15 | | –20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Input leakage current | $\|I_{LI}\|$ | $V_{CC}$ = Max<br>$V_{IN}$ = GND to $V_{CC}$ | – | 1 | – | 1 | – | 1 | – | 1 | µA | |
| Output leakage current | $\|I_{LO}\|$ | $V_{CC}$ = Max<br>$\overline{CE}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$<br>or $\overline{WE}$ = $V_{IL}$<br>$V_{I/O}$ = GND to $V_{CC}$ | – | 1 | – | 1 | – | 1 | – | 1 | µA | |
| Operating power supply current | $I_{CC}$ | $V_{CC}$ = Max<br>$\overline{CE} \le V_{IL}$, f = fmax, $I_{OUT}$ = 0 mA | - | 180 | - | 160 | - | 140 | - | 120 | mA | |
| Standby power supply current | $I_{SB}$ | $V_{CC}$ = Max<br>$\overline{CE} \ge V_{IH}$, f = Max | - | 60 | - | 55 | - | 50 | - | 45 | mA | |
| | $I_{SB1}$ | $V_{CC}$ = Max<br>$\overline{CE} \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0 | - | 10 | - | 10 | - | 10 | - | 10 | mA | |
| Output voltage | $V_{OL}$ | $I_{OL}$ = 6 mA, $V_{CC}$ = Min | – | 0.4 | – | 0.4 | – | 0.4 | – | 0.4 | V | 4 |
| | | $I_{OL}$ = 8 mA, $V_{CC}$ = Min | – | 0.5 | – | 0.5 | – | 0.5 | – | 0.5 | | |
| | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{CC}$ = Min | 2.4 | – | 2.4 | – | 2.4 | – | 2.4 | – | V | 4 |

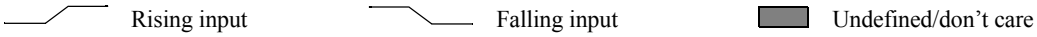
## Capacitance (f = 1MHz, $T_a$ = 25° C, $V_{CC}$ = NOMINAL)[4]

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ | $V_{IN}$ = 0V | 6 | pF |
| I/O capacitance | $C_{I/O}$ | I/O | $V_{IN}$ = $V_{OUT}$ = 0V | 8 | pF |

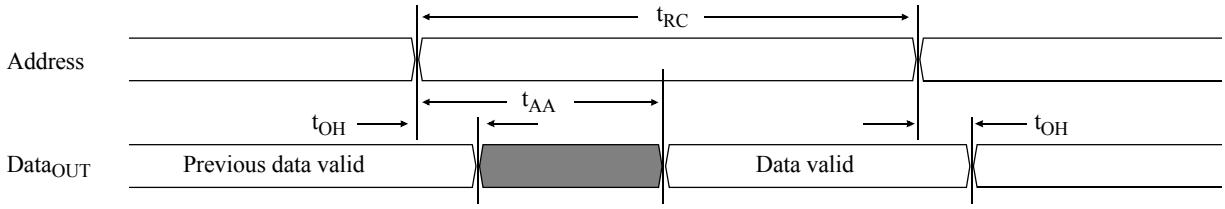
## Read cycle (over the operating range)[2,8]

| Parameter | Symbol | –10 | | –12 | | –15 | | –20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read cycle time | $t_{RC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Address access time | $t_{AA}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | |
| Chip enable ($\overline{CE}$) access time | $t_{ACE}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | |
| Output enable ($\overline{OE}$) access time | $t_{OE}$ | – | 5 | – | 6 | – | 6 | – | 6 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 4 |
| $\overline{CE}$ Low to output in low Z | $t_{CLZ}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 3, 4 |
| $\overline{CE}$ High to output in high Z | $t_{CHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | 3, 4 |
| $\overline{OE}$ Low to output in low Z | $t_{OLZ}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 3, 4 |
| $\overline{OE}$ High to output in high Z | $t_{OHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | 3, 4 |
| $\overline{LB}$, $\overline{UB}$ access time | $t_{BA}$ | – | 5 | – | 6 | – | 7 | – | 8 | ns | |
| $\overline{LB}$, $\overline{UB}$ Low to output in low Z | $t_{BLZ}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| $\overline{LB}$, $\overline{UB}$ High to output in high Z | $t_{BHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | |
| Power up time | $t_{PU}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4 |
| Power down time | $t_{PD}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 4 |

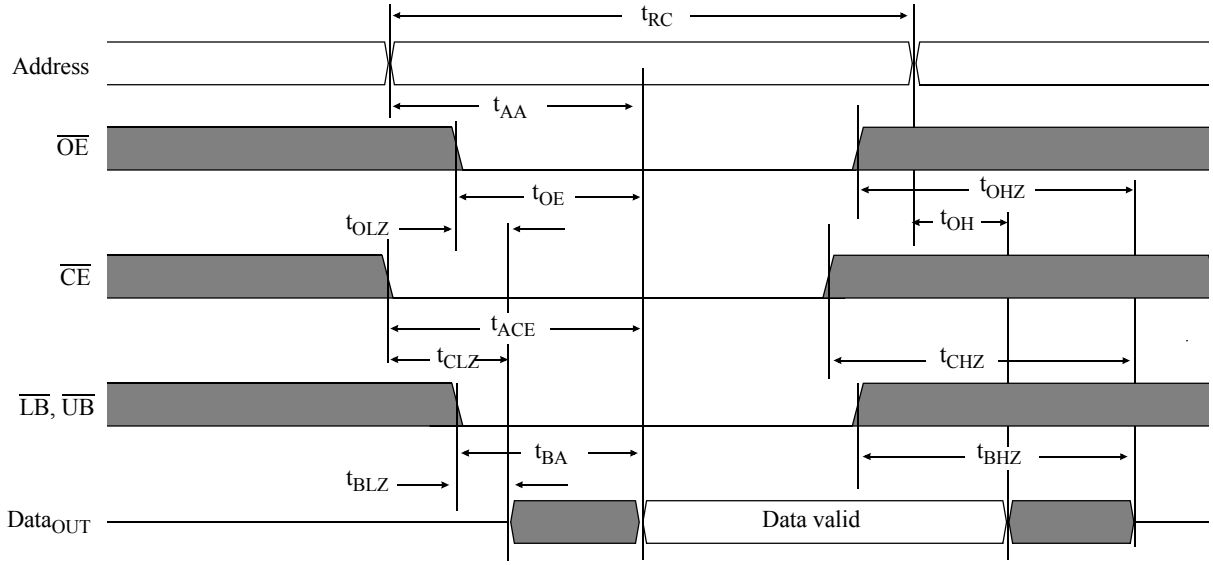
## Key to switching waveforms




## Read waveform 1 (address controlled)[5,6,8]



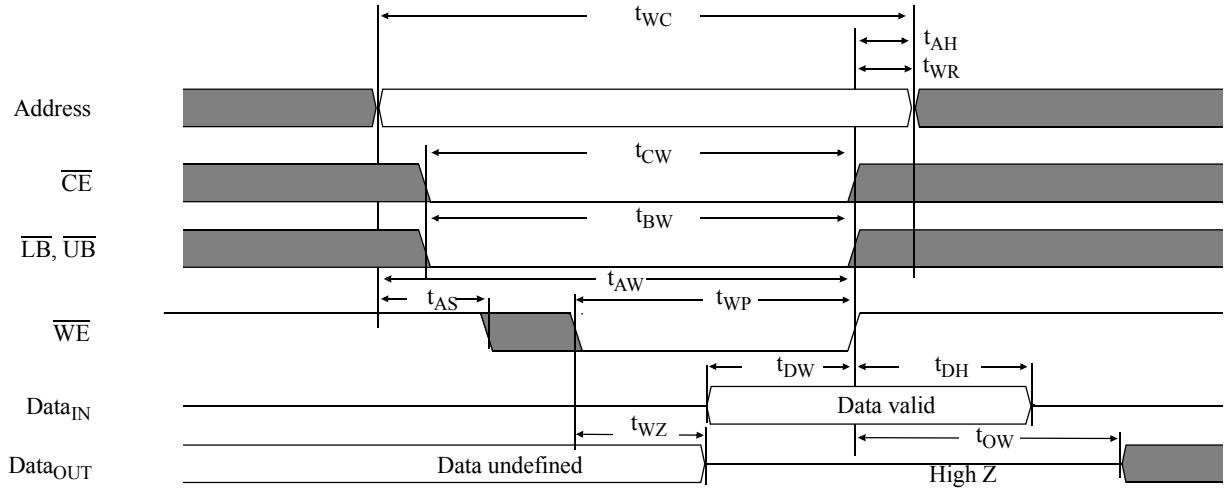
## Read waveform 2 ($\overline{CE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)[5,7,8]



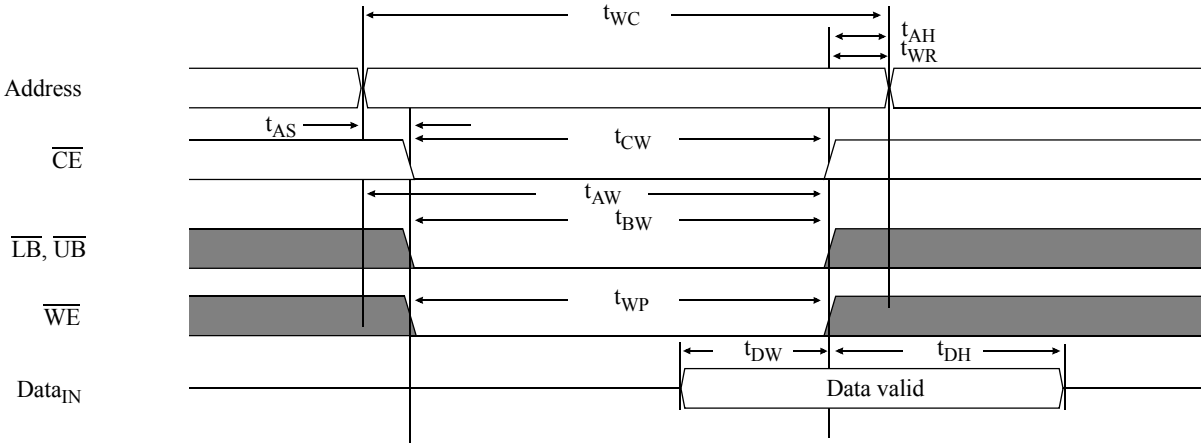

## Write cycle (over the operating range)[9]

| Parameter | Symbol | –10 | | –12 | | –15 | | –20 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write cycle time | $t_{WC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Chip enable ($\overline{CE}$) to write end | $t_{CW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Address setup to write end | $t_{AW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Address setup time | $t_{AS}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Write pulse width ($\overline{OE}$ = High) | $t_{WP1}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Write pulse width ($\overline{OE}$ = Low) | $t_{WP2}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Write recovery time | $t_{WR}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Address hold from end of write | $t_{AH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Data valid to write end | $t_{DW}$ | 5 | – | 6 | | 7 | – | 9 | – | ns | |
| Data hold time | $t_{DH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 3, 4 |
| Write enable to output in High-Z | $t_{WZ}$ | 2 | 5 | 2 | 6 | 2 | 7 | 2 | 9 | ns | 3, 4 |
| Output active from write end | $t_{OW}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 3, 4 |
| Byte enable Low to write end | $t_{BW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | 3, 4 |

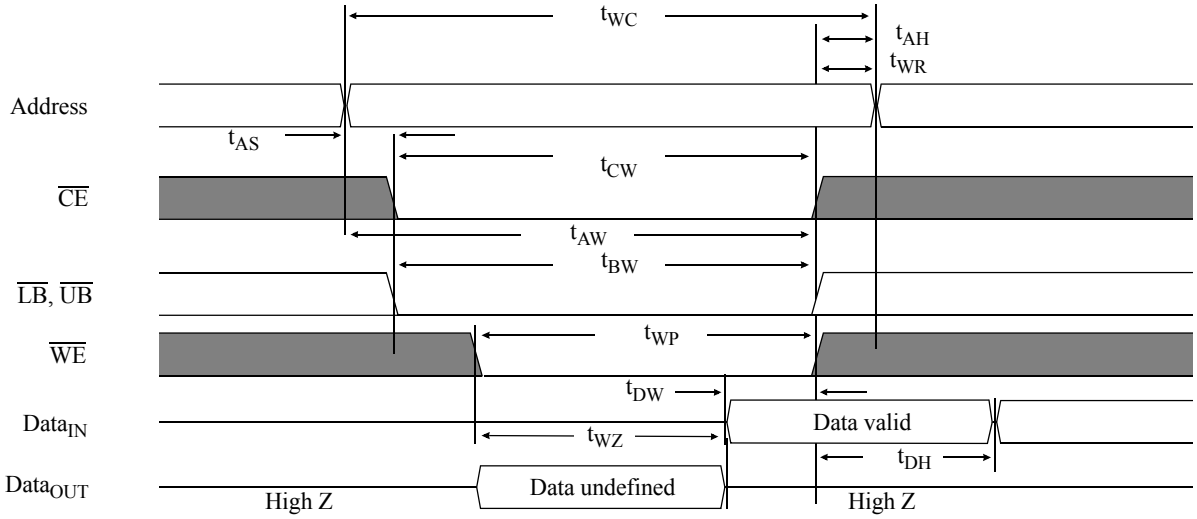
## Write waveform 1($\overline{WE}$ controlled)[9]




## Write waveform 2 ($\overline{CE}$ controlled)[9]



## Write waveform 3 [9]




## AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to $V_{CC}$ - 0.5V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

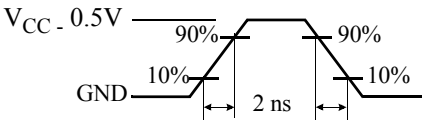



Figure A: Input pulse

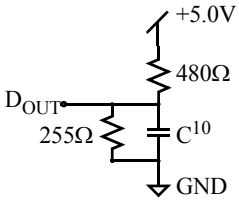
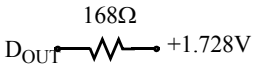



Figure B:5.0V Output load

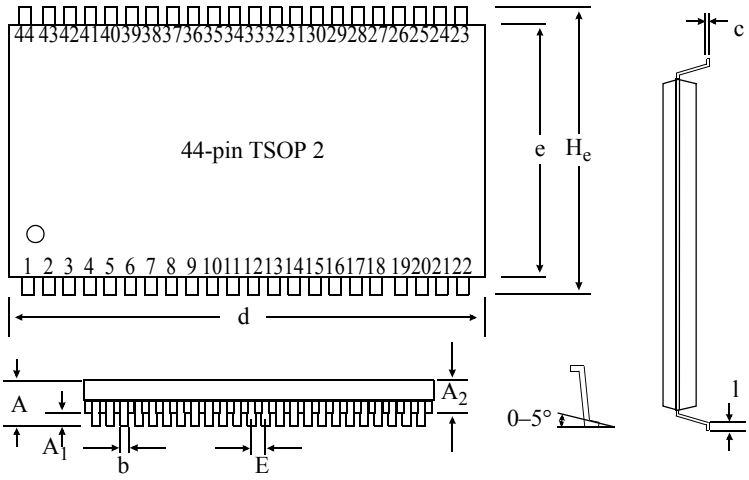
Thevenin equivalent:



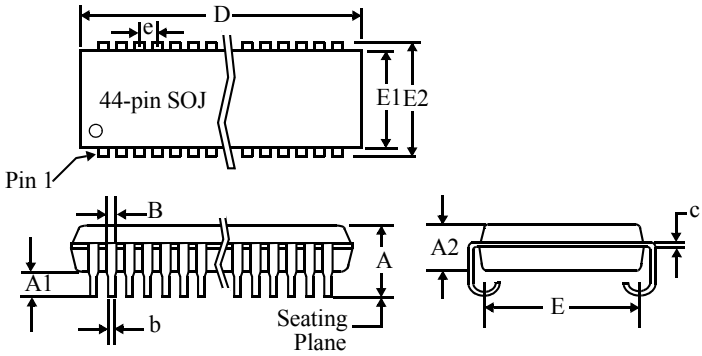

Notes

1 During $V_{CC}$ power-up, a pull-up resistor to $V_{CC}$ on $\overline{CE}$ is required to meet $I_{SB}$ specification.
2 For test conditions, see *AC Test Conditions*, Figures A and B.
3 $t_{CLZ}$ and $t_{CHZ}$ are specified with $C_L$ = 5pF as in Figure B. Transition is measured ±500mV from steady-state voltage.
4 This parameter is guaranteed, but not tested.
5 $\overline{WE}$ is High for read cycle.
6 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
7 Address valid prior to or coincident with $\overline{CE}$ transition Low.
8 All read cycle timings are referenced from the last valid address to the first transitioning address.
9 All write cycle timings are referenced from the last valid address to the first transitioning address.
10 C = 30 pF, except on High Z and Low Z parameters, where C = 5 pF.

## Package dimensions




| | 44-pin TSOP 2 | |
|---|---|---|
| | Min (mm) | Max (mm) |
| A | | 1.2 |
| $A_1$ | 0.05 | 0.15 |
| $A_2$ | 0.95 | 1.05 |
| b | 0.30 | 0.45 |
| c | 0.12 | 0.21 |
| d | 18.31 | 18.52 |
| e | 10.06 | 10.26 |
| $H_e$ | 11.68 | 11.94 |
| E | 0.80 (typical) | |
| l | 0.40 | 0.60 |




| | 44-pin SOJ 400 mils | |
|---|---|---|
| | Min(mils) | Max(mils) |
| A | 0.128 | 0.148 |
| A1 | 0.025 | - |
| A2 | 0.105 | 0.115 |
| B | 0.026 | 0.032 |
| b | 0.015 | 0.020 |
| c | 0.007 | 0.013 |
| D | 1.120 | 1.130 |
| E | 0.370 NOM | |
| E1 | 0.395 | 0.405 |
| E2 | 0.435 | 0.445 |
| e | 0.050 NOM | |

## Ordering Codes

| Package | Version | 10 ns | 12 ns | 15 ns | 20 ns |
|---|---|---|---|---|---|
| SOJ | 5.0V commercial | AS7C4098A-10JC | AS7C4098A-12JC | AS7C4098A-15JC | AS7C4098A-20JC |
| | 5.0V industrial | AS7C4098A-10JI | AS7C4098A-12JI | AS7C4098A-15JI | AS7C4098A-20JI |
| TSOP 2 | 5.0V commercial | AS7C4098A-10TC | AS7C4098A-12TC | AS7C4098A-15TC | AS7C4098A-20TC |
| | 5.0V industrial | AS7C4098A-10TI | AS7C4098A-12TI | AS7C4098A-15TI | AS7C4098A-20TI |

**Note: Add suffix 'N' to the above part numbers for Lead Free Parts. (Ex: AS7C4098A - 10TCN)**

## Part numbering system

| AS7C | 4098A | –XX | J or T | X | X |
|---|---|---|---|---|---|
| SRAM prefix | Device number | Access time | Packages:<br>J: SOJ 400 mil<br>T: TSOP 2 | Temperature ranges:<br>C: Commercial, 0°C to 70°C<br>I: Industrial, –40°C to 85°C | N = Lead Free Parts |

## Revision History

| Rev. No. | History | Revised Date |
|---|---|---|
| v1.0 | Initial release | 11/08/04 |
| v1.1 | Included $I_{CC}$, $I_{SB}$ & $I_{SB1}$ parameters | 05/27/05 |
| | Corrected the following: $T_{OE}$, $V_{IH}$, $V_{OL}$ & $t_{WZ}$ | |
| v1.2 | Removed the title “PRELIMINARY INFORMATION” | 02/21/06 |

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