

NX3L4684

Dual low-ohmic single-pole double-throw analog switch

Rev. 04 — 24 March 2010

Product data sheet

1. General description

The NX3L4684 provides two low-ohmic single-pole double-throw analog switches, suitable for use as an analog or digital multiplexer/demultiplexer. It has a digital select input (nS) with Schmitt trigger action, two independent inputs/outputs (nY0, nY1) and a common input/output (nZ). Schmitt trigger action at the select input (nS) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 1.4 V to 4.3 V.

A low input voltage threshold allows pin nS to be driven by lower level logic signals without a significant increase in supply current I_{CC} . This makes it possible for the NX3L4684 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation.

The NX3L4684 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ. Its low ON resistance (0.3 Ω for Y0 port, 0.5 Ω for Y1 port) and flatness (0.1 Ω) ensures minimal attenuation and distortion of transmitted signals.

2. Features

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak) for Y0 port:
 - ◆ 0.8 Ω (typical) at $V_{CC} = 1.4$ V
 - ◆ 0.5 Ω (typical) at $V_{CC} = 1.65$ V
 - ◆ 0.3 Ω (typical) at $V_{CC} = 2.3$ V
 - ◆ 0.25 Ω (typical) at $V_{CC} = 2.7$ V
 - ◆ 0.25 Ω (typical) at $V_{CC} = 4.3$ V
- Break-before-make switching
- High noise immunity
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78B Class II Level A
- 1.8 V control logic at $V_{CC} = 3.6$ V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Applications

- Cell phone
- PDA
- Portable media player

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NX3L4684GM	-40 °C to +125 °C	XQFN10U	plastic extremely thin quad flat package; no leads; 10 terminals; UTLP based; body 2 × 1.55 × 0.5 mm	SOT1049-2
NX3L4684TK	-40 °C to +125 °C	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; 3 × 3 × 0.85 mm	SOT650-1

5. Marking

Table 2. Marking

Type number	Marking code
NX3L4684GM	D84
NX3L4684TK	D84

6. Functional diagram

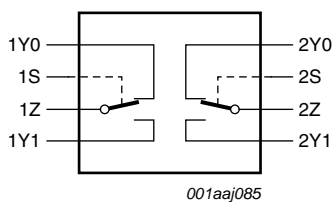


Fig 1. Logic symbol

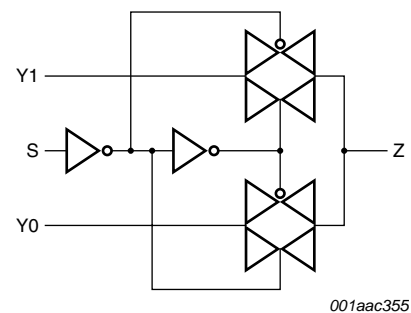


Fig 2. Logic diagram (one switch)

7. Pinning information

7.1 Pinning

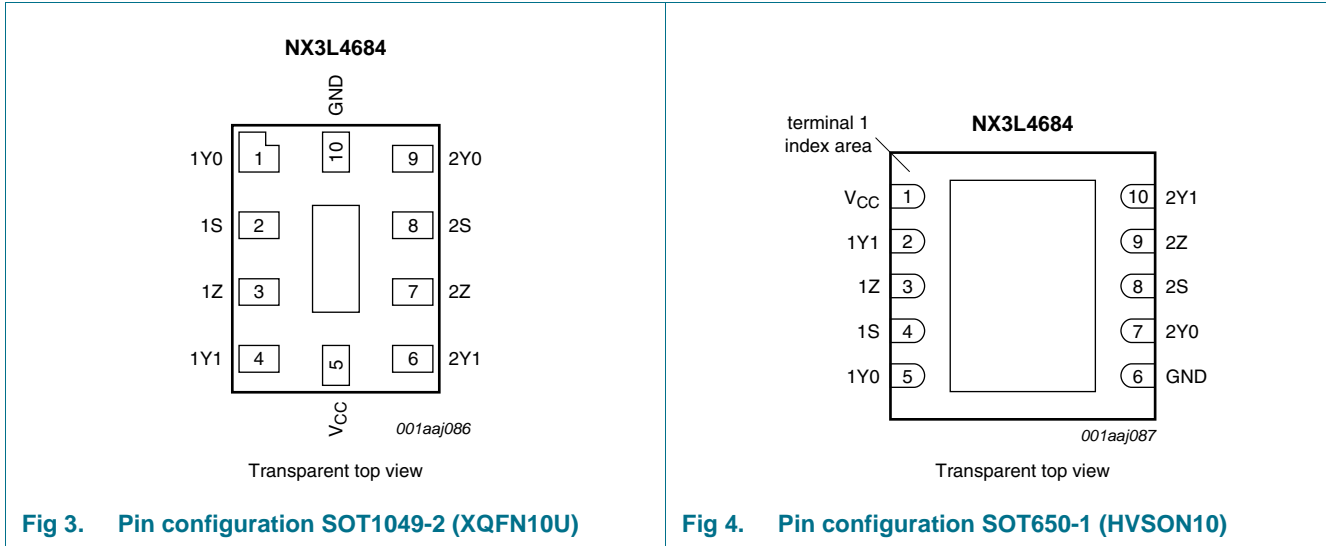


Fig 3. Pin configuration SOT1049-2 (XQFN10U)

Fig 4. Pin configuration SOT650-1 (HVSON10)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1049-2	SOT650-1	
1Y0	1	5	independent input or output
1S	2	4	select input
1Z	3	3	common output or input
1Y1	4	2	independent input or output
V _{CC}	5	1	supply voltage
2Y1	6	10	independent input or output
2Z	7	9	common output or input
2S	8	8	select input
2Y0	9	7	independent input or output
GND	10	6	ground (0 V)

8. Functional description

Table 4. Function table^[1]

Input nS	Channel on
L	nY0
H	nY1

- [1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	select input nS	^[1] -0.5	+4.6	V
V_{SW}	switch voltage	switch input nY0 or nY1	^[2] -0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	± 50	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current	-	± 350	mA
		$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	± 500	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3] -	250	mW

- [1] The minimum input voltage rating may be exceeded if the input current rating is observed.
 [2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.
 [3] For XQFN10U packages: above 132 °C the value of P_{tot} derates linearly with 14.1 mW/K.
 For HVSON10 packages: above 135 °C the value of P_{tot} derates linearly with 17.2 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.4	4.3	V
V_I	input voltage	select input nS	0	4.3	V
V_{SW}	switch voltage	switch input nY0 or nY1	^[1] 0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.4$ V to 4.3 V	^[2] -	200	ns/V

- [1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nYn. In this case, there is no limit for the voltage drop across the switch.
 [2] Applies to select input nS signal levels.

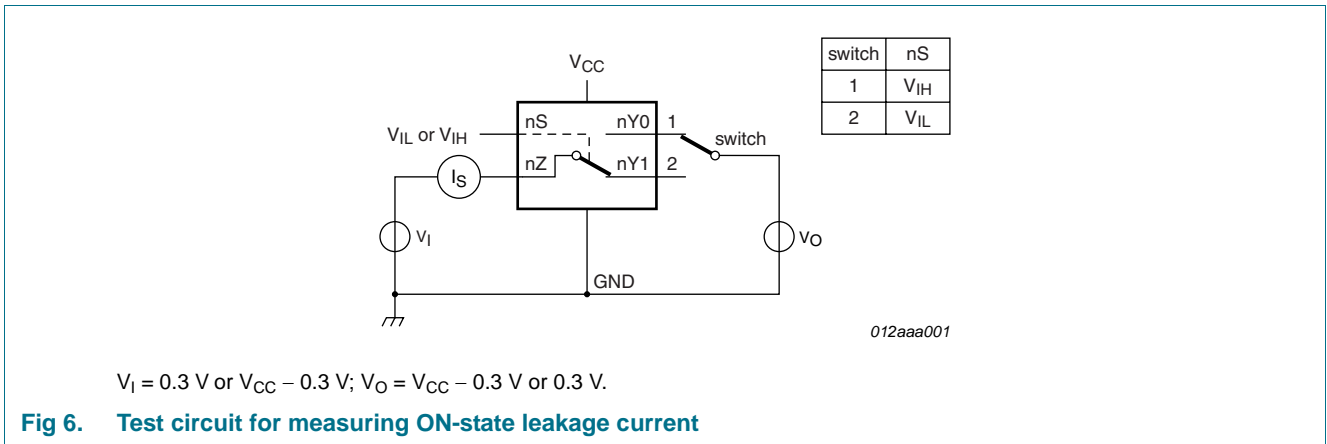
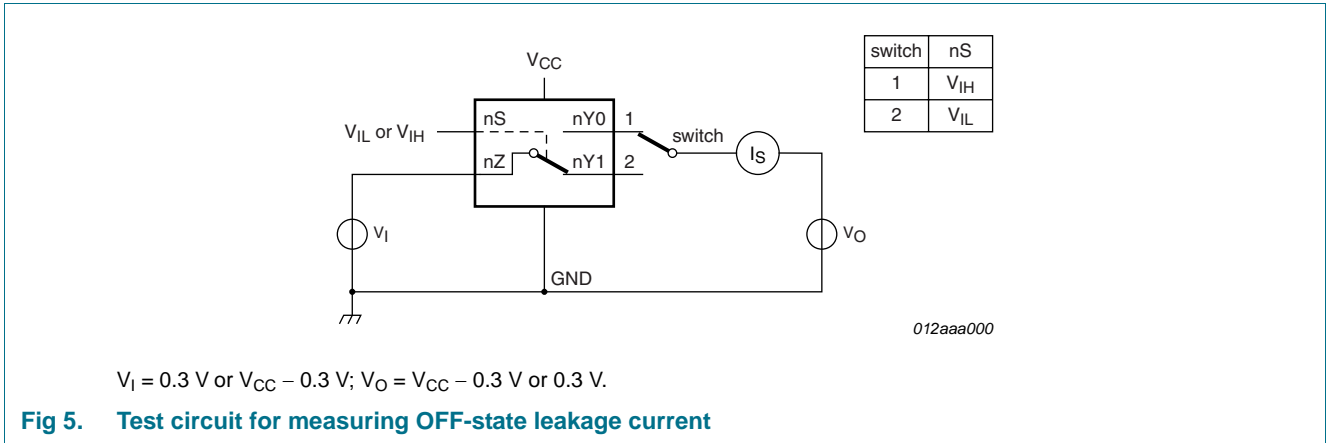
11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.4 V to 1.6 V	0.9	-	-	0.9	-	-	V
		V _{CC} = 1.65 V to 1.95 V	0.9	-	-	0.9	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.1	-	-	1.1	-	-	V
		V _{CC} = 2.7 V to 3.6 V	1.3	-	-	1.3	-	-	V
		V _{CC} = 3.6 V to 4.3 V	1.4	-	-	1.4	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.4 V to 1.6 V	-	-	0.3	-	0.3	0.3	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.4	-	0.4	0.3	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.5	-	0.5	0.4	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	0.5	V
		V _{CC} = 3.6 V to 4.3 V	-	-	0.6	-	0.6	0.6	V
I _I	input leakage current	select input nS; V _I = GND to 4.3 V; V _{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	±1	µA
I _{S(OFF)}	OFF-state leakage current	nYn port; see Figure 5							
		V _{CC} = 1.4 V to 3.6 V	-	-	±5	-	±10	±100	nA
		V _{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±200	nA
I _{S(ON)}	ON-state leakage current	nZ port; see Figure 6							
		V _{CC} = 1.4 V to 3.6 V	-	-	±5	-	±20	±200	nA
		V _{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±400	nA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{SW} = GND or V _{CC}							
		V _{CC} = 3.6 V	-	-	100	-	300	3000	nA
		V _{CC} = 4.3 V	-	-	150	-	500	5000	nA
ΔI _{CC}	additional supply current	V _{SW} = GND or V _{CC}							
		V _I = 2.6 V; V _{CC} = 4.3 V	-	2.0	4.0	-	7	7	µA
		V _I = 2.6 V; V _{CC} = 3.6 V	-	0.35	0.7	-	1	1	µA
		V _I = 1.8 V; V _{CC} = 4.3 V	-	7.0	10.0	-	15	15	µA
		V _I = 1.8 V; V _{CC} = 3.6 V	-	2.5	4.0	-	5	5	µA
C _I	input capacitance	V _I = 1.8 V; V _{CC} = 2.5 V	-	50	200	-	300	500	nA
			-	1.0	-	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	port nY0	-	65	-	-	-	-	pF
		port nY1	-	35	-	-	-	-	pF
C _{S(ON)}	ON-state capacitance	port nY0	-	260	-	-	-	-	pF
		port nY1	-	160	-	-	-	-	pF

11.1 Test circuits



11.2 ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 9](#) to [Figure 21](#).

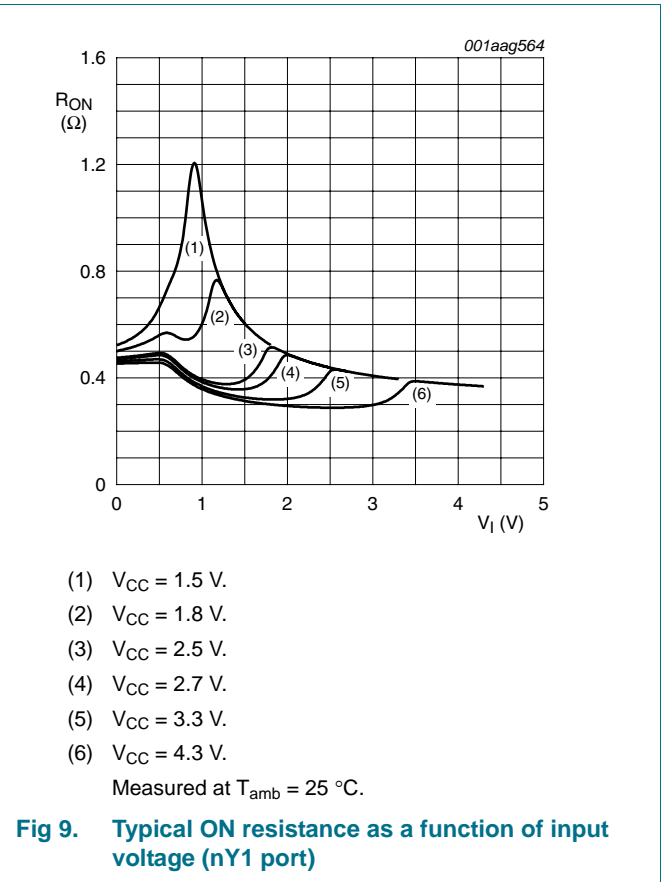
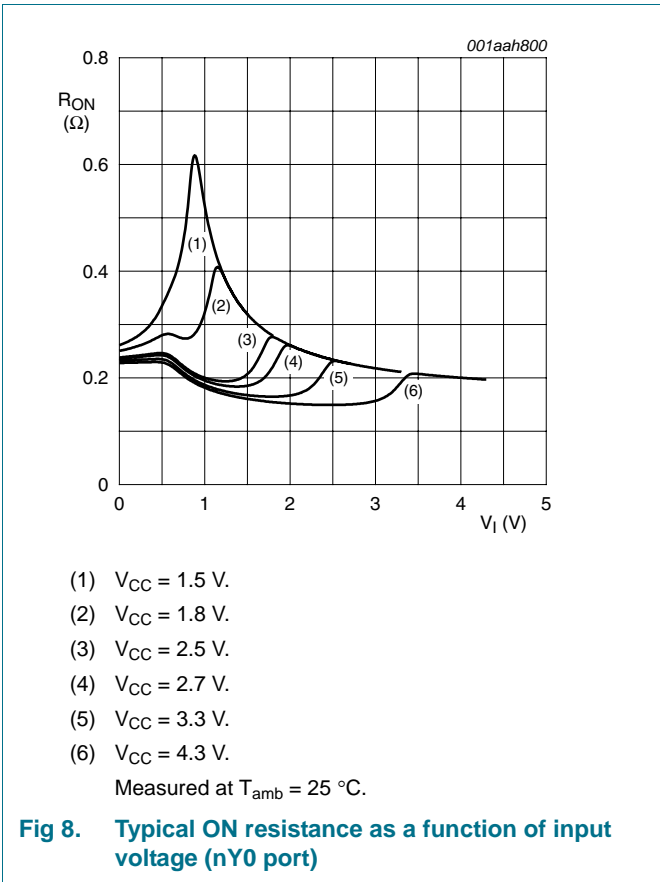
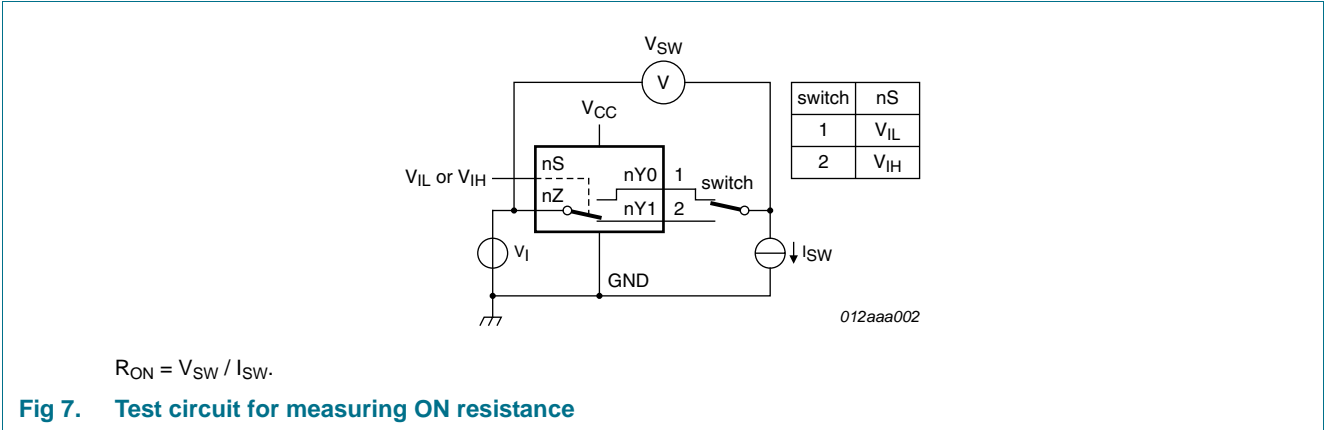
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit		
			Min	Typ ^[1]	Max	Min	Max			
R _{ON(peak)}	ON resistance (peak)	port nY0; see Figure 7 ; V _I = GND to V _{CC} ; I _{SW} = 100 mA								
		V _{CC} = 1.4 V	-	0.85	2.0	-	2.2	Ω		
		V _{CC} = 1.65 V	-	0.55	0.8	-	0.9	Ω		
		V _{CC} = 2.3 V	-	0.35	0.5	-	0.6	Ω		
		V _{CC} = 2.7 V	-	0.30	0.45	-	0.5	Ω		
		V _{CC} = 4.3 V	-	0.30	0.45	-	0.5	Ω		
		port nY1; see Figure 7 ; V _I = GND to V _{CC} ; I _{SW} = 100 mA								
		V _{CC} = 1.4 V	-	1.65	3.7	-	4.1	Ω		
		V _{CC} = 1.65 V	-	0.95	1.6	-	1.7	Ω		
		V _{CC} = 2.3 V	-	0.55	0.8	-	0.9	Ω		
		V _{CC} = 2.7 V	-	0.50	0.75	-	0.9	Ω		
		V _{CC} = 4.3 V	-	0.50	0.75	-	0.9	Ω		
		ΔR _{ON}	ON resistance mismatch between channels	V _I = GND to V _{CC} ; I _{SW} = 100 mA [2]						
				V _{CC} = 1.4 V	-	0.15	0.3	-	0.3	Ω
V _{CC} = 1.65 V	-			0.15	0.2	-	0.3	Ω		
V _{CC} = 2.3 V	-			0.04	0.08	-	0.1	Ω		
V _{CC} = 2.7 V	-			0.04	0.075	-	0.1	Ω		
V _{CC} = 4.3 V	-			0.04	0.075	-	0.1	Ω		
R _{ON(flat)}	ON resistance (flatness)	port nY0; V _I = GND to V _{CC} ; I _{SW} = 100 mA [3]								
		V _{CC} = 1.4 V	-	0.5	1.7	-	1.8	Ω		
		V _{CC} = 1.65 V	-	0.25	0.6	-	0.7	Ω		
		V _{CC} = 2.3 V	-	0.1	0.2	-	0.2	Ω		
		V _{CC} = 2.7 V	-	0.1	0.15	-	0.2	Ω		
		V _{CC} = 4.3 V	-	0.1	0.20	-	0.25	Ω		
		port nY1; V _I = GND to V _{CC} ; I _{SW} = 100 mA [3]								
		V _{CC} = 1.4 V	-	1.0	3.3	-	3.6	Ω		
		V _{CC} = 1.65 V	-	0.5	1.2	-	1.3	Ω		
		V _{CC} = 2.3 V	-	0.15	0.3	-	0.35	Ω		
		V _{CC} = 2.7 V	-	0.13	0.3	-	0.35	Ω		
		V _{CC} = 4.3 V	-	0.2	0.4	-	0.45	Ω		

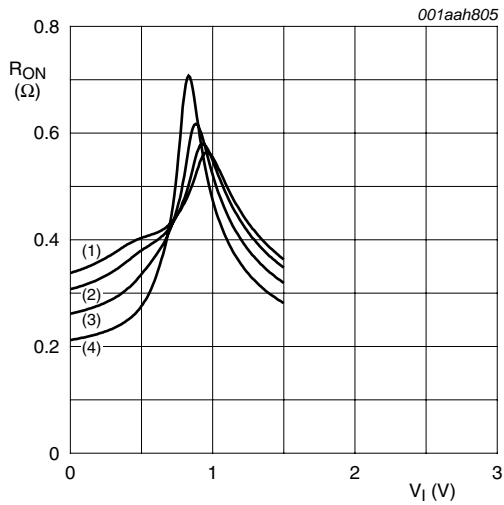
[1] Typical values are measured at T_{amb} = 25 °C.

[2] Measured at identical V_{CC}, temperature and input voltage.

[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

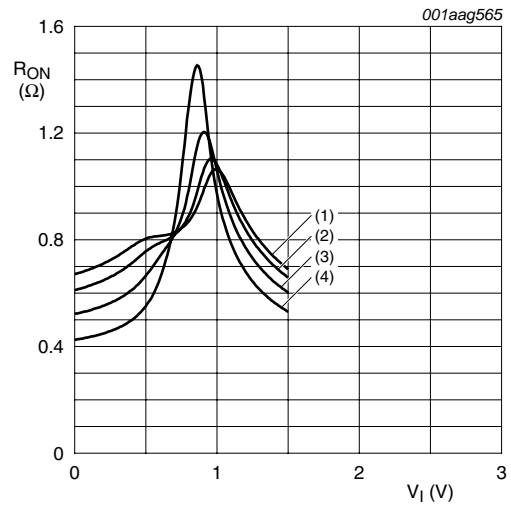
11.3 ON resistance test circuit and graphs





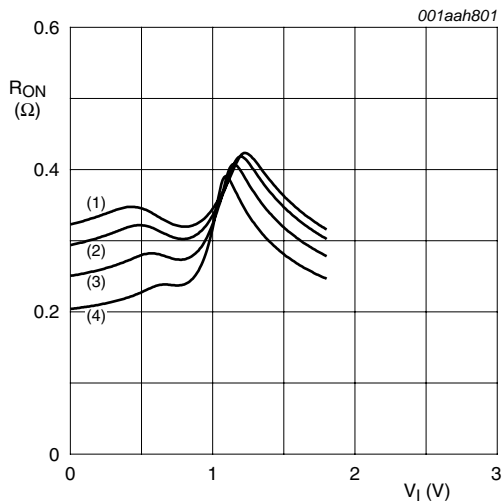
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 10. ON resistance as a function of input voltage; $V_{CC} = 1.5\text{ V}$ (nY0 port)



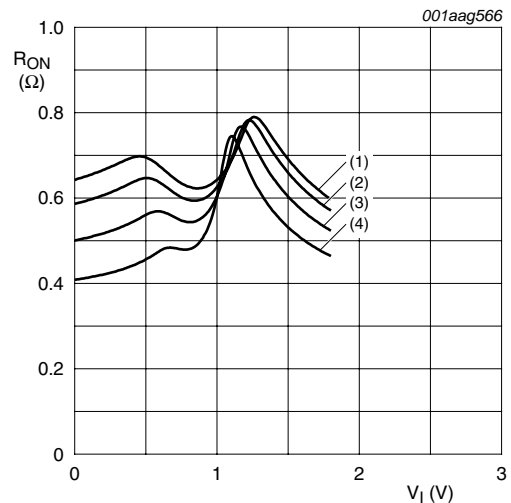
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 11. ON resistance as a function of input voltage; $V_{CC} = 1.5\text{ V}$ (nY1 port)



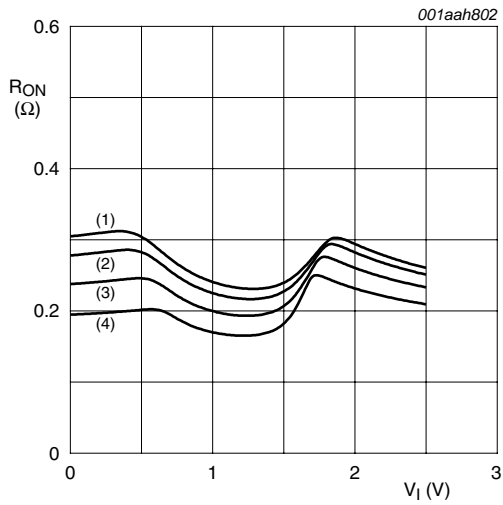
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 12. ON resistance as a function of input voltage; $V_{CC} = 1.8\text{ V}$ (nY0 port)



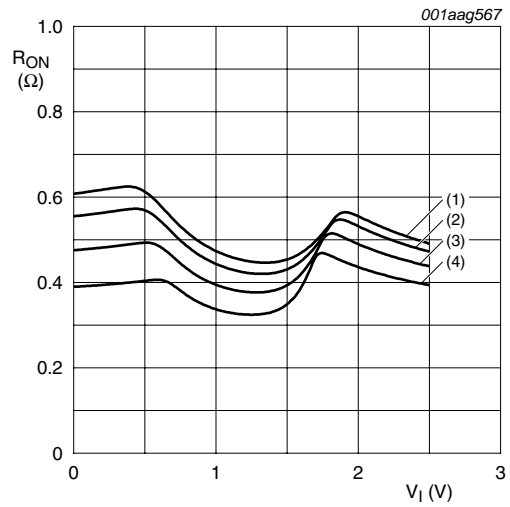
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 13. ON resistance as a function of input voltage; $V_{CC} = 1.8\text{ V}$ (nY1 port)



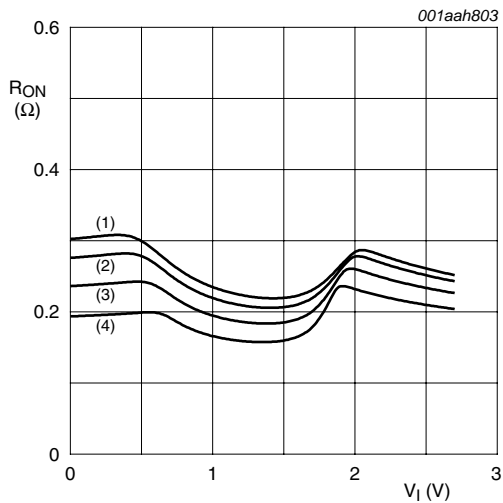
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 14. ON resistance as a function of input voltage; $V_{CC} = 2.5\text{ V}$ (nY0 port)



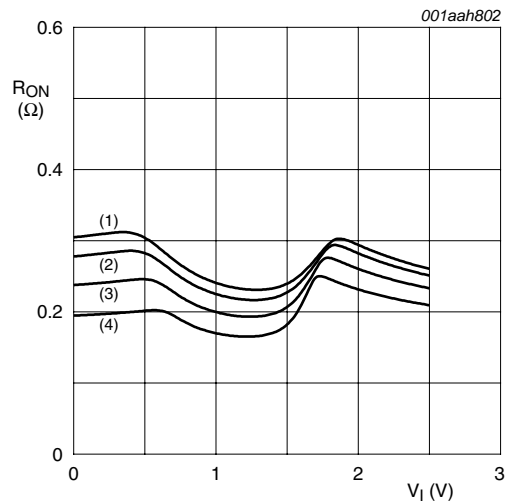
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 15. ON resistance as a function of input voltage; $V_{CC} = 2.5\text{ V}$ (nY1 port)



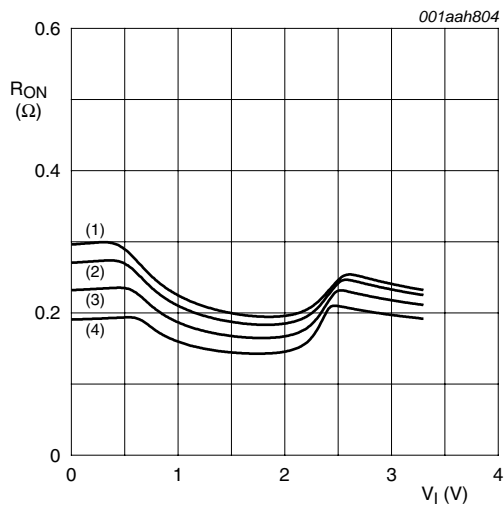
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 16. ON resistance as a function of input voltage; $V_{CC} = 2.7\text{ V}$ (nY0 port)



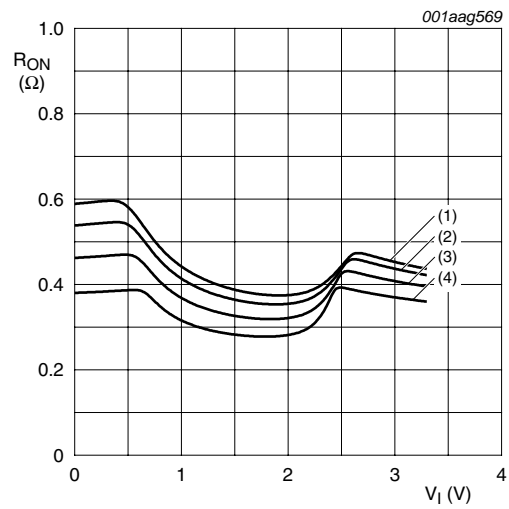
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 17. ON resistance as a function of input voltage; $V_{CC} = 2.7\text{ V}$ (nY1 port)



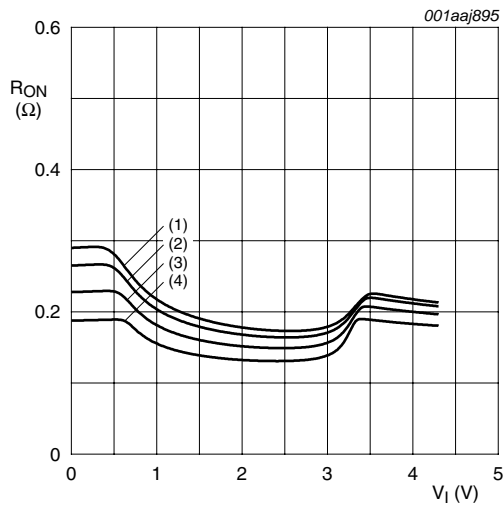
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 18. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$ (nY0 port)



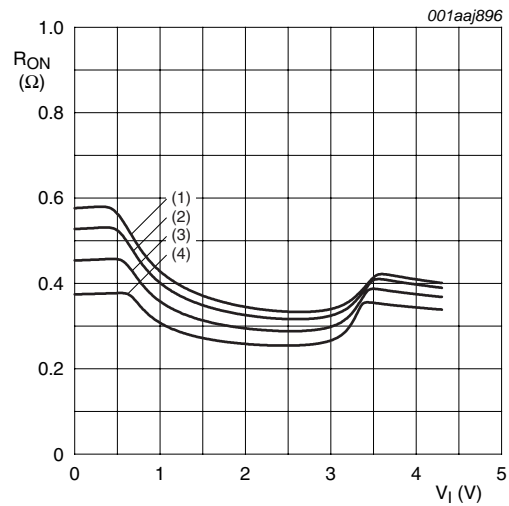
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 19. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$ (nY1 port)



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 20. ON resistance as a function of input voltage; $V_{CC} = 4.3\text{ V}$ (nY0 port)



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}.$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}.$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}.$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}.$

Fig 21. ON resistance as a function of input voltage; $V_{CC} = 4.3\text{ V}$ (nY1 port)

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see [Figure 24](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t _{en}	enable time	nS to nZ or nYn; see Figure 22							
		V _{CC} = 1.4 V to 1.6 V	-	50	100	-	130	130	ns
		V _{CC} = 1.65 V to 1.95 V	-	35	80	-	85	95	ns
		V _{CC} = 2.3 V to 2.7 V	-	24	50	-	55	60	ns
		V _{CC} = 2.7 V to 3.6 V	-	20	45	-	50	55	ns
		V _{CC} = 3.6 V to 4.3 V	-	20	45	-	50	55	ns
t _{dis}	disable time	nS to nZ or nYn; see Figure 22							
		V _{CC} = 1.4 V to 1.6 V	-	30	70	-	80	90	ns
		V _{CC} = 1.65 V to 1.95 V	-	18	55	-	60	65	ns
		V _{CC} = 2.3 V to 2.7 V	-	11	25	-	30	35	ns
		V _{CC} = 2.7 V to 3.6 V	-	9	20	-	25	30	ns
		V _{CC} = 3.6 V to 4.3 V	-	9	20	-	25	30	ns
t _{b-m}	break-before-make time	see Figure 23 ^[2]							
		V _{CC} = 1.4 V to 1.6 V	-	20	-	9	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	19	-	7	-	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	13	-	4	-	-	ns
		V _{CC} = 2.7 V to 3.6 V	-	10	-	2	-	-	ns
		V _{CC} = 3.6 V to 4.3 V	-	10	-	1	-	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

[2] Break-before-make guaranteed by design.

12.1 Waveform and test circuits

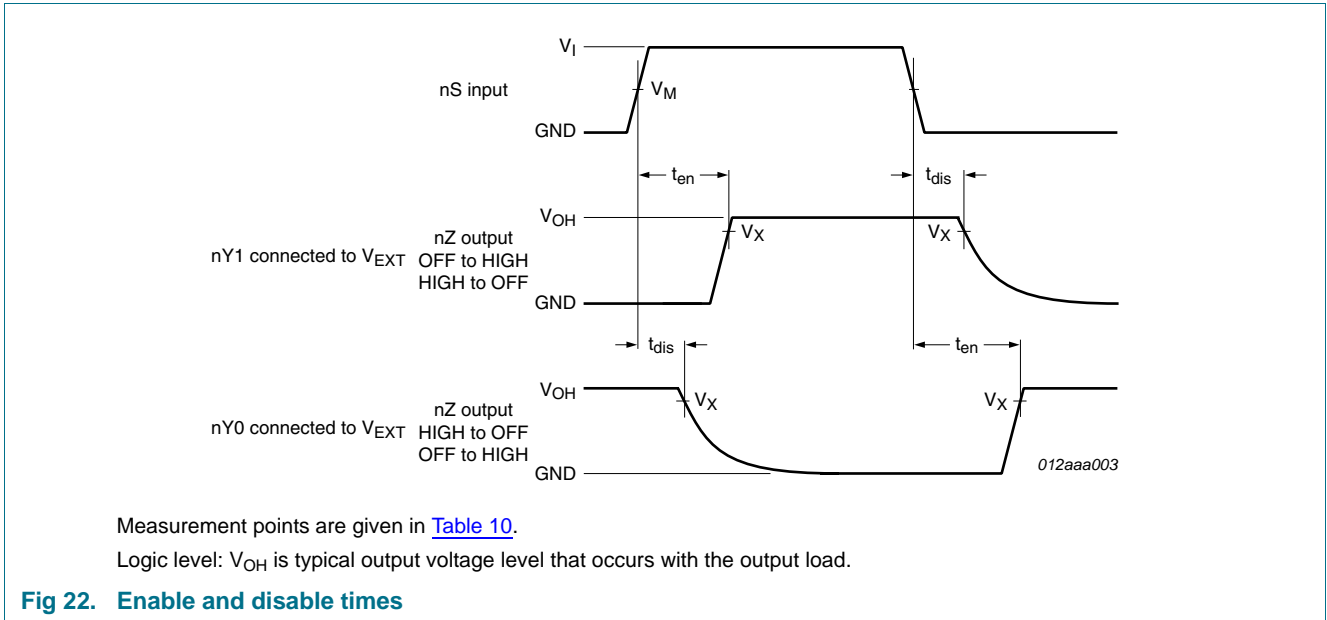


Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

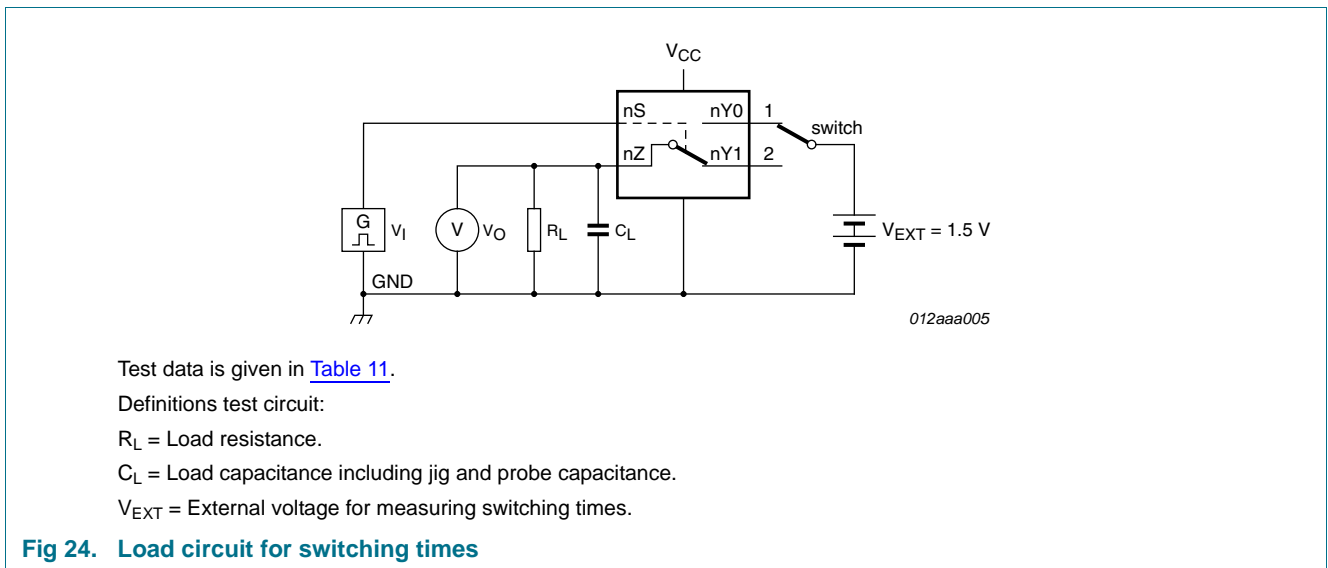
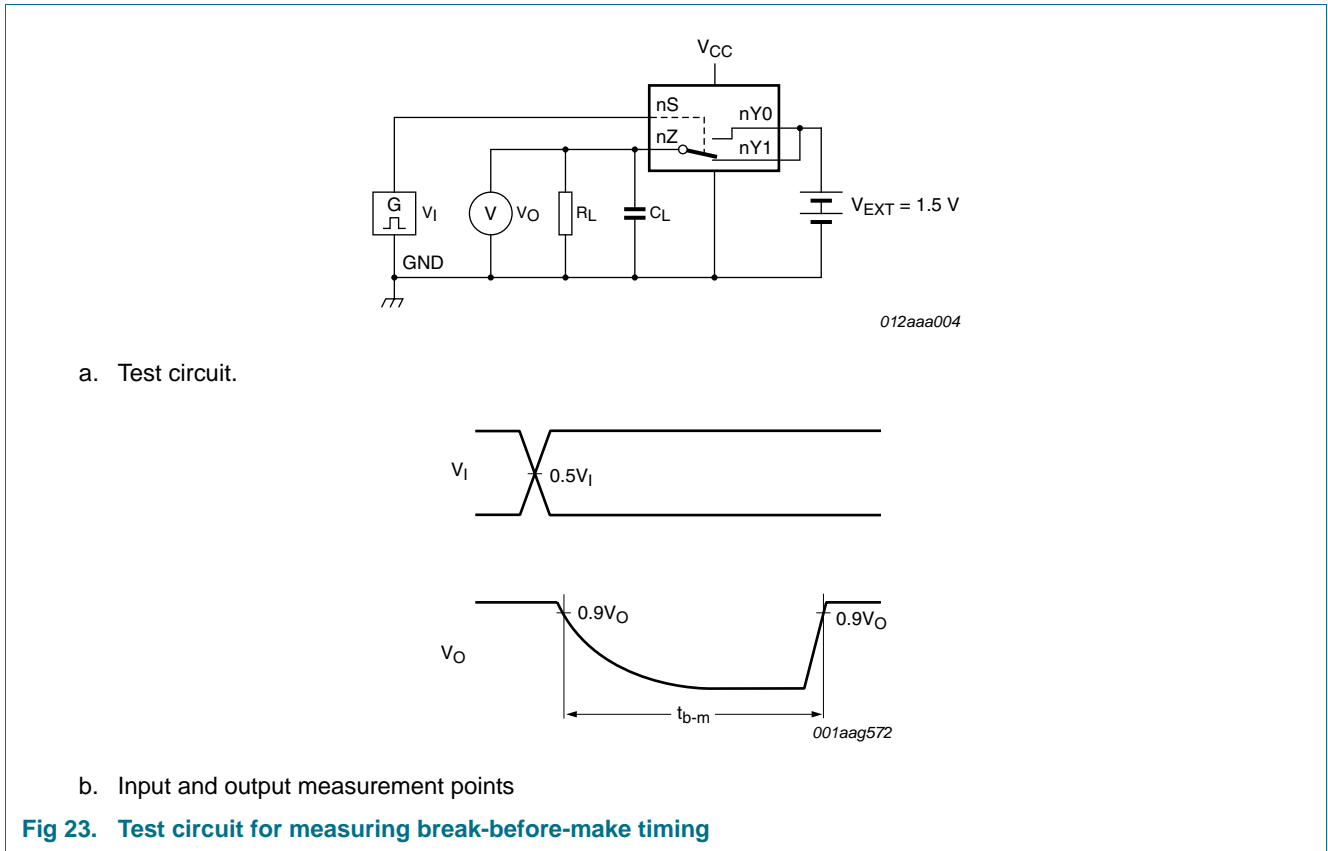


Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5 \text{ ns}$.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
THD	total harmonic distortion	$f_i = 20 \text{ Hz to } 20 \text{ kHz}; R_L = 32 \text{ } \Omega$; see Figure 25 [1]				
		$V_{CC} = 1.4 \text{ V}; V_I = 1 \text{ V (p-p)}$	-	0.06	-	%
		$V_{CC} = 1.65 \text{ V}; V_I = 1.2 \text{ V (p-p)}$	-	0.02	-	%
		$V_{CC} = 2.3 \text{ V}; V_I = 1.5 \text{ V (p-p)}$	-	0.02	-	%
		$V_{CC} = 2.7 \text{ V}; V_I = 2 \text{ V (p-p)}$	-	0.02	-	%
		$V_{CC} = 4.3 \text{ V}; V_I = 2 \text{ V (p-p)}$	-	0.02	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50 \text{ } \Omega$; see Figure 26 [1]				
		port nY0; $V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$	-	15	-	MHz
		port nY1; $V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$	-	20	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 100 \text{ kHz}; R_L = 50 \text{ } \Omega$; see Figure 27 [1]				
		$V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$	-	-90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}; C_L = 50 \text{ pF}; R_L = 50 \text{ } \Omega$; see Figure 28				
		$V_{CC} = 1.4 \text{ V to } 3.6 \text{ V}$	-	0.5	-	V
		$V_{CC} = 3.6 \text{ V to } 4.3 \text{ V}$	-	0.7	-	V
Xtalk	crosstalk	between switches; [1] $f_i = 100 \text{ kHz}; R_L = 50 \text{ } \Omega$; see Figure 29				
		$V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$	-	-90	-	dB
Q_{inj}	charge injection	$f_i = 1 \text{ MHz}; C_L = 0.1 \text{ nF}; R_L = 1 \text{ M}\Omega; V_{\text{gen}} = 0 \text{ V}; R_{\text{gen}} = 0 \text{ } \Omega$; see Figure 30				
		$V_{CC} = 1.5 \text{ V}$	-	10	-	pC
		$V_{CC} = 1.8 \text{ V}$	-	14	-	pC
		$V_{CC} = 2.5 \text{ V}$	-	21	-	pC
		$V_{CC} = 3.3 \text{ V}$	-	30	-	pC
		$V_{CC} = 4.3 \text{ V}$	-	50	-	pC

[1] f_i is biased at $0.5V_{CC}$.

12.3 Test circuits

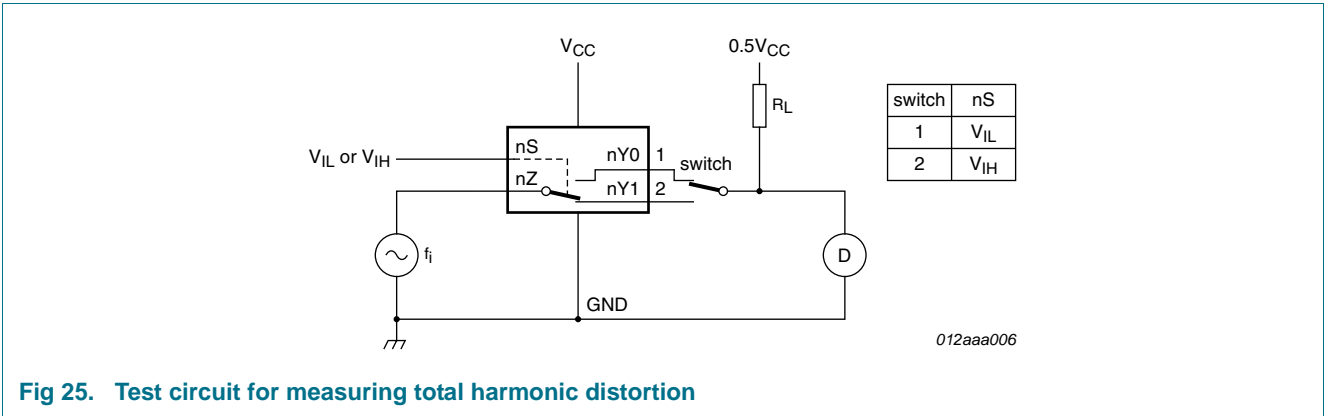


Fig 25. Test circuit for measuring total harmonic distortion

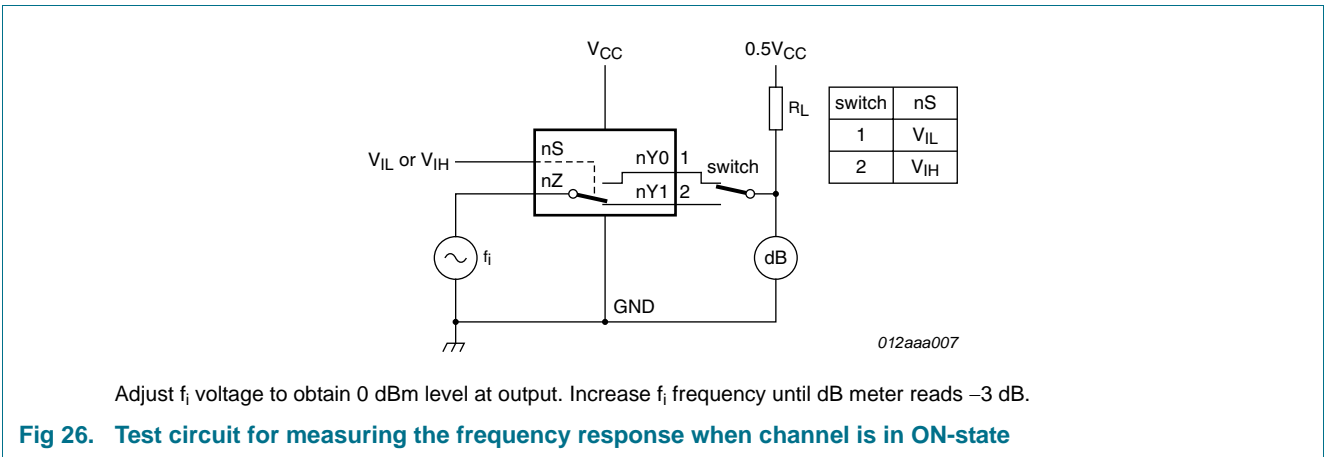


Fig 26. Test circuit for measuring the frequency response when channel is in ON-state

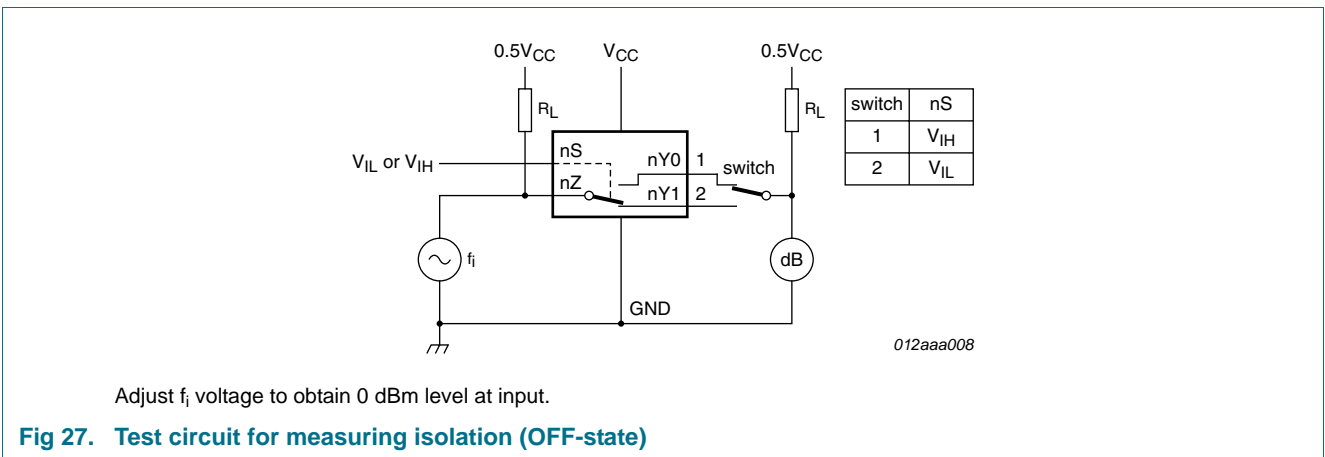
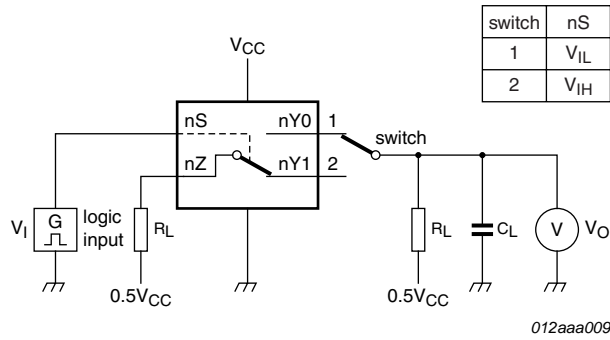
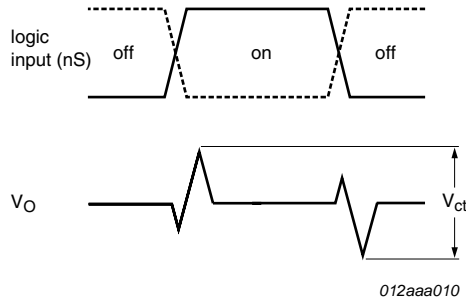


Fig 27. Test circuit for measuring isolation (OFF-state)

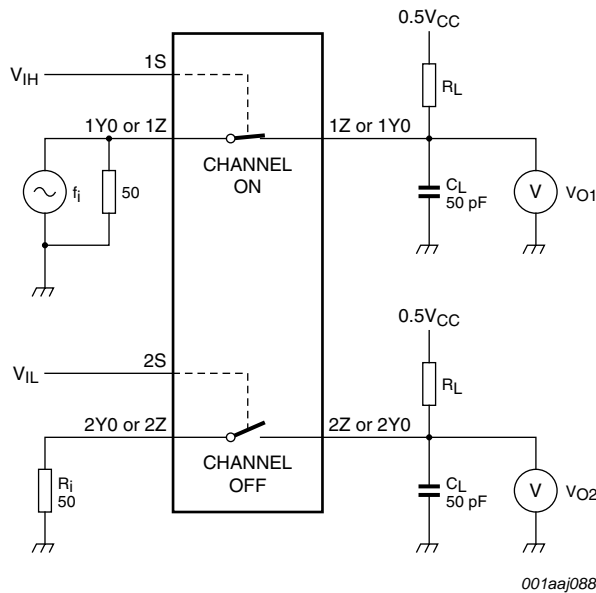


a. Test circuit



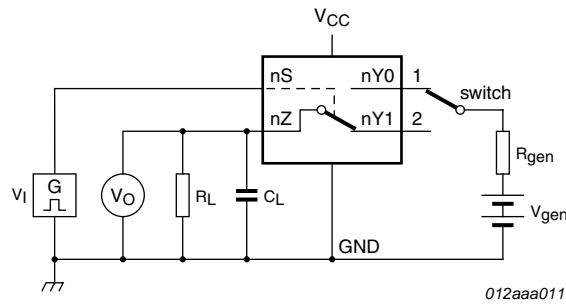
b. Input and output pulse definitions

Fig 28. Test circuit for measuring crosstalk voltage between digital inputs and switch

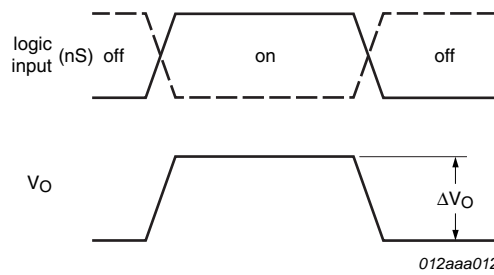


$$20 \log_{10} (V_{O2} / V_{O1}) \text{ or } 20 \log_{10} (V_{O1} / V_{O2}).$$

Fig 29. Test circuit for measuring crosstalk between switches



a. Test circuit.



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 30. Test circuit for measuring charge injection

13. Package outline

XQFN10U: plastic extremely thin quad flat package; no leads; 10 terminals;
UTLP based; body 2 x 1.55 x 0.5 mm

SOT1049-2

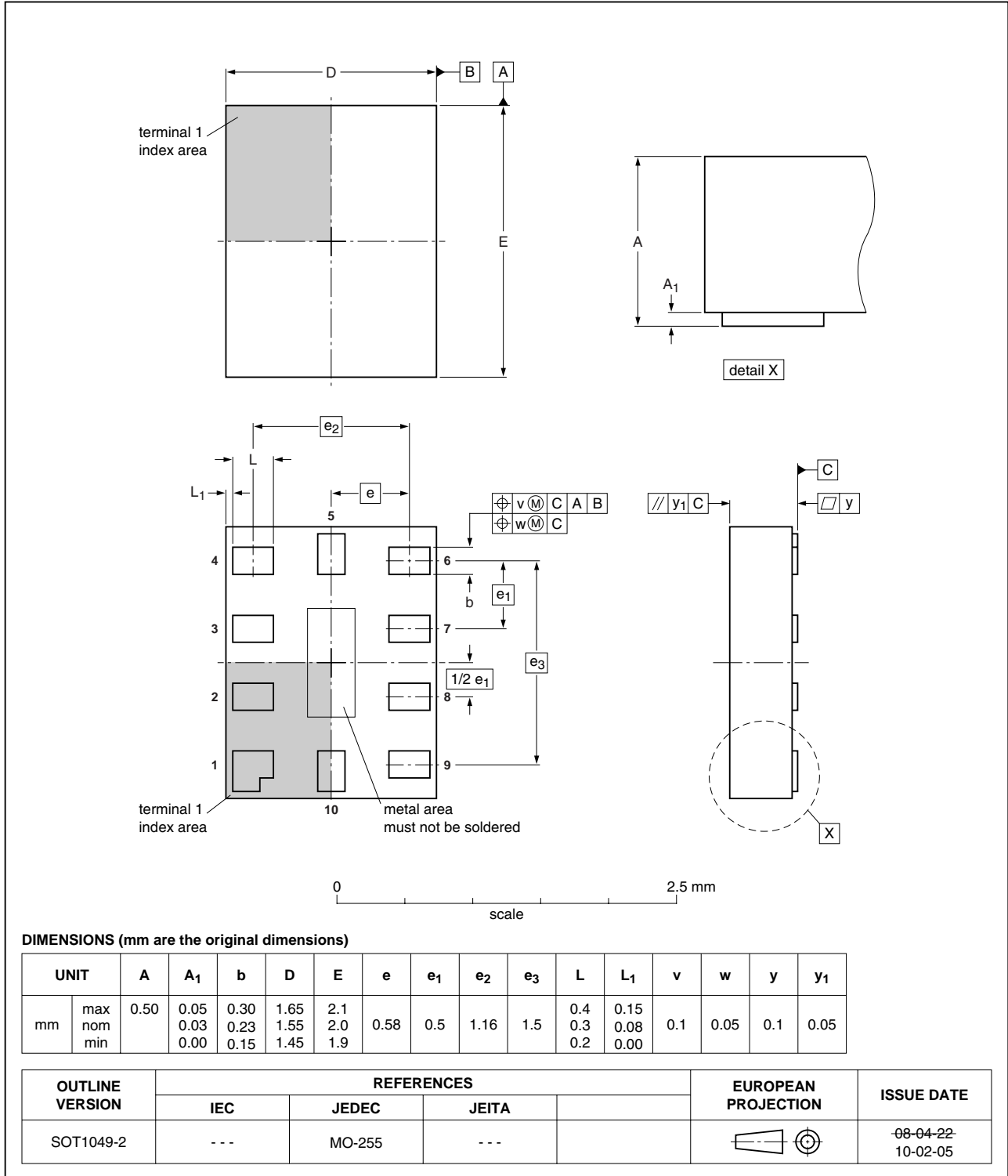


Fig 31. Package outline SOT1049-2 (XQFN10U)

**HVSON10: plastic thermal enhanced very thin small outline package; no leads;
10 terminals; body 3 x 3 x 0.85 mm**

SOT650-1

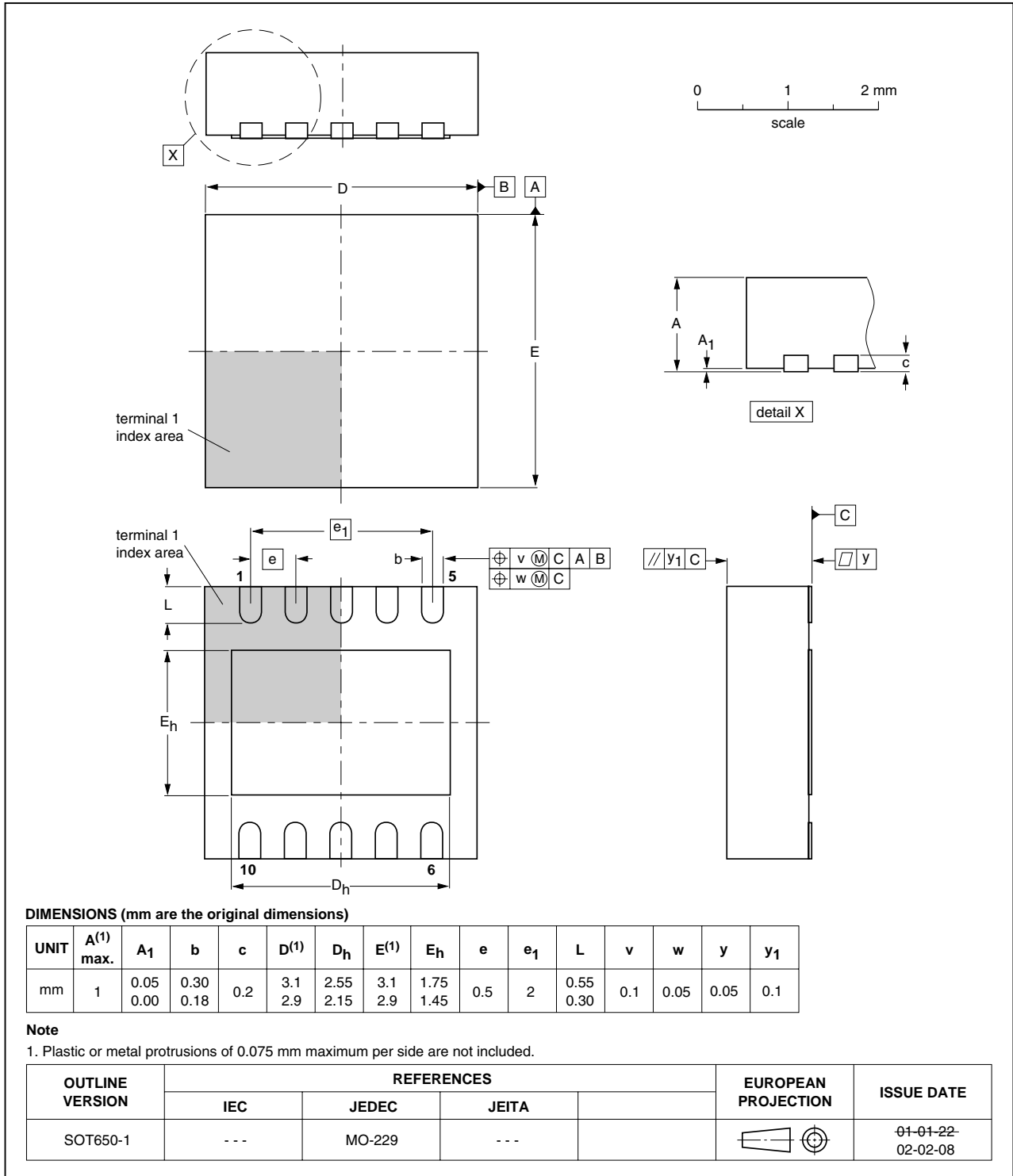


Fig 32. Package outline SOT650-1 (HVSON10)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3L4684_4	20100324	Product data sheet	-	NX3L4684_3
NX3L4684_3	20100209	Product data sheet	-	NX3L4684_2
Modifications:	<ul style="list-style-type: none"> • Table 8: ON resistance (flatness) for pins nY0 and nY1 changed at $V_{CC} = 4.3$ V. 			
NX3L4684_2	20090401	Product data sheet	-	NX3L4684_1
NX3L4684_1	20081127	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be

suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features	1
3	Applications	2
4	Ordering information	2
5	Marking	2
6	Functional diagram	2
7	Pinning information	3
7.1	Pinning	3
7.2	Pin description	3
8	Functional description	4
9	Limiting values	4
10	Recommended operating conditions	4
11	Static characteristics	5
11.1	Test circuits	6
11.2	ON resistance	7
11.3	ON resistance test circuit and graphs	8
12	Dynamic characteristics	12
12.1	Waveform and test circuits	13
12.2	Additional dynamic characteristics	15
12.3	Test circuits	16
13	Package outline	19
14	Abbreviations	21
15	Revision history	21
16	Legal information	22
16.1	Data sheet status	22
16.2	Definitions	22
16.3	Disclaimers	22
16.4	Trademarks	22
17	Contact information	23
18	Contents	24

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 March 2010

Document identifier: NX3L4684_4

founded by

PHILIPS