

FEATURES

- **Guaranteed Low Offset Voltage**

LT1001AM	15 μ V max
LT1001C	60 μ V max
- **Guaranteed Low Drift**

LT1001AM	0.6 μ V/ $^{\circ}$ C max
LT1001C	1.0 μ V/ $^{\circ}$ C max
- **Guaranteed Low Bias Current**

LT1001AM	2nA max
LT1001C	4nA max
- **Guaranteed CMRR**

LT1001AM	114dB min
LT1001C	110dB min
- **Guaranteed PSRR**

LT1001AM	110dB min
LT1001C	106dB min
- **Low Power Dissipation**

LT1001AM	75mW max
LT1001C	80mW max
- **Low Noise 0.3 μ V_{p-p}**

APPLICATIONS

- Thermocouple amplifiers
- Strain gauge amplifiers
- Low level signal processing
- High accuracy data acquisition

DESCRIPTION

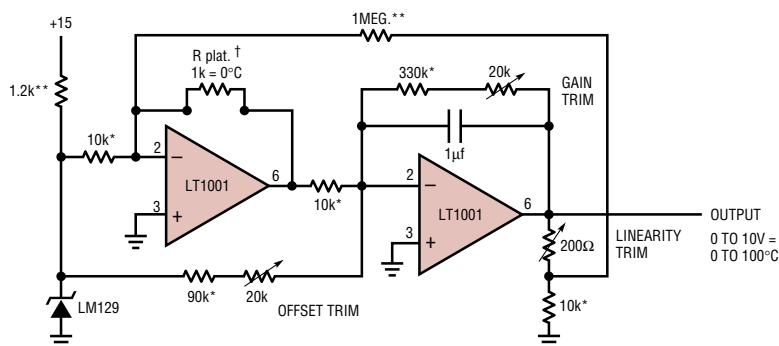
The LT[®]1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

Essentially, the input offset voltage of all units is less than 50 μ V (see distribution plot below). This allows the LT1001AM/883 to be specified at 15 μ V. Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer guaranteed performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the LT1001 is also enhanced with voltage gain guaranteed at 10mA of load current. For similar performance in a dual precision op amp, with guaranteed matching specifications, see the LT1002. Shown below is a platinum resistance thermometer application.

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TYPICAL APPLICATION

Linearized Platinum Resistance Thermometer
with $\pm 0.025^{\circ}$ C Accuracy Over 0 to 100° C

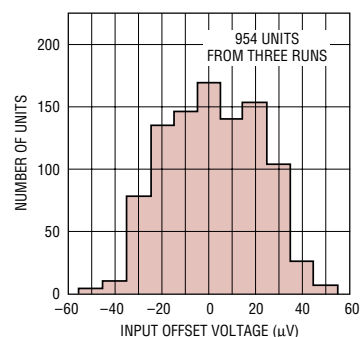


* ULTRONIX 105A WIREWOUND
** 1% FILM
† PLATINUM RTD
118MF (ROSEMOUNT, INC.)

‡ Trim sequence: trim offset (0° C = 1000.0 Ω), trim linearity (35° C = 1138.7 Ω), trim gain (100° C = 1392.6 Ω). Repeat until all three points are fixed with $\pm 0.025^{\circ}$ C.

1001 TA01

Typical Distribution of Offset Voltage
 $V_S = \pm 15V$, $T_A = 25^{\circ}$ C



1001 TA02

ABSOLUTE MAXIMUM RATINGS

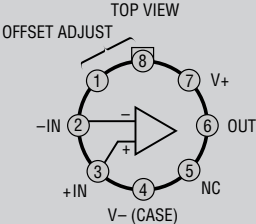
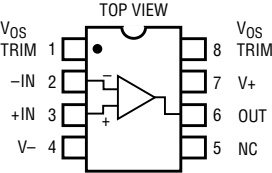
(Note 1)

Supply Voltage	$\pm 22\text{V}$
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	$\pm 22\text{V}$
Output Short Circuit Duration	Indefinite

Operating Temperature Range

LT1001AM/LT1001M (OBSOLETE) ..	-55°C to 150°C
LT1001AC/LT1001C	0°C to 125°C
Storage: All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW OFFSET ADJUST  H PACKAGE METAL CAN $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$, $\theta_{JC} = 45^{\circ}C/W$	ORDER PART NUMBER LT1001AMH/883 LT1001MH LT1001ACH LT1001CH	TOP VIEW  N8 PACKAGE 8 PIN PLASTIC DIP S8 PACKAGE 8 PIN PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$ (N) $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$ (S)	ORDER PART NUMBER LT1001ACN8 LT1001CN8 LT1001CS8
		S8 PART MARKING 1001	
		ORDER PART NUMBER LT1001AMJ8/883 LT1001MJ8 LT1001ACJ8 LT1001CJ8	
	OBSOLETE PACKAGE Consider the N8 and S8 Packages for Alternate Source		OBSOLETE PACKAGE Consider the N8 and S8 Packages for Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AM/883 LT1001AC			LT1001M/LT1001C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	Note 2	LT1001AM/883	7	15	18	60		μV	
			LT1001AC	10	25					
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability	Notes 3 and 4		0.2	1.0	0.3	1.5		μV/month	
I _{OS}	Input Offset Current			0.3	2.0	0.4	3.8		nA	
I _b	Input Bias Current			±0.5	±2.0	±0.7	±4.0		nA	
e _n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		0.3	0.6	0.3	0.6		μV _{p-p}	
e _n	Input Noise Voltage Density	f ₀ = 10Hz (Note 6)		10.3	18.0	10.5	18.0		nV/√Hz	
		f ₀ = 1000Hz (Note 3)		9.6	11.0	9.8	11.0		nV/√Hz	
A _{VOL}	Large Signal Voltage Gain	R _L ≥ 2kΩ, V _O = ±12V		450	800	400	800		V/mV	
		R _L ≥ 1kΩ V _O = ±10V		300	500	250	500		V/mV	
CMRR	Common Mode Rejection Ratio	V _{CM} = ±13V		114	126	110	126		dB	
PSRR	Power Supply Rejection Ratio	V _S = ±3V to ±18V		110	123	106	123		dB	
R _{in}	Input Resistance Differential Mode			30	100	15	80		MΩ	

1001fb

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883 LT1001AC			LT1001M/LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Voltage Range		± 13	± 14		± 13	± 14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	± 13	± 14		± 13	± 14		V
		$R_L \geq 1\text{k}\Omega$	± 12	± 13.5		± 12	± 13.5		V
S_R	Slew Rate	$R_L \geq 2\text{k}\Omega$ (Note 5)	0.1	0.25		0.1	0.25		V/ μs
GBW	Gain-Bandwidth Product	(Note 5)	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation	No load		46	75		48	80	mW
		No load, $V_S = \pm 3\text{V}$		4	6		4	8	mW

$V_S = \pm 15\text{V}$, $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AM/883			LT1001M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●		30	60		45	160	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Offset Voltage Drift		●		0.2	0.6		0.3	1.0	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●		0.8	4.0		1.2	7.6	nA
I_B	Input Bias Current		●		± 1.0	± 4.0		± 1.5	± 8.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	●	300	700		200	700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13\text{V}$	●	110	122		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ to $\pm 18\text{V}$	●	104	117		100	117		dB
	Input Voltage Range		●	± 13	± 14		± 13	± 14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	●	± 12.5	± 13.5		± 12.0	± 13.5		V
P_d	Power Dissipation	No load	●		55	90		60	100	mW

$V_S = \pm 15\text{V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AC			LT1001C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●		20	60		30	110	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Offset Voltage Drift		●		0.2	0.6		0.3	1.0	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●		0.5	3.5		0.6	5.3	nA
I_B	Input Bias Current		●		± 0.7	± 3.5		± 1.0	± 5.5	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	●	350	750		250	750		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13\text{V}$	●	110	124		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3\text{V}$ to $\pm 18\text{V}$	●	106	120		103	120		dB
	Input Voltage Range		●	± 13	± 14		± 13	± 14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	●	± 12.5	± 13.8		± 12.5	± 13.8		V
P_d	Power Dissipation	No load	●		50	85		55	90	mW

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Offset voltage for the LT1001AM/883 and LT1001AC are measured after power is applied and the device is fully warmed up. All other grades are measured with high speed test equipment, approximately 1 second after power is applied. The LT1001AM/883 receives 168 hr. burn-in at 125°C . or equivalent.

Note 3: This parameter is tested on a sample basis only.

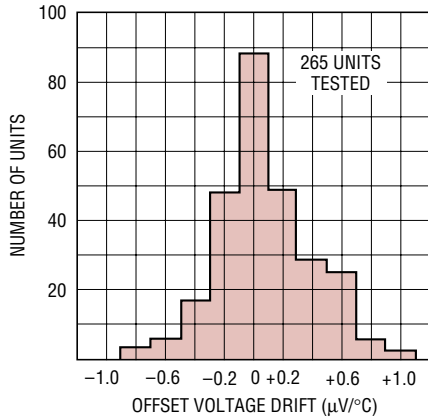
Note 4: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu\text{V}$.

Note 5: Parameter is guaranteed by design.

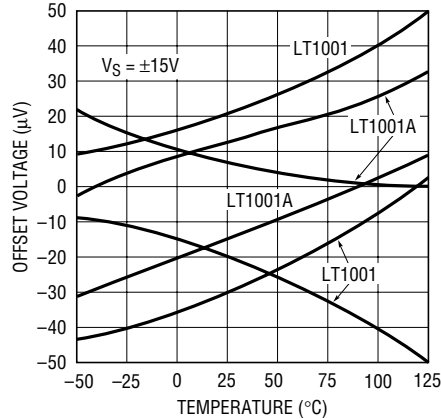
Note 6: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

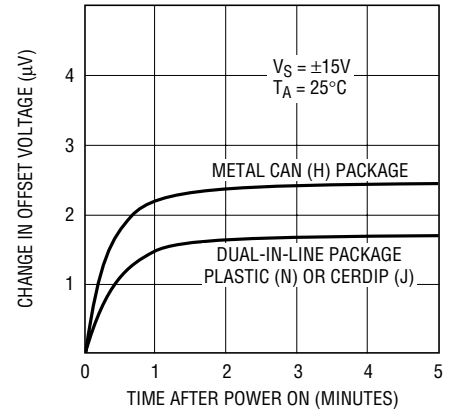
Typical Distribution of Offset Voltage Drift with Temperature



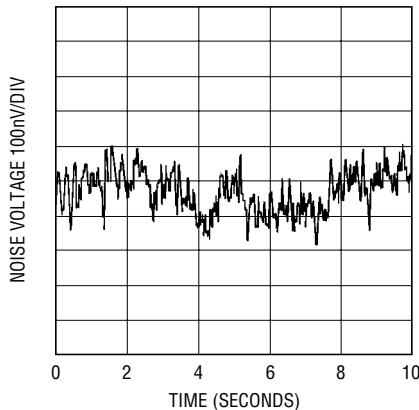
Offset Voltage Drift with Temperature of Representative Units



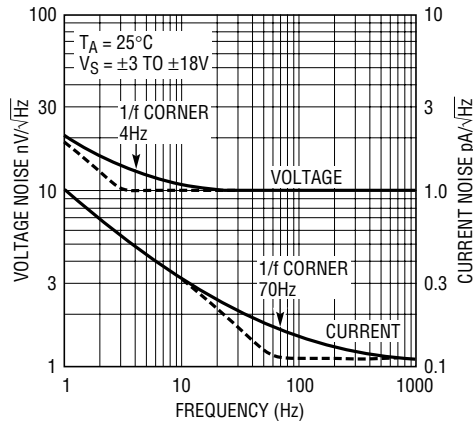
Warm-Up Drift



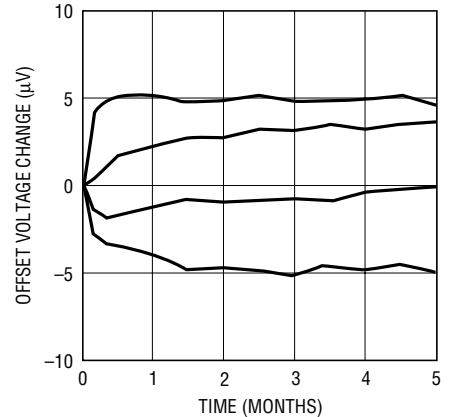
0.1Hz to 10Hz Noise



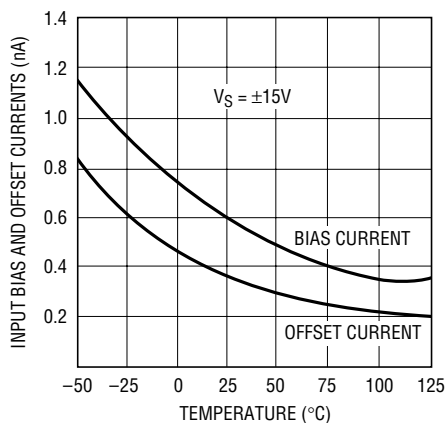
Noise Spectrum



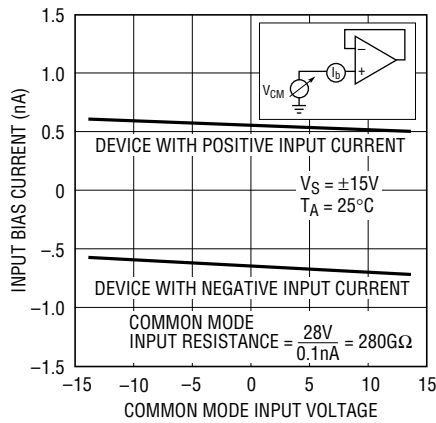
Long Term Stability of Four Representative Units



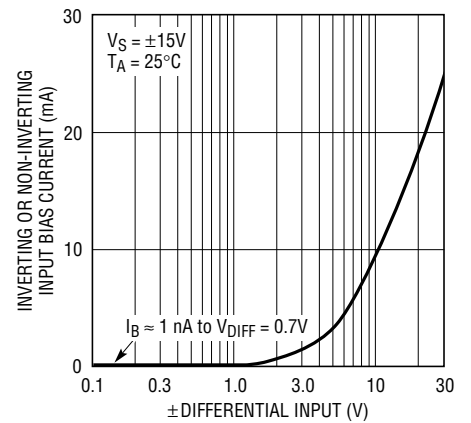
Input Bias and Offset Current vs Temperature



Input Bias Current Over the Common Mode Range

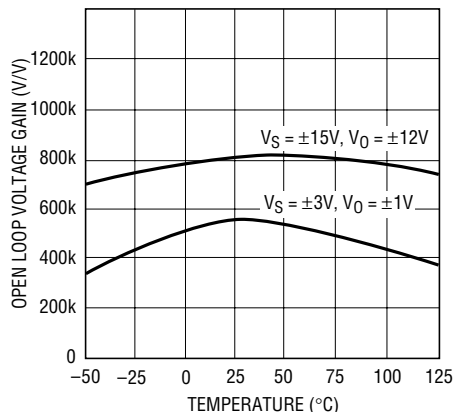


Input Bias Current vs Differential Input Voltage

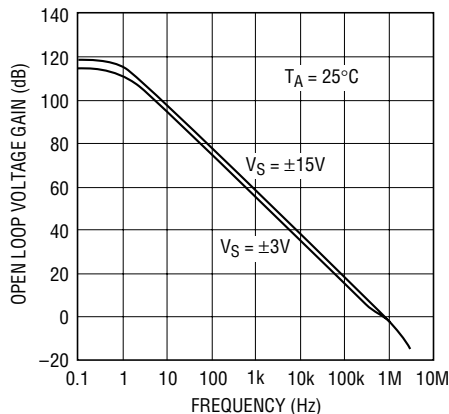


TYPICAL PERFORMANCE CHARACTERISTICS

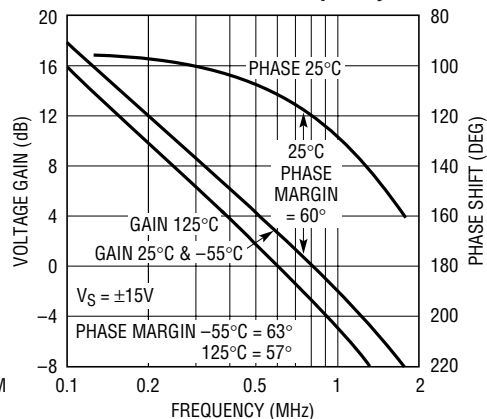
Open Loop Voltage Gain vs Temperature



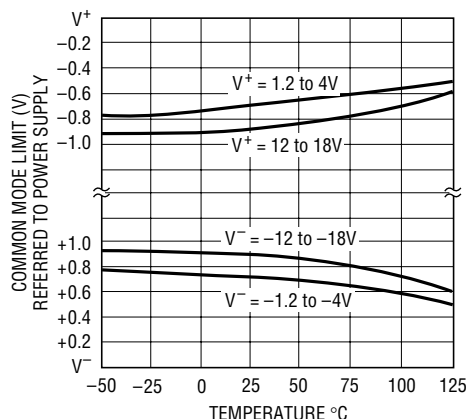
Open Loop Voltage Gain Frequency Response



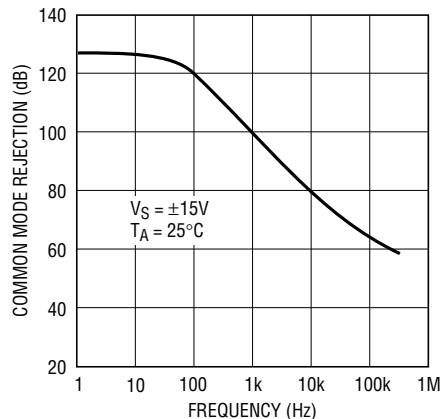
Gain, Phase Shift vs Frequency



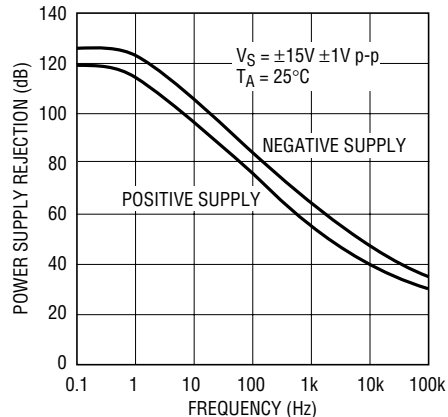
Common Mode Limit vs Temperature



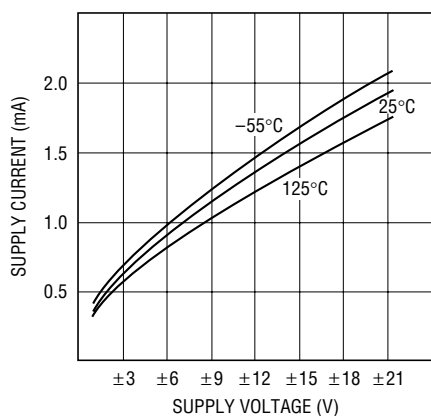
Common Mode Rejection Ratio vs Frequency



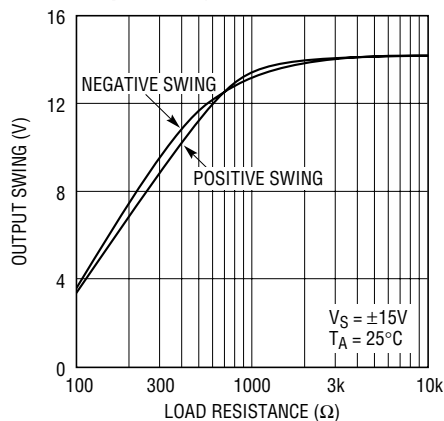
Power Supply Rejection Ratio vs Frequency



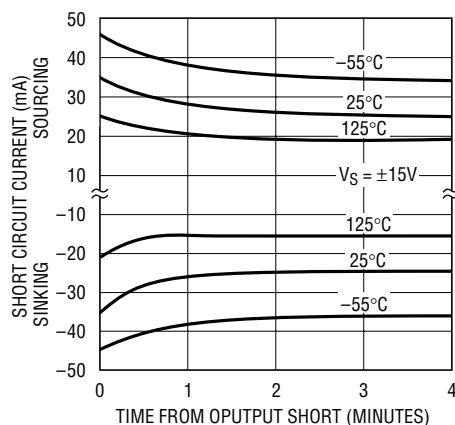
Supply Current vs Supply Voltage



Output Swing vs Load Resistance

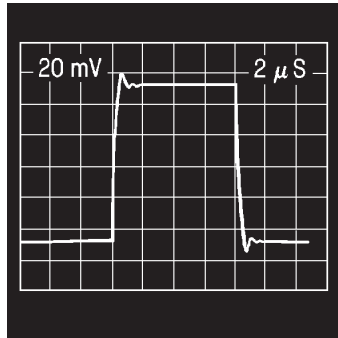


Output Short-Circuit Current vs Time



TYPICAL PERFORMANCE CHARACTERISTICS

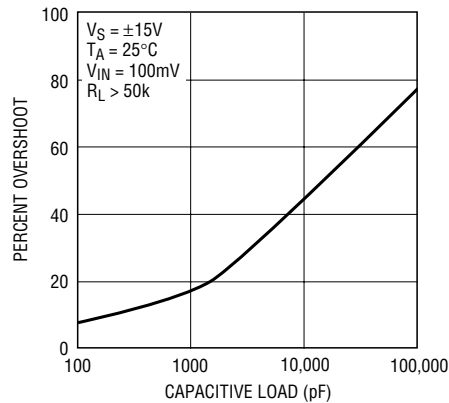
Small Signal Transient Response



$A_V = +1$, $C_L = 50\text{pF}$

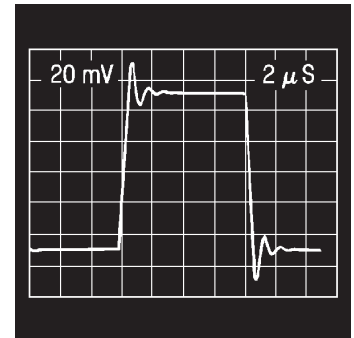
1001 G19

Voltage Follower Overshoot vs Capacitive Load



1001 G20

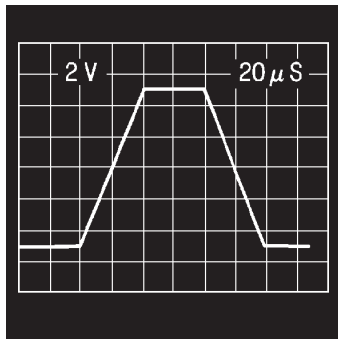
Small Signal Transient Response



$A_V = +1$, $C_L = 1000\text{pF}$

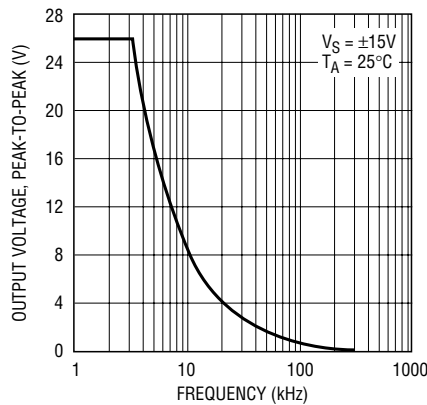
1001 G21

Large Signal Transient Response



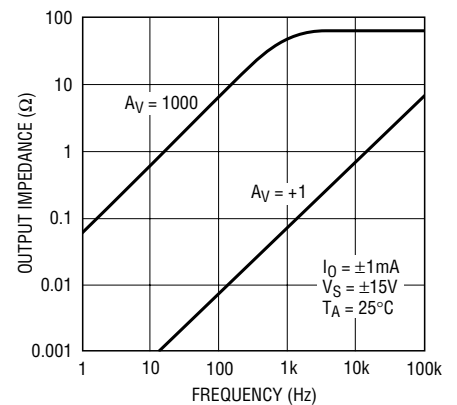
1001 G22

Maximum Undistorted Output vs. Frequency



1001 G23

Closed Loop Output Impedance



1001 G24

APPLICATIONS INFORMATION

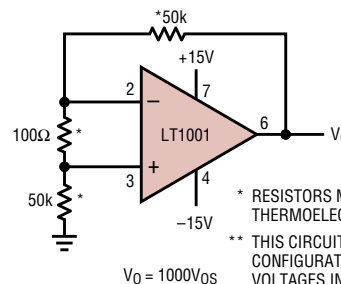
Application Notes and Test Circuits

The LT1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1001 is specified over a wide range of power supply voltages from $\pm 3\text{V}$ to $\pm 18\text{V}$. Operation with lower supplies is possible down to $\pm 1.2\text{V}$ (two Ni-Cad batteries). However, with $\pm 1.2\text{V}$ supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature



* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

** THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1001, WITH SUPPLY VOLTAGES INCREASED TO $\pm 20\text{V}$.

$V_O = 1000V_{OS}$

1001 F01

1001fb

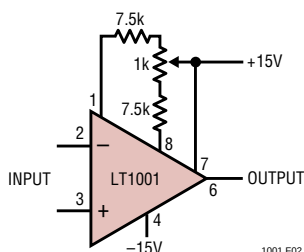
APPLICATIONS INFORMATION

Offset Voltage Adjustment

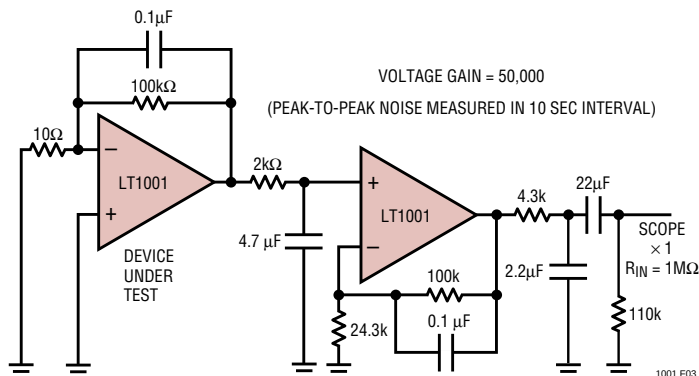
The input offset voltage of the LT1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of V_{os} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{os}/300)\mu V/^{\circ}C$, e.g., if V_{os} is

adjusted to $300\mu V$, the change in drift will be $1\mu V/^{\circ}C$. The adjustment range with a 10k or 20k pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of $\pm 100\mu V$.

Improved Sensitivity Adjustment

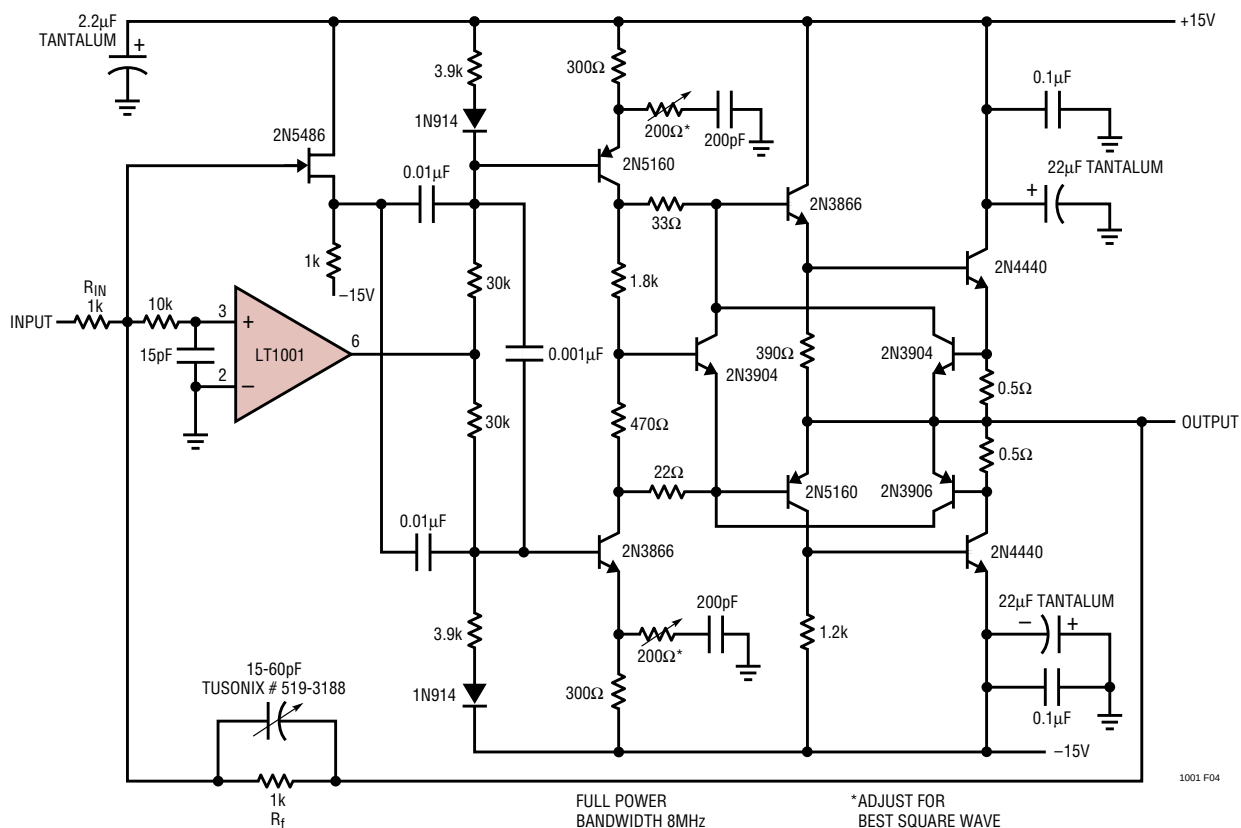


0.1Hz to 10Hz Noise Test Circuit



The device under test should be warmed up for three minutes and shielded from air currents.

DC Stabilized 1000v/μsec Op Amp



NON INVERTING INPUT

INVERTING INPUT

LT1001

5V

1.21M 1%

39.2Ω 1%

4.99k 1%

20k 5%

5k 5%

OUTPUT

2N3904

IN914

-5V

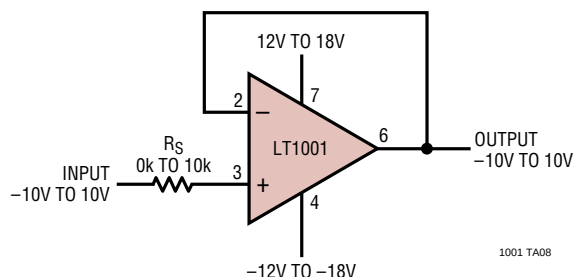
POSITIVE FEEDBACK TO ONE OF THE NULLING TERMINALS CREATES 5μ TO 20μV OF HYSTERESIS. INPUT OFFSET VOLTAGE IS TYPICALLY CHANGED BY LESS THAN 5μV DUE TO THE FEEDBACK.

1001 TA03

The diagram shows an LT1001 op-amp configured as a Class AB output stage. The op-amp's non-inverting input (+) is connected to V_{IN} (0 to $V^+ - 1V$). Its inverting input (-) is connected to the output. The op-amp is powered by $V^+ = 2V$ to $35V$ (pin 7) and $-5V$ (pin 4). The output of the op-amp (pin 6) drives the base of a 2N3685 PNP transistor. The emitter of the 2N3685 is connected to a 10K resistor, which is in turn connected to the base of a 2N2219 NPN transistor. The emitter of the 2N2219 is also connected to a 10K resistor, which is connected to ground. The collector of the 2N2219 is connected to the output node, which is also connected to a load resistor R to ground. The output current $I_{OUT} = \frac{V_{IN}}{R}$ is indicated. The 10K resistors are used for thermal matching between the two transistors.

[illegible]

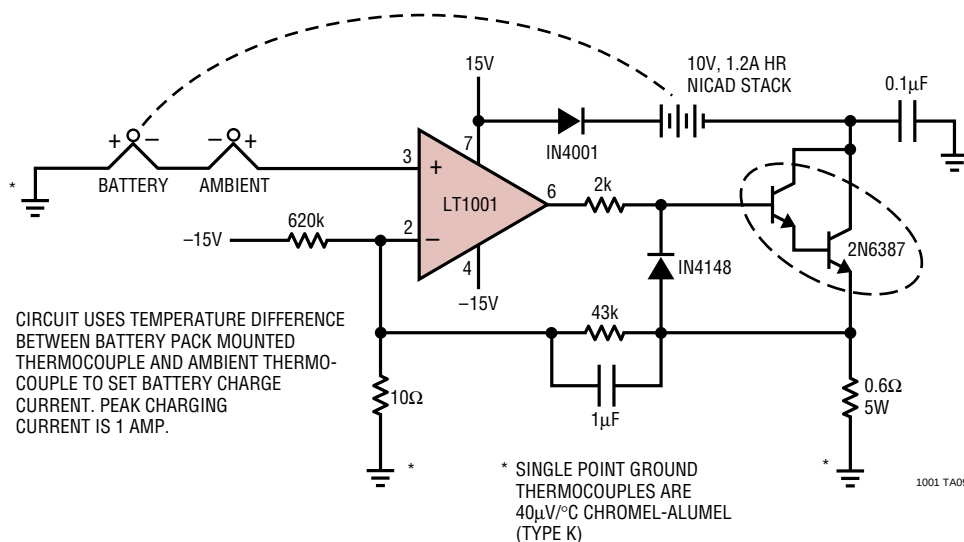
rejections. Worst-case summation of guaranteed specifications is tabulated below.



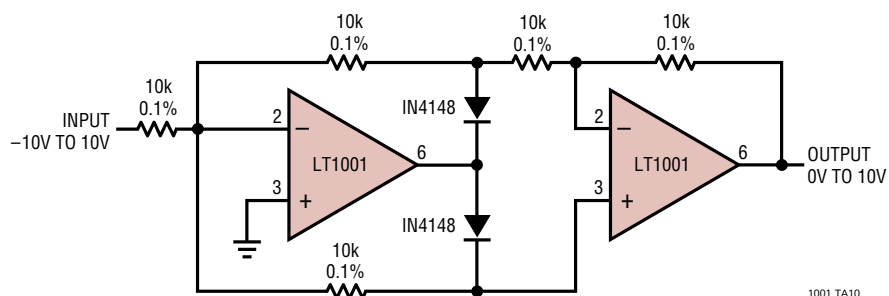
The voltage follower is an ideal example illustrating the overall excellence of the LT1001. The contributing error terms are due to offset voltage, input bias current, voltage gain, common mode and power-supply

OUTPUT ACCURACY				
Error	LT1001AM /883	LT1001C	LT1001AM /883	LT1001C
	25°C Max.	25°C Max.	-55 to 125°C Max.	0 to 70°C Max.
Offset Voltage	15µV	60µV	60µV	110µV
Bias Current	20µV	40µV	40µV	55µV
Common Mode Rejection	20µV	30µV	30µV	50µV
Power Supply Rejection	18µV	30µV	36µV	42µV
Voltage Gain	22µV	25µV	33µV	40µV
Worst-case Sum	95µV	185µV	199µV	297µV
Percent of Full Scale (=20V)	0.0005%	0.0009%	0.0010%	0.0015%

Thermally Controlled NiCad Charger

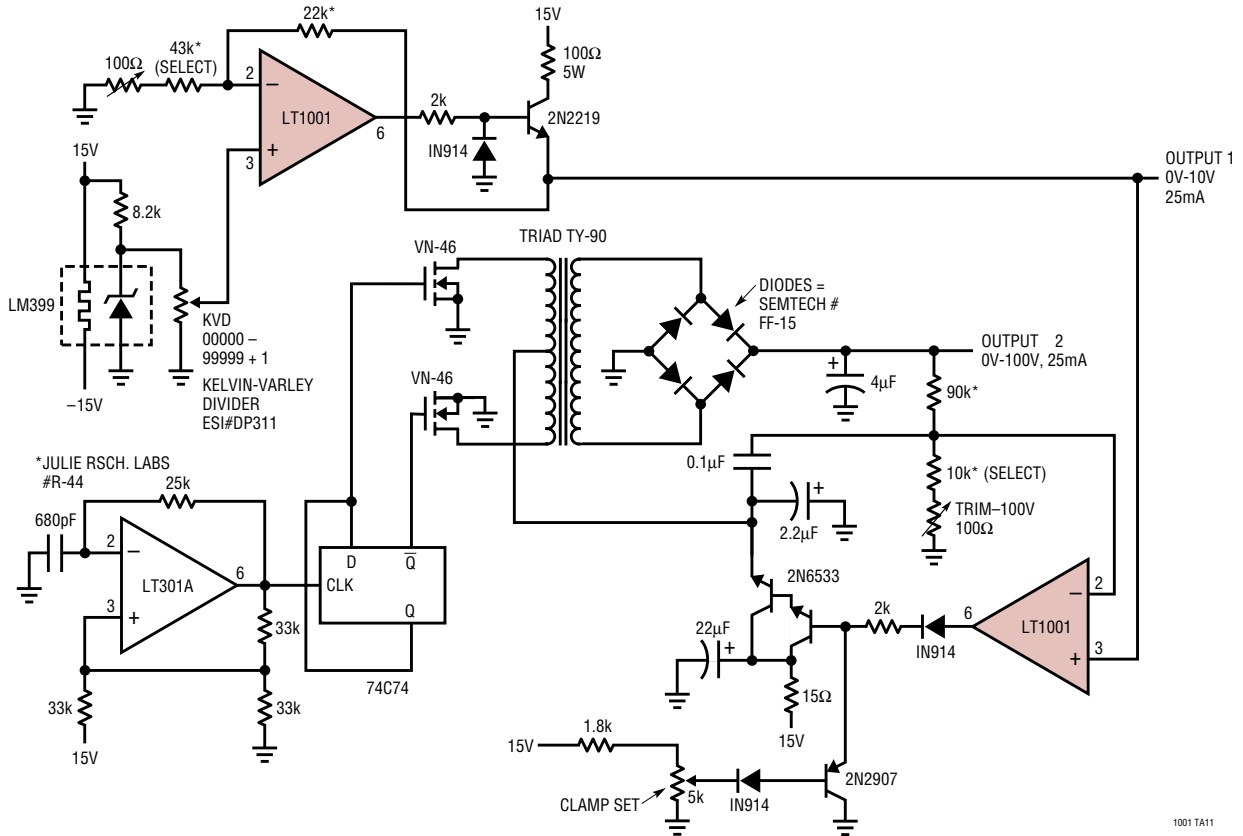


Precision Absolute Value Circuit



TYPICAL APPLICATIONS

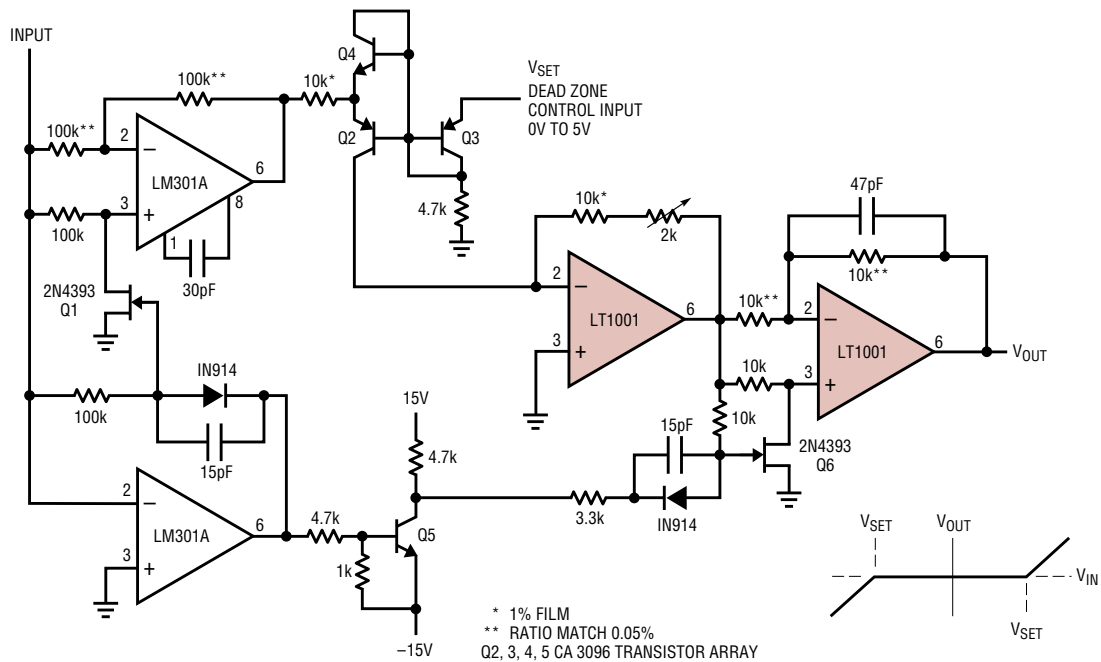
Precision Power Supply with Two Outputs
(1) 0V to 10V in 100 μ V STEPS (2) 0V to 100V in 1mV STEPS



1001 TA11

Dead Zone Generator

BIPOLAR SYMMETRY IS EXCELLENT BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS



* 1% FILM
** RATIO MATCH 0.05%
Q2, 3, 4, 5 CA 3096 TRANSISTOR ARRAY

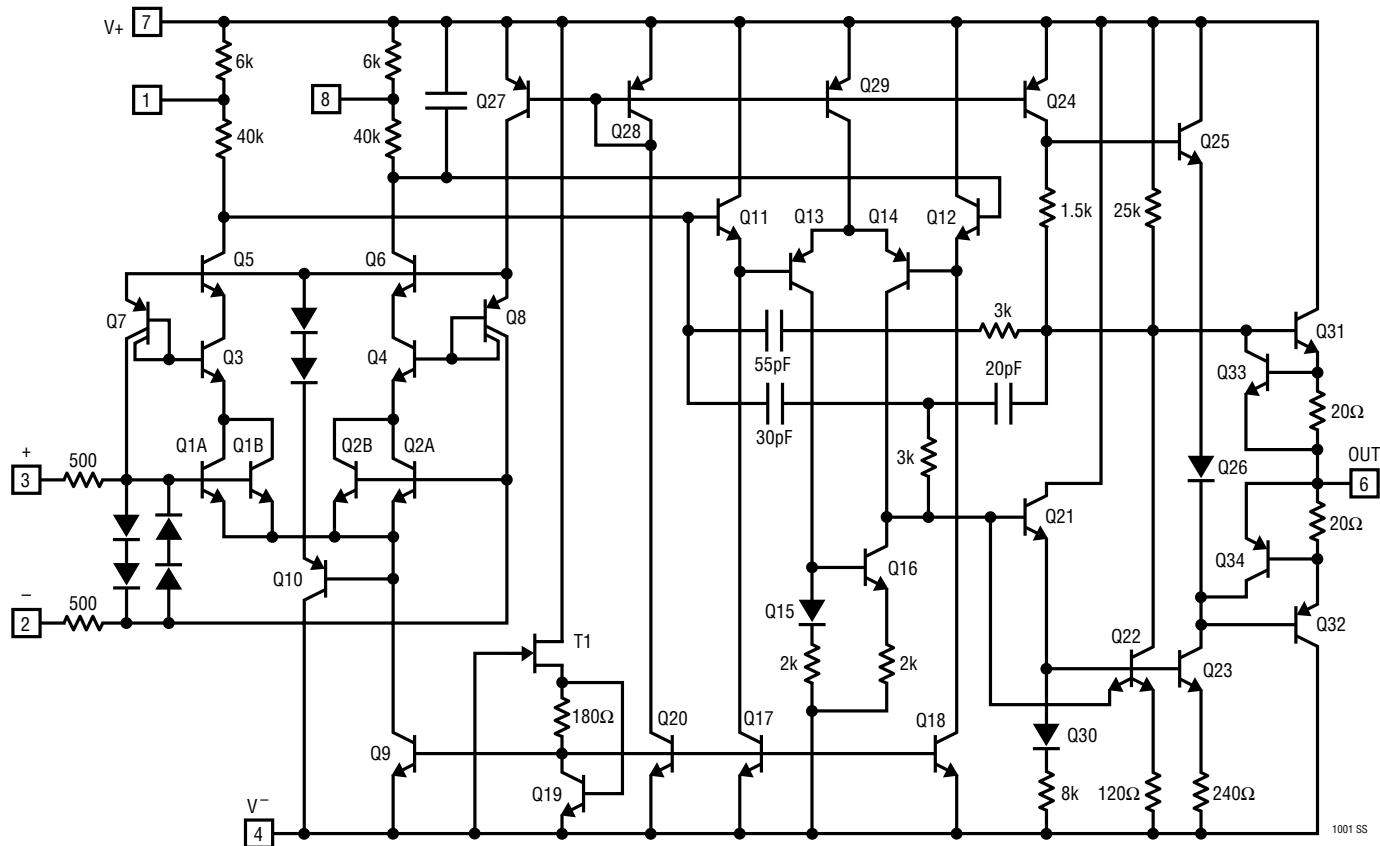
1001 TA12

1001fb

1) ALL DIODES IN4148
 2) S1-S4 OPTO MOS SWITCH OFM-1A, THETA-J CORP.
 3) *FILM RESISTOR
 4) **POLYPROPYLENE CAPACITORS
 5) ADJUST R1 FOR 93 Hz AT TEST POINT A

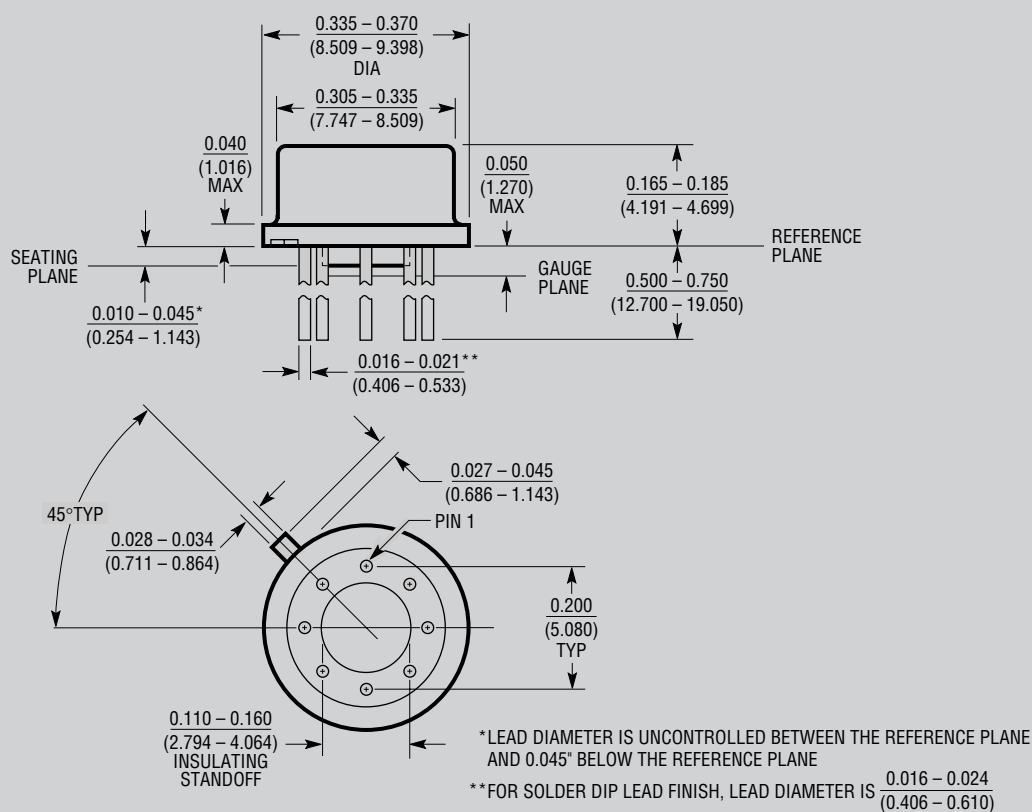
A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO-DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON MODE VOLTAGE TO A SINGLE ENDED SIGNAL AT THE LT1001 OUTPUT.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.200 Inch PCD)
 (Reference LTC DWG # 05-08-1320)

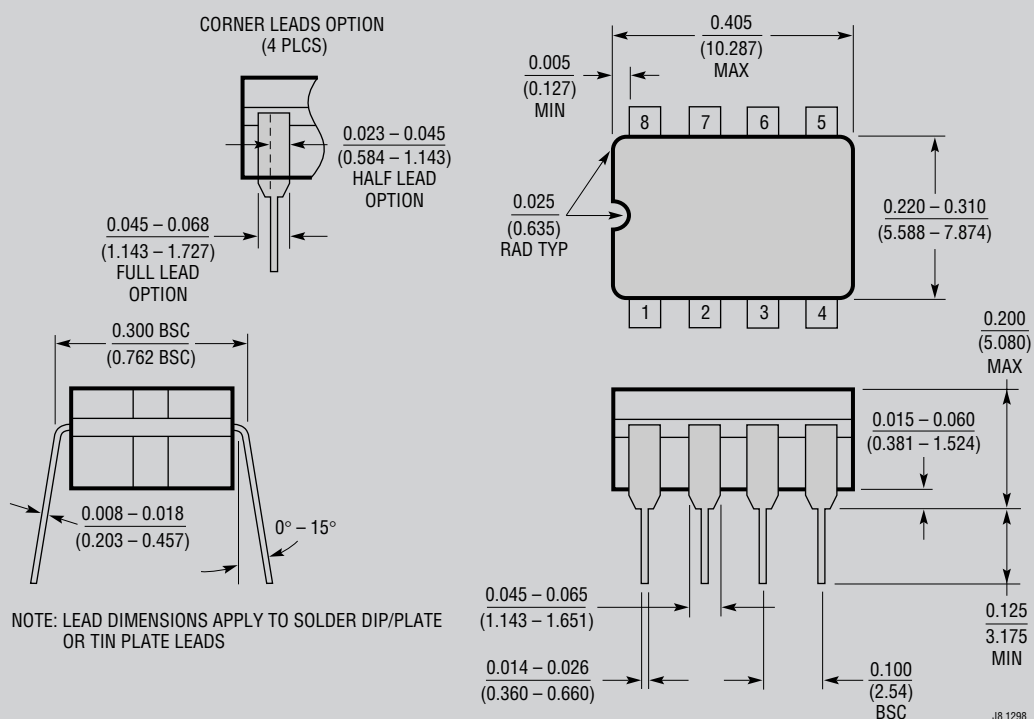


H8(TO-5) 0.200 PCD 1197

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

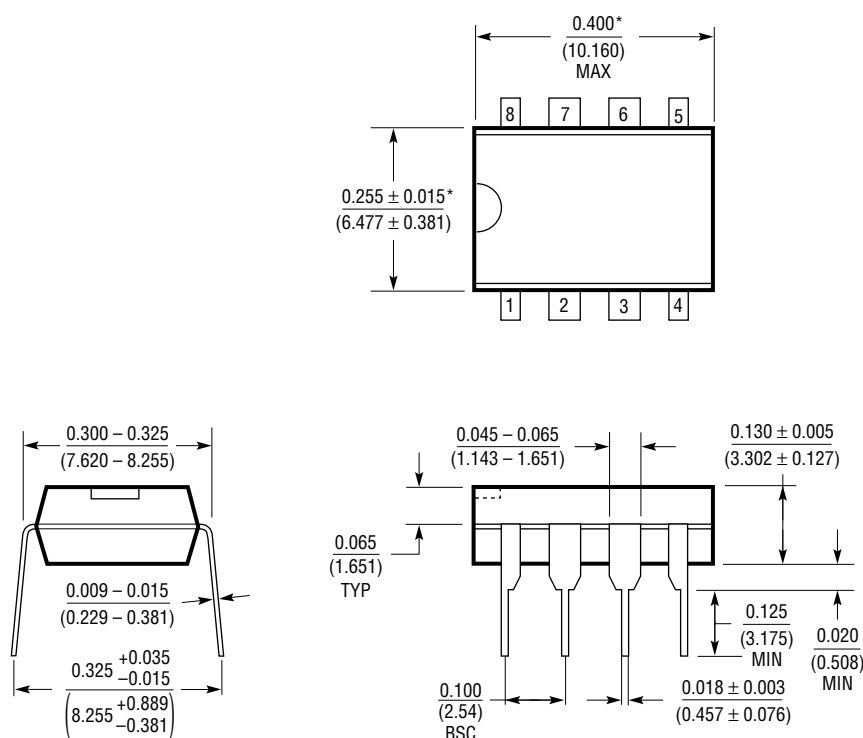
J8 Package 8-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)

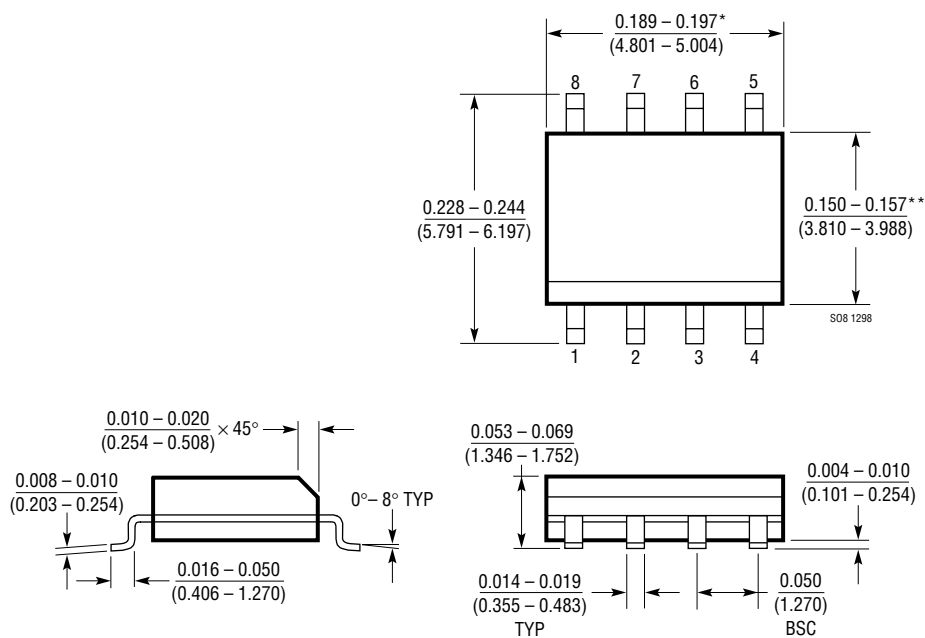


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N8 1098

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
 (Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE