



BUK7608-40B

N-channel TrenchMOS standard level FET

Rev. 04 — 24 September 2008

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

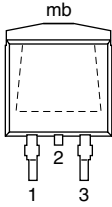
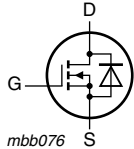
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3 ;	[1]	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	157	W
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	241	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $T_j = 25\text{ °C}$; see Figure 14	-	12	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12 ; see Figure 11	-	6.6	8	m Ω

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT404 (D2PAK)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK7608-40B	D2PAK	Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3 ; [1]	-	101	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; [1]	-	71	A
		$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3 ; [2]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 3	-	407	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	157	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$; [1]	-	101	A
		$T_{mb} = 25\text{ °C}$; [2]	-	75	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	407	A

Table 4. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	-	241	mJ

- [1] Current is limited by power dissipation chip rating.
[2] Continuous current is limited by package.

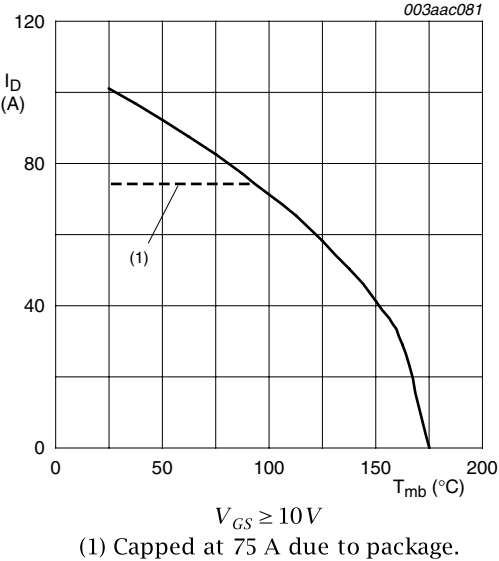


Fig 1. Continuous drain current as a function of mounting base temperature

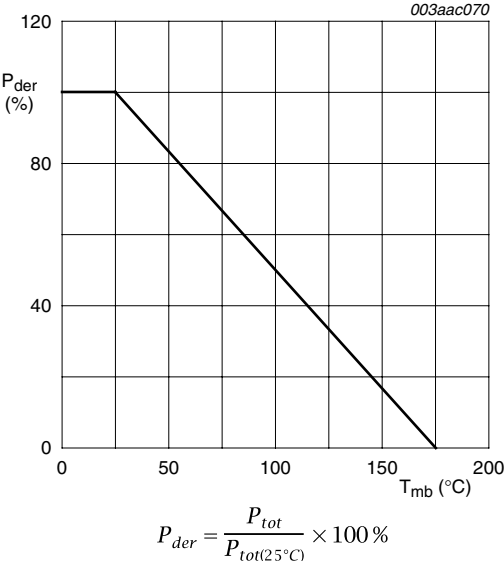


Fig 2. Normalized total power dissipation as a function of solder point temperature

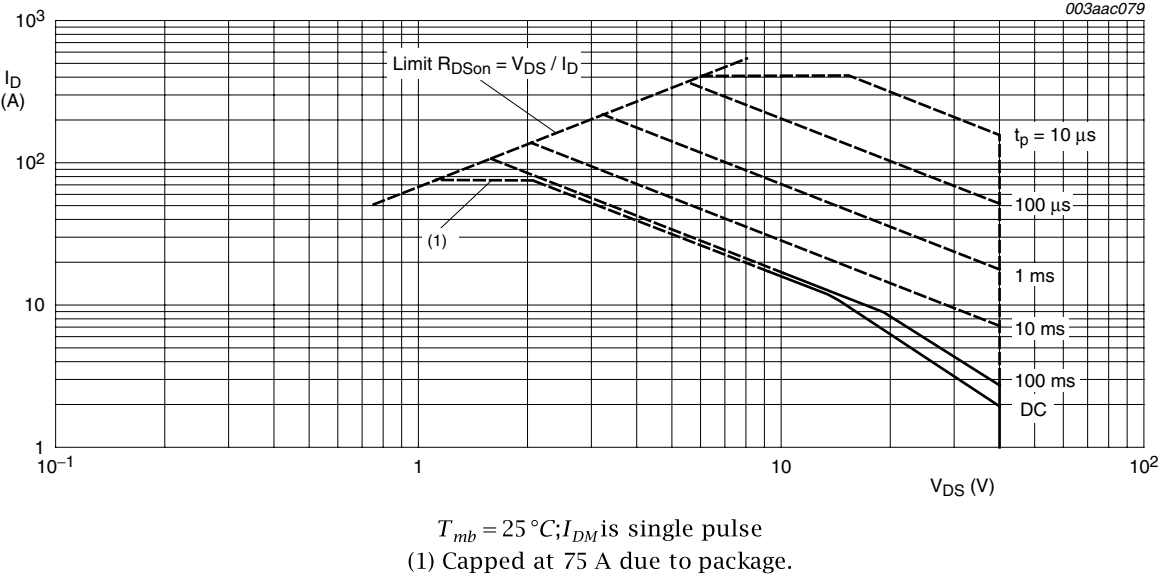


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-s

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W

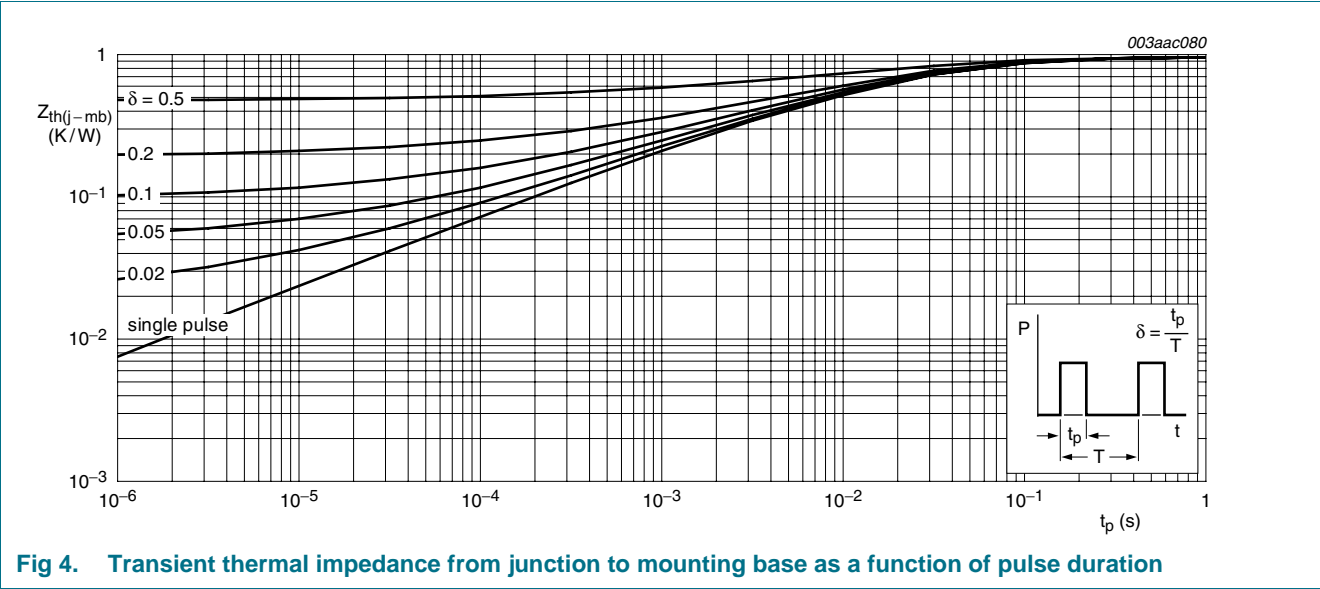
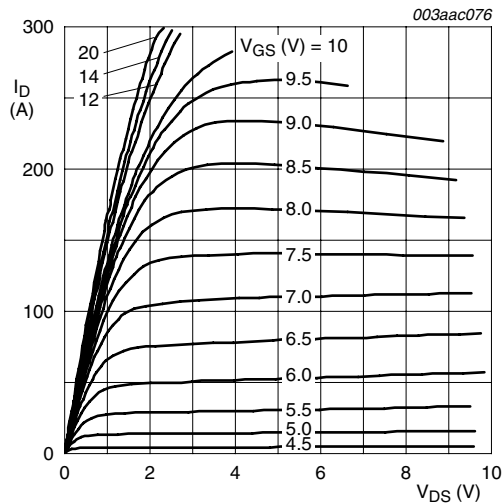


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

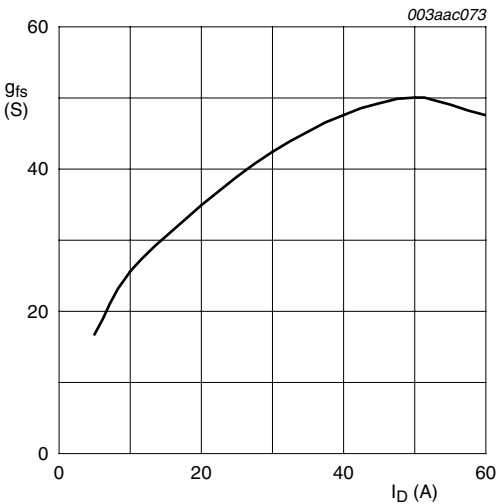
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	40	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 9 ; see Figure 10	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 9 ; see Figure 10	-	-	4.4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 9 ; see Figure 10	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	µA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	µA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 20 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -20 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 11 ; see Figure 12	-	-	15.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 12 ; see Figure 11	-	6.6	8	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 14	-	36	-	nC
Q _{GS}	gate-source charge		-	9	-	nC
Q _{GD}	gate-drain charge		-	12	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 15	-	2017	2689	pF
C _{oss}	output capacitance		-	486	583	pF
C _{rss}	reverse transfer capacitance		-	213	291	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	20	-	ns
t _r	rise time		-	51	-	ns
t _{d(off)}	turn-off delay time		-	20	-	ns
t _f	fall time		-	33	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to center of die; T _j = 25 °C	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	from source lead 6 mm from package to source bond pad; T _j = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/µs; V _{GS} = -10 V; V _{DS} = 20 V; T _j = 25 °C	-	53	-	ns
Q _r	recovered charge		-	44	-	nC



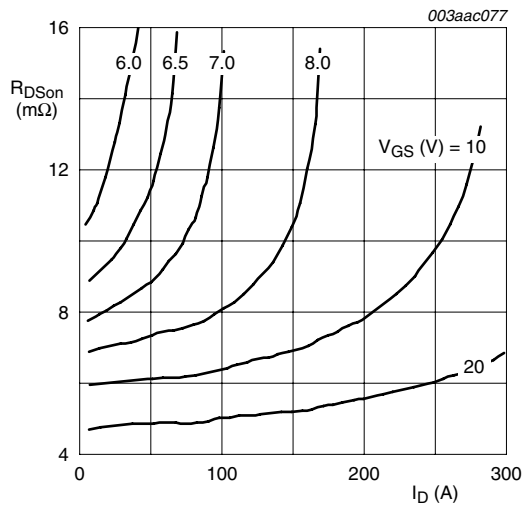
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



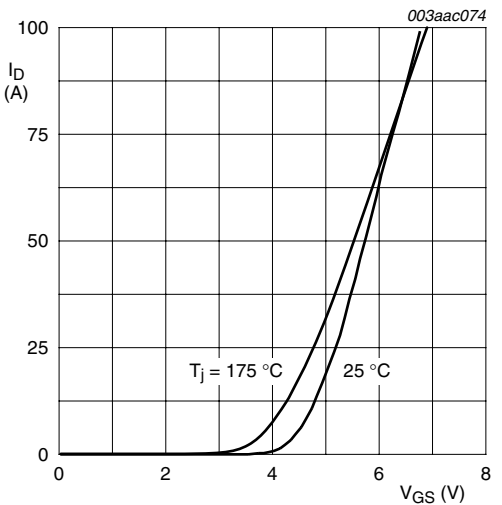
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{ V}$

Fig 6. Forward transconductance as a function of drain current; typical values



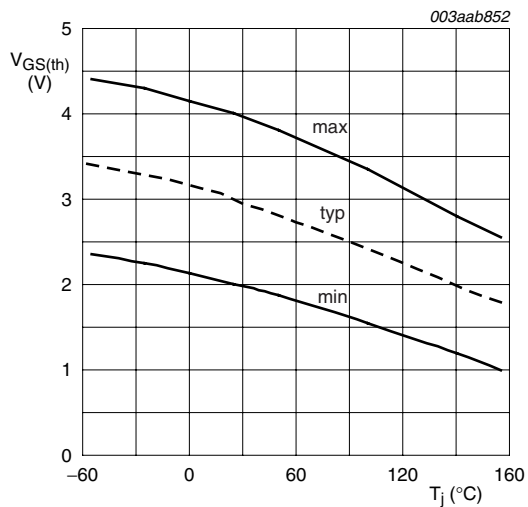
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



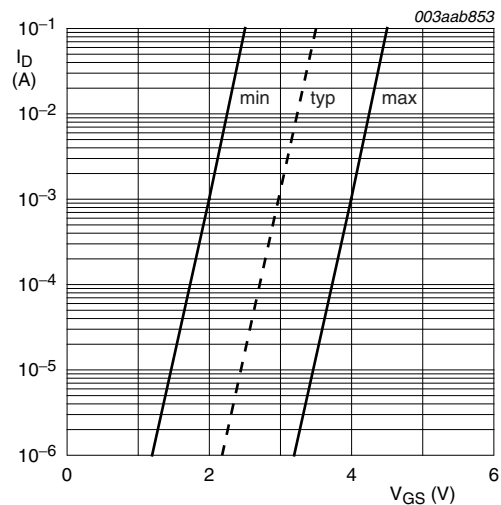
$V_{DS} = 25\text{ V}$

Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



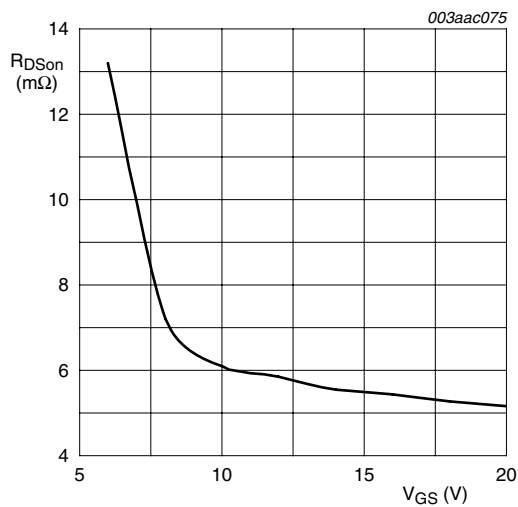
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 9. Gate-source threshold voltage as a function of junction temperature



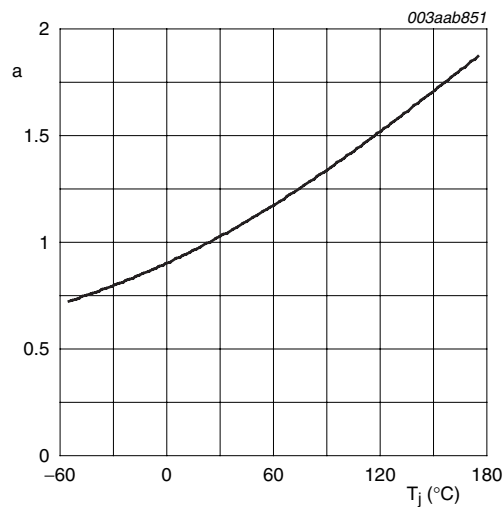
$$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$$T_j = 25^\circ\text{C}; I_D = 25 \text{ A}$$

Fig 11. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

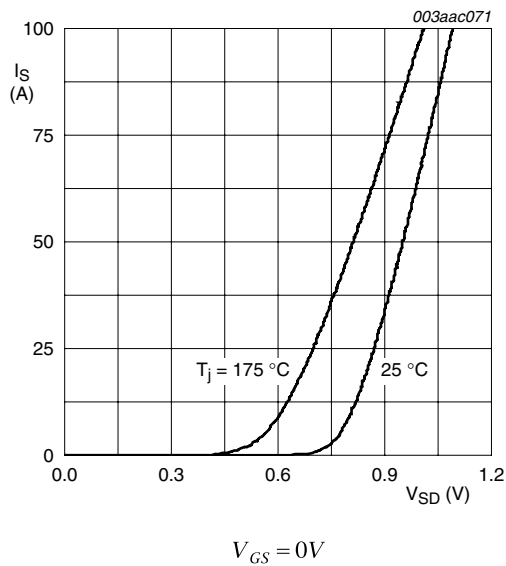


Fig 13. Reverse diode current as a function of reverse diode voltage; typical values

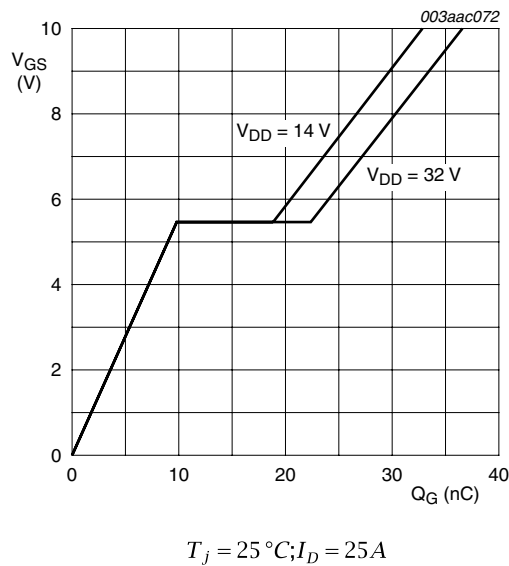


Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values

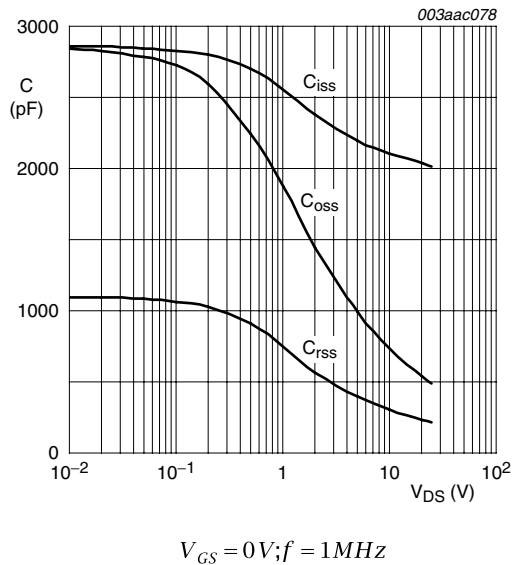


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

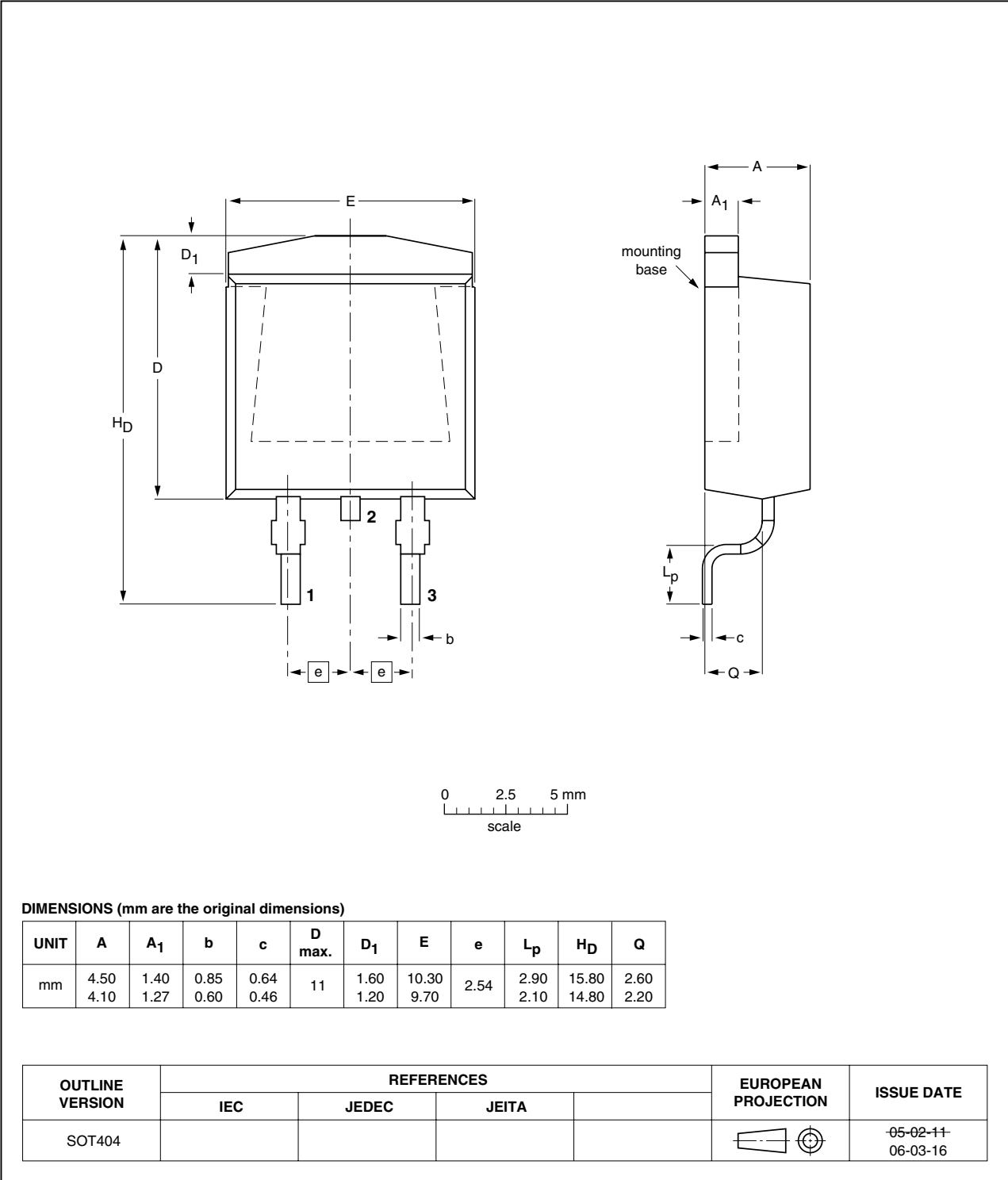


Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7608-40B_4	20080924	Product data sheet	-	BUK75_7608-40B_3
Modifications:		• Type number BUK7608-40B separated from data sheet BUK75_7608-40B_3		
BUK75_7608-40B_3	20071128	Product data sheet	-	BUK75_7608-40B_2
BUK75_7608-40B_2	20071116	Product data sheet	-	BUK75_7608_40B-01
BUK75_7608_40B-01	20030319	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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