

**Revision History****AS4C2M32D1A - 144 ball FBGA PACKAGE**

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Dec 2015

## Features

- Fast clock rate: 200 MHz
- Differential Clock CK &  $\overline{CK}$
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 512K x 32-bit for each bank
- Programmable Mode and Extended Mode registers
  - CAS Latency: 2, 2.5, 3
  - Burst length: 2, 4, 8
  - Burst Type: Sequential & Interleaved
- Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 64ms
- Precharge & active power down
- Operating Temperature:
  - Commercial (0 ~ 70 °C)
  - Industrial (-40 ~ 85 °C)
- Power supplies: V<sub>DD</sub> & V<sub>DDQ</sub> = 2.5V ± 0.2V
- Interface: SSTL\_2 I/O Interface
- 144-ball 12 x 12 x 1.4mm FBGA package
  - Pb and Halogen Free

## Overview

The 64Mb DDR SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 64 Mbits. It is internally configured as a quad 512K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK).

Data outputs occur at both rising edges of CK and  $\overline{CK}$ . Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The device provides programmable Read or Write burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, 64Mb DDR features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth; result in a device particularly well suited to high performance main memory and graphics applications.

**Table 1. Ordering Information**

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C2M32D1A-5BCN	2Mx 32	Commercial 0°C to 70°C	200	144-ball FBGA
AS4C2M32D1A-5BIN	2Mx 32	Industrial -40°C to 85°C	200	144-ball FBGA

**Figure 1. Ball Assignment (Top View)**

**Table 2. Ball Assignment by Name (FBGA 144Ball)**

Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location
A0	M4	DQ6	C1	DQ24	D12	CK	L10	VDDQ	B6	VSS	E5	VSS	J7	VSSQ	G4
A1	M5	DQ7	D1	DQ25	C12	CK	L11	VDDQ	B7	VSS	E6	VSS	J8	VSSQ	G9
A2	L5	DQ8	J12	DQ26	C11	CKE	M11	VDDQ	B9	VSS	E7	VSS	K4	VSSQ	H4
A3	M6	DQ9	J11	DQ27	B12	CS	M1	VDDQ	B11	VSS	E8	VSS	K9	VSSQ	H9
A4	M7	DQ10	H12	DQ28	A9	RAS	L1	VDDQ	D2	VSS	F5	VSSQ	A3	VSSQ	J4
A5	L8	DQ11	H11	DQ29	A8	CAS	K1	VDDQ	D11	VSS	F6	VSSQ	A10	VSSQ	J9
A6	M8	DQ12	F12	DQ30	B8	WE	K2	VDDQ	E3	VSS	F7	VSSQ	C3	NC	B3
A7	M9	DQ13	F11	DQ31	A7	VREF	M12	VDDQ	E10	VSS	F8	VSSQ	C4	NC	B10
A8/AP	M10	DQ14	E12	DQS0	A1	VDD	C6	VDDQ	F3	VSS	G5	VSSQ	C5	NC	G3
A9	L7	DQ15	E11	DQS1	G12	VDD	C7	VDDQ	F10	VSS	G6	VSSQ	C8	NC	G10
A10	K5	DQ16	E2	DQS2	G1	VDD	D3	VDDQ	H3	VSS	G7	VSSQ	C9	NC	K8
NC	L6	DQ17	E1	DQS3	A12	VDD	D10	VDDQ	H10	VSS	G8	VSSQ	C10	NC	K11
DQ0	A6	DQ18	F2	DM0	A2	VDD	K3	VDDQ	J3	VSS	H5	VSSQ	D5	NC	K12
DQ1	B5	DQ19	F1	DM1	G11	VDD	K6	VDDQ	J10	VSS	H6	VSSQ	D8	NC	L2
DQ2	A5	DQ20	H2	DM2	G2	VDD	K7	VSS	D4	VSS	H7	VSSQ	E4	NC	L3
DQ3	A4	DQ21	H1	DM3	A11	VDD	K10	VSS	D6	VSS	H8	VSSQ	E9	NC	L9
DQ4	B1	DQ22	J1	BA0	M3	VDDQ	B2	VSS	D7	VSS	J5	VSSQ	F4	NC	L12
DQ5	C2	DQ23	J2	BA1	L4	VDDQ	B4	VSS	D9	VSS	J6	VSSQ	F9	NC	M2

Figure 2. Block Diagram



**Ball Descriptions**
**Table 3. Ball Details**

Symbol	Type	Description
CK, $\overline{CK}$	Input	<b>Differential Clock:</b> CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ . Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of the crossing)
CKE	Input	<b>Clock Enable:</b> CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	<b>Bank Activate:</b> BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A10	Input	<b>Address Inputs:</b> A0-A10 are sampled during the Bank Activate command (row address A0-A10) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 512K available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set or Extended Mode Register Set command.
$\overline{CS}$	Input	<b>Chip Select:</b> $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{RAS}$	Input	<b>Row Address Strobe:</b> The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted "HIGH" the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW" the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
$\overline{CAS}$	Input	<b>Column Address Strobe:</b> The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ is held "HIGH" and $\overline{CS}$ is asserted "LOW" the column access is started by asserting $\overline{CAS}$ "LOW". Then, the Read or Write command is selected by asserting $\overline{WE}$ "HIGH" or "LOW".
$\overline{WE}$	Input	<b>Write Enable:</b> The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command.
DQS0-DQS3	Input / Output	<b>Bidirectional Data Strobe:</b> The DQSx signals are mapped to the following data bytes: DQS0 to DQ0-DQ7, DQS1 to DQ8-DQ15, DQS2 to DQ16-DQ23, DQS3 to DQ24-DQ31.
DM0 - DM3	Input	<b>Data Input Mask:</b> DM0-DM3 are byte specific. Input data is masked when DM is sampled HIGH during a write cycle. DM3 masks DQ31-DQ24, DM2 masks DQ23-DQ16, DM1 masks DQ15-DQ8, and DM0 masks DQ7-DQ0.
DQ0 - DQ31	Input / Output	<b>Data I/O:</b> The DQ0-DQ31 input and output data are synchronized with positive and negative edges of DQS0~DQS3. The I/Os are byte-maskable during Writes.
V <sub>DD</sub>	Supply	<b>Power Supply:</b> 2.5V ± 0.2V.
V <sub>SS</sub>	Supply	<b>Ground</b>
V <sub>DDQ</sub>	Supply	<b>DQ Power:</b> 2.5V ± 0.2V . Provide isolated power to DQs for improved noise immunity.

V <sub>SSQ</sub>	Supply	<b>DQ Ground:</b> Provide isolated ground to DQs for improved noise immunity.
V <sub>REF</sub>	Supply	<b>Reference Voltage for Inputs:</b> +0.5*V <sub>DDQ</sub>
NC	-	<b>No Connect:</b> These pins should be left unconnected.

## Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 3 shows the truth table for the operation commands.

**Table 4. Truth Table (Note (1), (2))**

Command	State	CKEn-1	CKEn	DM	BA1	BA0	A10	A9-0	CS	RAS	CAS	WE
BankActivate	Idle <sup>(3)</sup>	H	X	X	V	V	Row Address		L	L	H	H
BankPrecharge	Any	H	X	X	V	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	X	H	X	L	L	H	L
Write	Active <sup>(3)</sup>	H	X	V	V	V	L	Column Address A0~A7	L	H	L	L
Write and AutoPrecharge	Active <sup>(3)</sup>	H	X	V	V	V	H		L	H	L	L
Read	Active <sup>(3)</sup>	H	X	X	V	V	L		L	H	L	H
Read and Autoprecharge	Active <sup>(3)</sup>	H	X	X	V	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	L	L	OP code		L	L	L	L
Extended Mode Register Set	Idle	H	X	X	L	H			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	X	H	X	X	X
Burst Stop	Active <sup>(4)</sup>	H	X	X	X	X	X	X	L	H	H	L
AutoRefresh	Idle	H	H	X	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Entry	Idle/Active <sup>(5)</sup>	H	L	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Data Mask Enable	Active	H	X	H	X	X	X	X	X	X	X	X
Data Mask Disable	Active	H	X	L	X	X	X	X	X	X	X	X

- Note:** 1. V=Valid data, X=Don't Care, L=Low level, H=High level  
 2. CKEn signal is input level when commands are provided.  
 CKEn-1 signal is input level one clock cycle before the commands are provided.  
 3. These are states of bank designated by BA signal.  
 4. Device state is 2, 4, and 8 burst operation.  
 5. Power Down Mode can not enter in the burst operation.

### Mode Register Set (MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs CAS Latency, Burst Type, and Burst Length to make the DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed. The Mode Register is written by asserting Low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A10 and BA0, BA1 in the same cycle in which  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$  and  $\overline{WE}$  are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and CAS latencies.

**Table 5. Mode Register Bitmap**



\* Note: RFU (Reserved for future use) must be set to "0" during MRS cycle.

- Burst Length Field (A2~A0)**

This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8.

**Table 6. Burst Length**

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



- Addressing Mode Select Field (A3)

The Addressing Mode can be one of two modes, either Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4 and 8.

**Table 7. Addressing Mode**

A3	Addressing Mode
0	Sequential
1	Interleave

- Burst Definition, Addressing Sequence of Sequential and Interleave Mode

**Table 8. Burst Address ordering**

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

- CAS Latency Field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field.  $t_{CAC}(\min) \leq \text{CAS Latency} \times t_{CK}$

**Table 9. CAS Latency**

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved

- Test Mode field (A8~A7)

These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

**Table 10. Test Mode**

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset

- (BA0, BA1)

**Table 11. MRS/EMRS**

BA1	BA0	A10 ~ A0
0	0	MRS Cycle
0	1	Extended Functions (EMRS)

### Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The Extended Mode Register is written by asserting Low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of A0 ~ A10 and BA1 are written in the mode register in the same cycle as  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 is used for setting driver strength. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

**Table 12. Extended Mode Register Bitmap**


**Table 13. Absolute Maximum Rating**

Symbol	Item	Values	Unit	
V <sub>I/O</sub>	Voltage on I/O Pins Relative to V <sub>SS</sub>	- 0.5 ~ V <sub>DDQ</sub> + 0.5	V	
V <sub>DD</sub> , V <sub>DDQ</sub>	Voltage on V <sub>DD</sub> , V <sub>DDQ</sub> Supply Relative to V <sub>SS</sub>	- 1 ~ 3.6	V	
V <sub>IN</sub>	Voltage on Inputs Relative to V <sub>SS</sub>	- 1 ~ 3.6	V	
T <sub>A</sub>	Ambient Temperature	Commercial	0 ~ 70	°C
		Industrial	- 40 ~ 85	°C
T <sub>STG</sub>	Storage Temperature	- 55 ~ 150	°C	
P <sub>D</sub>	Power Dissipation	1	W	
I <sub>OS</sub>	Short Circuit Output Current	50	mA	

**Note:** Absolute maximum DC requirements contain stress ratings only. Functional operation at the absolute maximum limits is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability.

**Table 14. Recommended D.C. Operating Conditions (V<sub>DD</sub> = 2.5V ± 0.2V, T<sub>A</sub> = -40~85 °C)**

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage	2.3	2.7	V
V <sub>DDQ</sub>	Power Supply Voltage (for I/O Buffer)	2.3	2.7	V
V <sub>REF</sub>	Input Reference Voltage	0.49*V <sub>DDQ</sub>	0.51* V <sub>DDQ</sub>	V
V <sub>IH</sub> (DC)	Input High Voltage (DC)	V <sub>REF</sub> + 0.15	V <sub>DDQ</sub> + 0.3	V
V <sub>IL</sub> (DC)	Input Low Voltage (DC)	-0.3	V <sub>REF</sub> - 0.15	V
V <sub>TT</sub>	Termination Voltage	V <sub>REF</sub> - 0.04	V <sub>REF</sub> + 0.04	V
V <sub>IN</sub> (DC)	Input Voltage Level, CK and $\overline{CK}$ inputs	-0.3	V <sub>DDQ</sub> + 0.3	V
V <sub>ID</sub> (DC)	Input Different Voltage, CK and $\overline{CK}$ inputs	0.36	V <sub>DDQ</sub> + 0.6	V
I <sub>I</sub>	Input leakage current	-2	2	μA
I <sub>OZ</sub>	Output leakage current	-5	5	μA
I <sub>OH</sub>	Output High Current (V <sub>OH</sub> = 1.95V)	-16.2	-	mA
I <sub>OL</sub>	Output Low Current (V <sub>OL</sub> = 0.35V)	16.2	-	mA

**Note:** All voltages are referenced to V<sub>SS</sub>.

**Table 15. Capacitance (V<sub>DD</sub> = 2.5V, f = 1MHz, T<sub>A</sub> = 25 °C)**

Symbol	Parameter	Min.	Max.	Delta	Unit
C <sub>IN1</sub>	Input Capacitance (CK, $\overline{CK}$ )	1.5	2.5	0.25	pF
C <sub>IN2</sub>	Input Capacitance (All other input-only pins)	1.5	2.5	0.5	pF
C <sub>I/O</sub>	DQ, DQS, DM Input/Output Capacitance	3.5	4.5	0.5	pF

**Note:** These parameters are guaranteed by design, periodically sampled and are not 100% tested

**Table 16. D.C. Characteristics ( $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40 \sim 85 \text{ }^\circ\text{C}$ )**

Parameter & Test Condition	Symbol	-5	Unit	Note
		Max.		
<b>OPERATING CURRENT:</b> One bank; Active-Precharge; $t_{RC}=t_{RC}(\text{min})$ ; $t_{CK}=t_{CK}(\text{min})$ ; DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	120	mA	
<b>OPERATING CURRENT :</b> One bank; Active-Read-Precharge; BL=4; $t_{RC}=t_{RC}(\text{min})$ ; $t_{CK}=t_{CK}(\text{min})$ ; $I_{out}=0\text{mA}$ ; Address and control inputs changing once per clock cycle	IDD1	140	mA	
<b>PRECHARGE POWER-DOWN STANDBY CURRENT:</b> All banks idle; power-down mode; $t_{CK}=t_{CK}(\text{min})$ ; CKE=LOW	IDD2P	15	mA	
<b>IDLE STANDBY CURRENT :</b> CKE = HIGH; $\overline{CS}=\text{HIGH}(\text{DESELECT})$ ; All banks idle; $t_{CK}=t_{CK}(\text{min})$ ; Address and control inputs changing once per clock cycle; $V_{IN}=V_{REF}$ for DQ, DQS and DM	IDD2N	40	mA	
<b>ACTIVE POWER-DOWN STANDBY CURRENT :</b> one bank active; power-down mode; CKE=LOW; $t_{CK}=t_{CK}(\text{min})$	IDD3P	40	mA	
<b>ACTIVE STANDBY CURRENT :</b> $\overline{CS}=\text{HIGH}$ ;CKE=HIGH; one bank active ; $t_{RC}=t_{RC}(\text{max})$ ; $t_{CK}=t_{CK}(\text{min})$ ;Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	50	mA	
<b>OPERATING CURRENT BURST READ :</b> BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; $t_{CK}=t_{CK}(\text{min})$ ; $I_{out}=0\text{mA}$ ;50% of data changing on every transfer	IDD4R	150	mA	
<b>OPERATING CURRENT BURST Write :</b> BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; $t_{CK}=t_{CK}(\text{min})$ ; DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	150	mA	
<b>AUTO REFRESH CURRENT :</b> $t_{RC}=t_{RFC}(\text{min})$ ; $t_{CK}=t_{CK}(\text{min})$	IDD5	150	mA	
<b>SELF REFRESH CURRENT:</b> Self Refresh Mode ; CKE $\leq 0.2V$ ; $t_{CK}=t_{CK}(\text{min})$	IDD6	3	mA	1
<b>BURST OPERATING CURRENT 4 bank operation:</b> Four bank interleaving READs; BL=4;with Auto Precharge; $t_{RC}=t_{RC}(\text{min})$ ; $t_{CK}=t_{CK}(\text{min})$ ; Address and control inputs change only during Active, READ , or WRITE command	IDD7	240	mA	

**Table 17. Electrical Characteristics and Recommended A.C. Operating Condition**
 $(V_{DD} = 2.5V \pm 0.2V, T_A = -40 \sim 85 \text{ } ^\circ\text{C})$ 

Symbol	Parameter		-5		Unit	Note
			Min.	Max.		
t <sub>CK</sub>	Clock cycle time	CL = 2	7.5	12	ns	
		CL = 2.5	6	12	ns	
		CL = 3	5	7.5	ns	
t <sub>CH</sub>	Clock high level width		0.45	0.55	t <sub>CK</sub>	
t <sub>CL</sub>	Clock low level width		0.45	0.55	t <sub>CK</sub>	
t <sub>HP</sub>	Clock half period		t <sub>CLMIN</sub> or t <sub>CHMIN</sub>	-	ns	2
t <sub>HZ</sub>	Data-out-high impedance time from CK, $\overline{CK}$		-	0.7	ns	3
t <sub>LZ</sub>	Data-out-low impedance time from CK, $\overline{CK}$		-0.7	0.7	ns	3
t <sub>DQ<sub>SCK</sub></sub>	DQS-out access time from CK, $\overline{CK}$		-0.6	0.6	ns	
t <sub>AC</sub>	Output access time from CK, $\overline{CK}$		-0.7	0.7	ns	
t <sub>DQ<sub>SQ</sub></sub>	DQS-DQ Skew		-	0.4	ns	
t <sub>RP<sub>RE</sub></sub>	Read preamble		0.9	1.1	t <sub>CK</sub>	
t <sub>RP<sub>ST</sub></sub>	Read postamble		0.4	0.6	t <sub>CK</sub>	
t <sub>DQ<sub>SS</sub></sub>	CK to valid DQS-in		0.72	1.25	t <sub>CK</sub>	
t <sub>WP<sub>PRES</sub></sub>	DQS-in setup time		0	-	ns	4
t <sub>WP<sub>RE</sub></sub>	DQS Write preamble		0.25	-	t <sub>CK</sub>	
t <sub>WP<sub>ST</sub></sub>	DQS write postamble		0.4	0.6	t <sub>CK</sub>	5
t <sub>DQ<sub>SH</sub></sub>	DQS in high level pulse width		0.35	-	t <sub>CK</sub>	
t <sub>DQ<sub>SL</sub></sub>	DQS in low level pulse width		0.35	-	t <sub>CK</sub>	
t <sub>IS</sub>	Address and Control input setup time		0.7	-	ns	6
t <sub>IH</sub>	Address and Control input hold time		0.7	-	ns	6
t <sub>DS</sub>	DQ & DM setup time to DQS		0.4	-	ns	
t <sub>DH</sub>	DQ & DM hold time to DQS		0.4	-	ns	
t <sub>QH</sub>	DQ/DQS output hold time from DQS		t <sub>HP</sub> - t <sub>QHS</sub>	-	ns	
t <sub>RC</sub>	Row cycle time		55	-	ns	
t <sub>RFC</sub>	Refresh row cycle time		70	-	ns	
t <sub>RAS</sub>	Row active time		40	70K	ns	
t <sub>RCD</sub>	Active to Read or Write delay		15	-	ns	
t <sub>RP</sub>	Row precharge time		15	-	ns	
t <sub>RRD</sub>	Row active to Row active delay		10	-	ns	
t <sub>WR</sub>	Write recovery time		15	-	ns	
t <sub>WTR</sub>	Internal Write to Read Command Delay		10	-	ns	
t <sub>MRD</sub>	Mode register set cycle time		10	-	ns	
t <sub>REFI</sub>	Average Periodic Refresh interval		-	15.6	μs	7
t <sub>XSRD</sub>	Self refresh exit to read command delay		200	-	t <sub>CK</sub>	
t <sub>XSNR</sub>	Self refresh exit to non-read command delay		75	-	ns	
t <sub>DAL</sub>	Auto Precharge write recovery + precharge time		t <sub>WR</sub> +t <sub>RP</sub>	-	ns	
t <sub>DIPW</sub>	DQ and DM input puls width		1.75	-	ns	
t <sub>IPW</sub>	Control and Address input pulse width		2.2	-	ns	
t <sub>QHS</sub>	Data Hold Skew Factor		-	0.5	ns	
t <sub>DSS</sub>	DQS falling edge to CK setup time		0.2	-		
t <sub>D<sub>SH</sub></sub>	DQS falling edge hold time from CK		0.2	-		

**Table 18. Recommended A.C. Operating Conditions** ( $V_{DD} = 2.5V \pm 0.2V$ ,  $T_A = -40\sim 85\text{ }^\circ\text{C}$ )

Symbol	Parameter	Min.	Max.	Unit
$V_{IH}$ (AC)	Input High Voltage (AC)	$V_{REF} + 0.31$	-	V
$V_{IL}$ (AC)	Input Low Voltage (AC)	-	$V_{REF} - 0.31$	V
$V_{ID}$ (AC)	Input Different Voltage, CK and $\overline{CK}$ inputs	0.7	$V_{DDQ} + 0.6$	V
$V_{IX}$ (AC)	Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$0.5 * V_{DDQ} - 0.2$	$0.5 * V_{DDQ} + 0.2$	V

**Note:**

- 1) Enables on-chip refresh and address counters.
- 2)  $\text{Min}(t_{CL}, t_{CH})$  refers to the smaller of the actual clock low time and actual clock high time as provided to the device.
- 3)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
- 4) The specific requirement is that DQS be valid (High, Low, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on  $t_{DQSS}$ .
- 5) The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- 6) For command/address and CK &  $\overline{CK}$  slew rate  $\geq 1.0V/ns$ .
- 7) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
- 8) Power-up sequence is described in Note 11
- 9) A.C. Test Conditions

**Table 19. SSTL \_2 Interface**

Reference Level of Output Signals ( $V_{REF}$ )	$0.5 * V_{DDQ}$
Output Load	Reference to the Test Load
Input Signal Levels	$V_{REF} + 0.31\text{ V} / V_{REF} - 0.31\text{ V}$
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	$0.5 * V_{DDQ}$

10) Figure 2 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment is suggested.

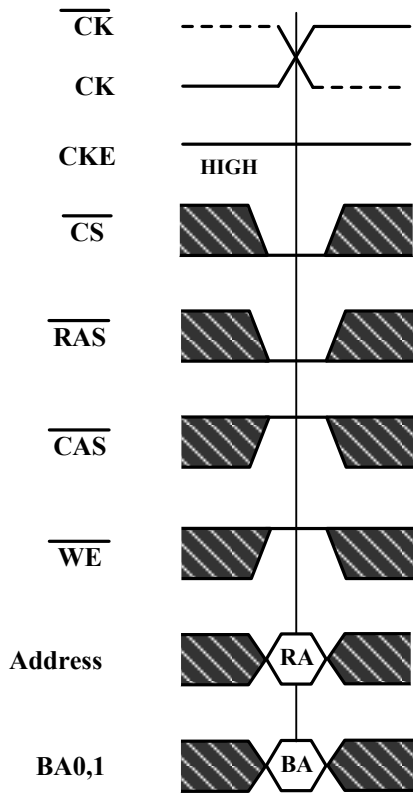
**Figure 3. SSTL\_2 A.C. Test Load**



#### 11) Power up Sequence

Power up must be performed in the following sequence.

- 1) Apply power to  $V_{DD}$  before or at the same time as  $V_{DDQ}$ ,  $V_{TT}$  and  $V_{REF}$  when all input signals are held "NOP" state and maintain CKE "LOW".
- 2) Start clock and maintain stable condition for minimum 200 $\mu$ s.
- 3) Issue a "NOP" command and keep CKE "HIGH"
- 4) Issue a "Precharge All" command.
- 5) Issue EMRS – enable DLL.
- 6) Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
- 7) Precharge all banks of the device.
- 8) Issue two or more Auto Refresh commands.
- 9) Issue MRS – with A8 to low to initialize the mode register.

**Timing Waveforms**
**Figure 4. Activating a Specific Row in a Specific Bank**


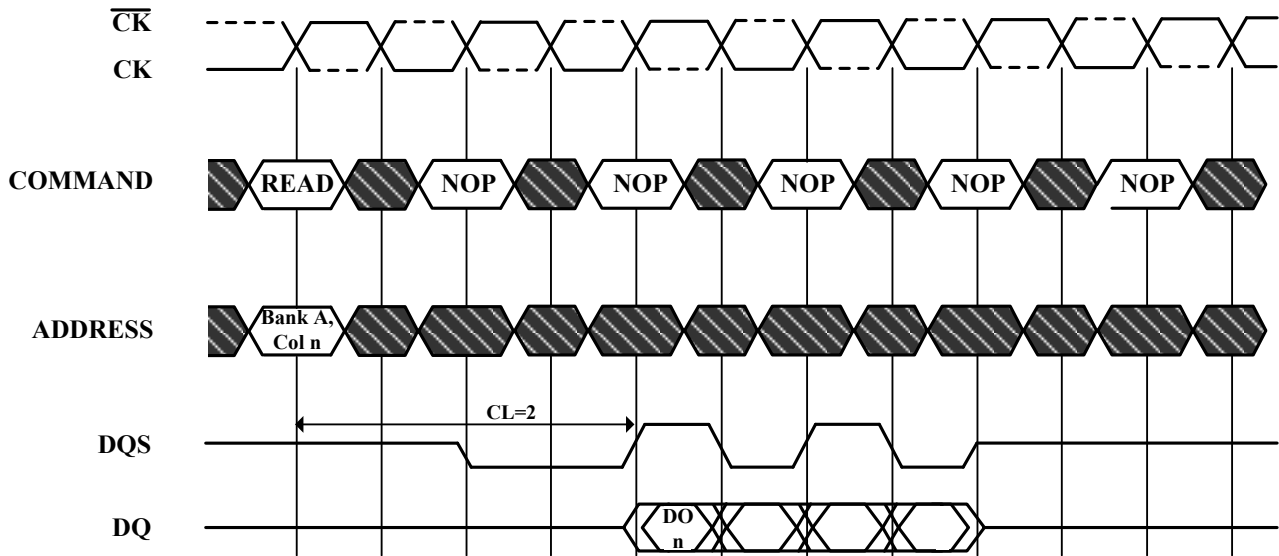
RA=Row Address  
 BA=Bank Address

 Don't Care



**Figure 5. tRCD and tRRD Definition**

**Figure 6. READ Command**

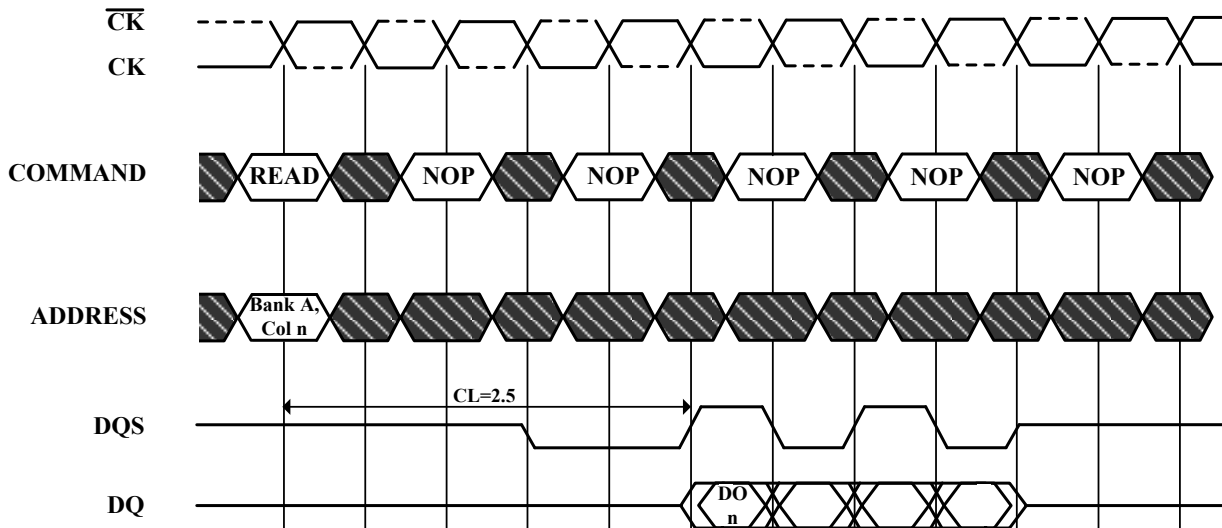

**Figure 7. Read Burst Required CAS Latencies (CL=2)**


DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

**Read Burst Required CAS Latencies (CL=2.5)**


DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

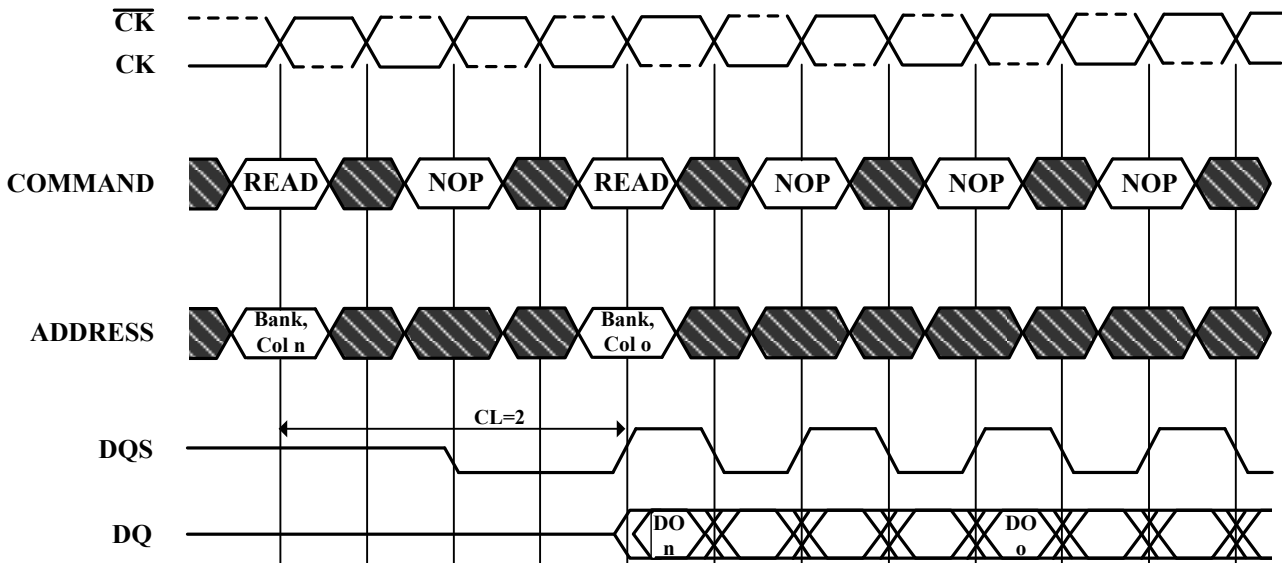
**Read Burst Required CAS Latencies (CL=3)**


DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

**Figure 8. Consecutive Read Bursts Required CAS Latencies (CL=2)**


DO n (or o)=Data Out from column n (or column o)

Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o

Read commands shown must be to the same device

 Don't Care

**Consecutive Read Bursts Required CAS Latencies (CL=2.5)**


**DO n (or o)=Data Out from column n (or column o)**

**Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)**

**3 subsequent elements of Data Out appear in the programmed order following DO n**

**3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o**

**Read commands shown must be to the same device**

 **Don't Care**

**Consecutive Read Bursts Required CAS Latencies (CL=3)**


DO n (or o)=Data Out from column n (or column o)

Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)

3 subsequent elements of Data Out appear in the programmed order following DO n

3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o

Read commands shown must be to the same device

 Don't Care

**Figure 9. Non-Consecutive Read Bursts Required CAS Latencies (CL=2)**


DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

 Don't Care

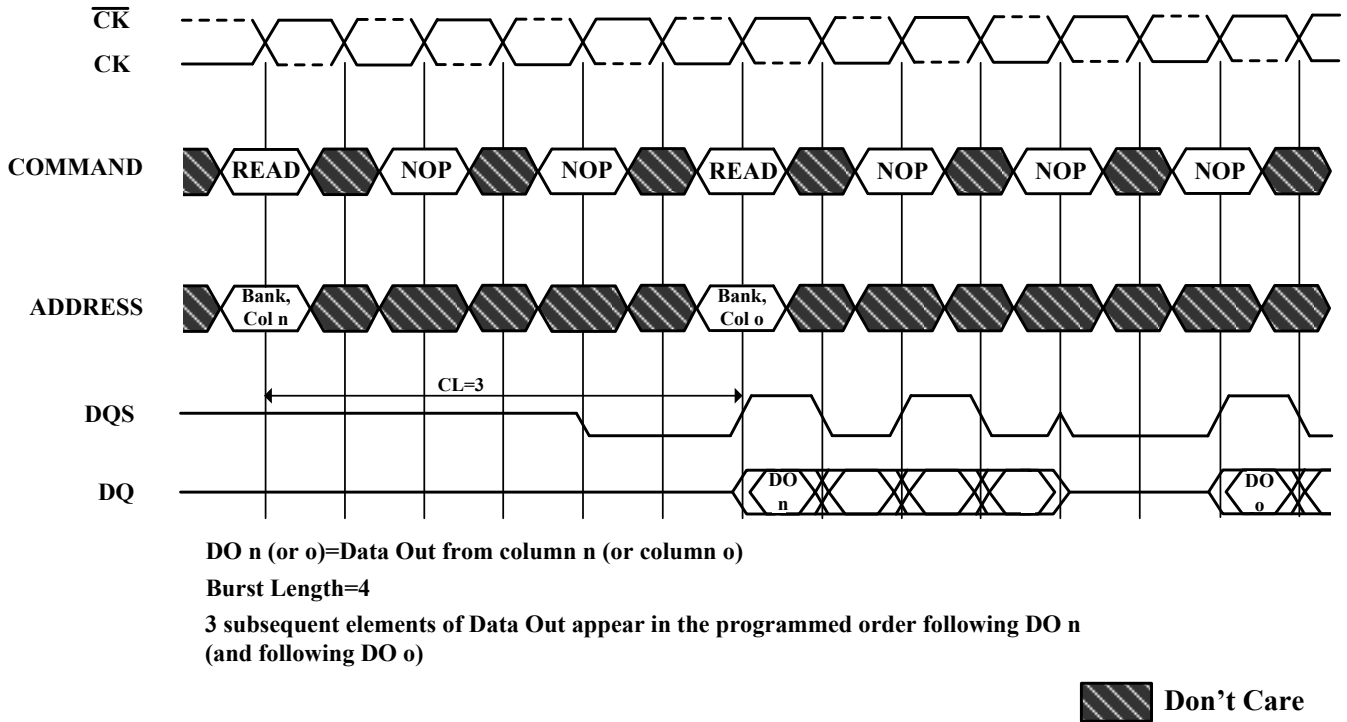
**Non-Consecutive Read Bursts Required CAS Latencies (CL=2.5)**


DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

 Don't Care

**Non-Consecutive Read Bursts Required CAS Latencies (CL=3)**


DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

 Don't Care



**Figure 10. Random Read Accesses Required CAS Latencies (CL=2)**


DO n, etc. =Data Out from column n, etc.

n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

 Don't Care

**Random Read Accesses Required CAS Latencies (CL=2.5)**


DO n, etc. =Data Out from column n, etc.

n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

 Don't Care

**Random Read Accesses Required CAS Latencies (CL=3)**

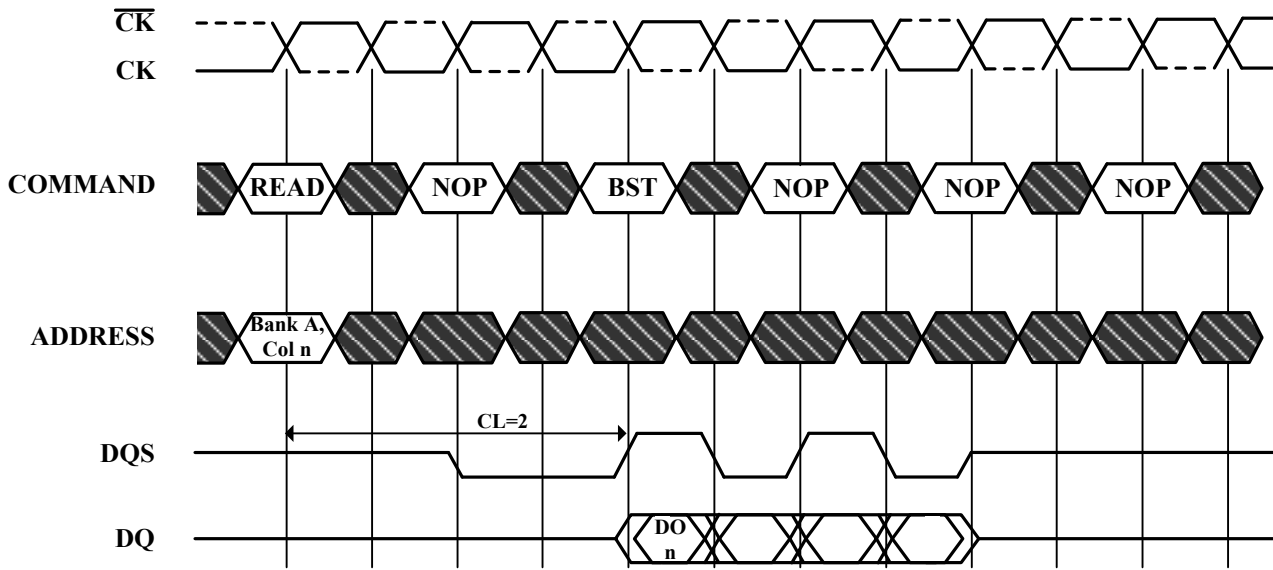

DO n, etc. =Data Out from column n, etc.

n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

 Don't Care

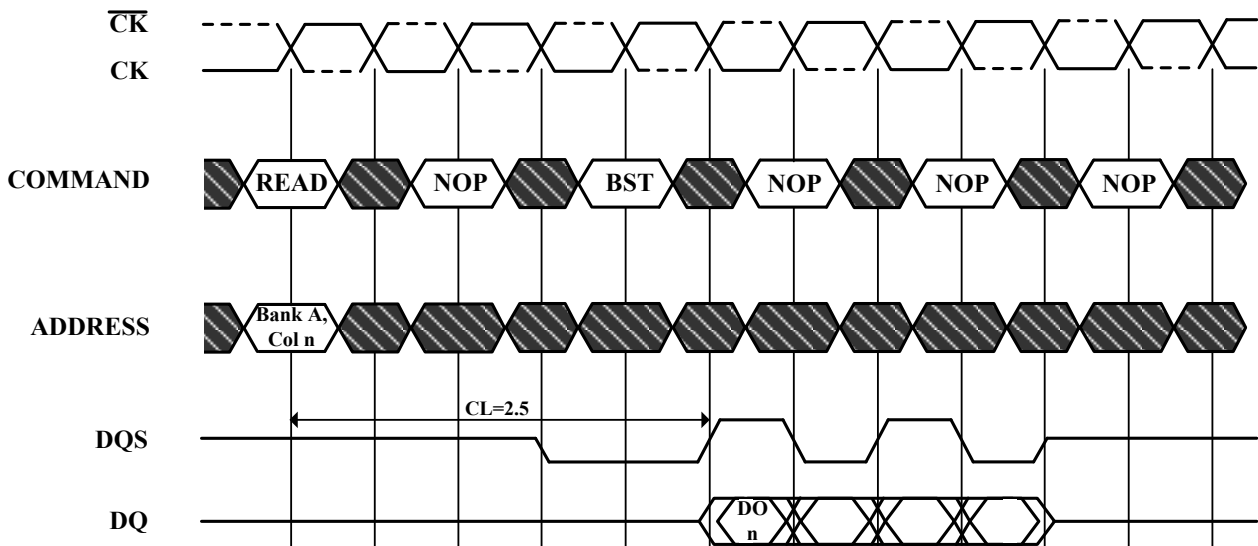
**Figure 11. Terminating a Read Burst Required CAS Latencies (CL=2)**


DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

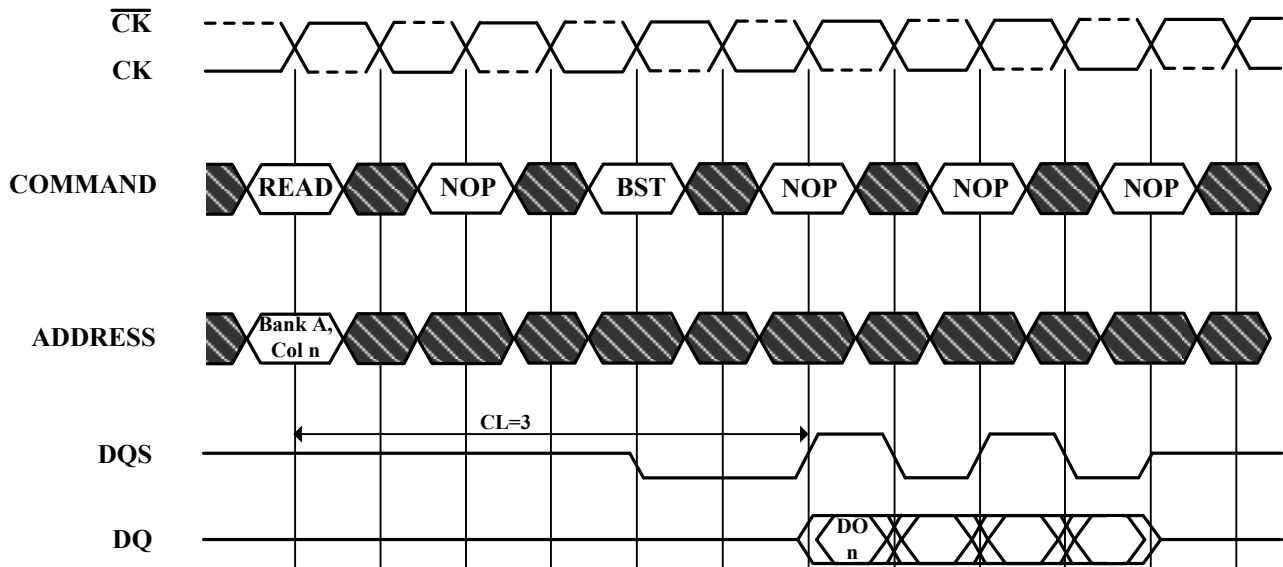
**Terminating a Read Burst Required CAS Latencies (CL=2.5)**


DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

**Terminating a Read Burst Required CAS Latencies (CL=3)**


DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

 Don't Care

**Figure 12. Read to Write Required CAS Latencies (CL=2)**

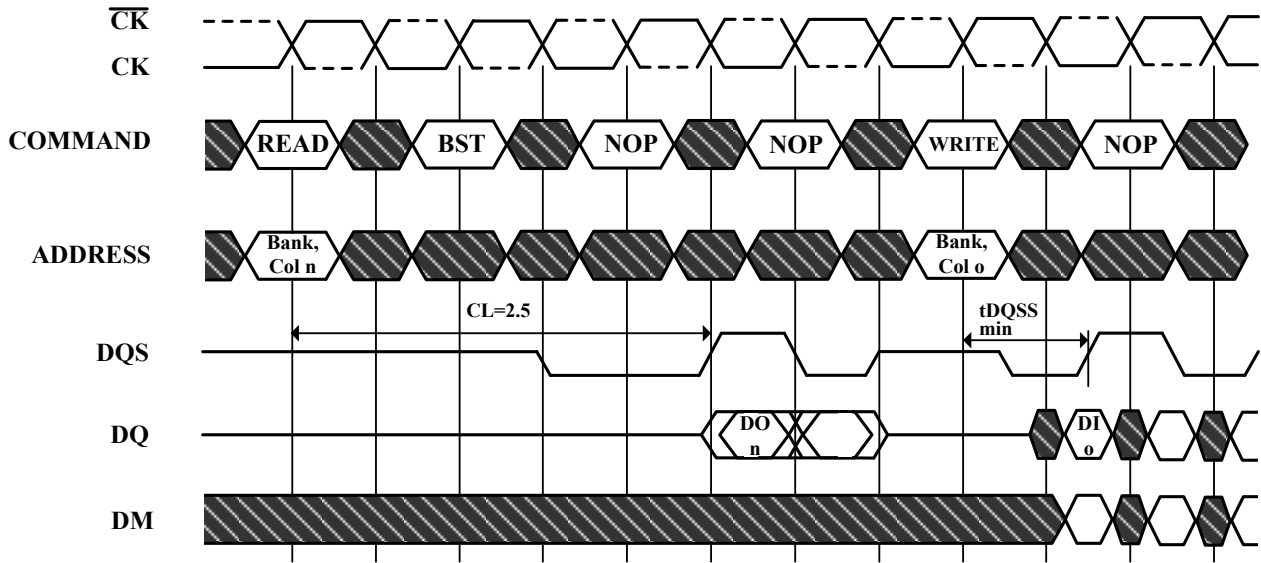

DO n (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

 Don't Care

**Read to Write Required CAS Latencies (CL=2.5)**


DO<sub>n</sub> (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO<sub>n</sub>

Data in elements are applied following DI<sub>o</sub> in the programmed order

 Don't Care

**Read to Write Required CAS Latencies (CL=3)**

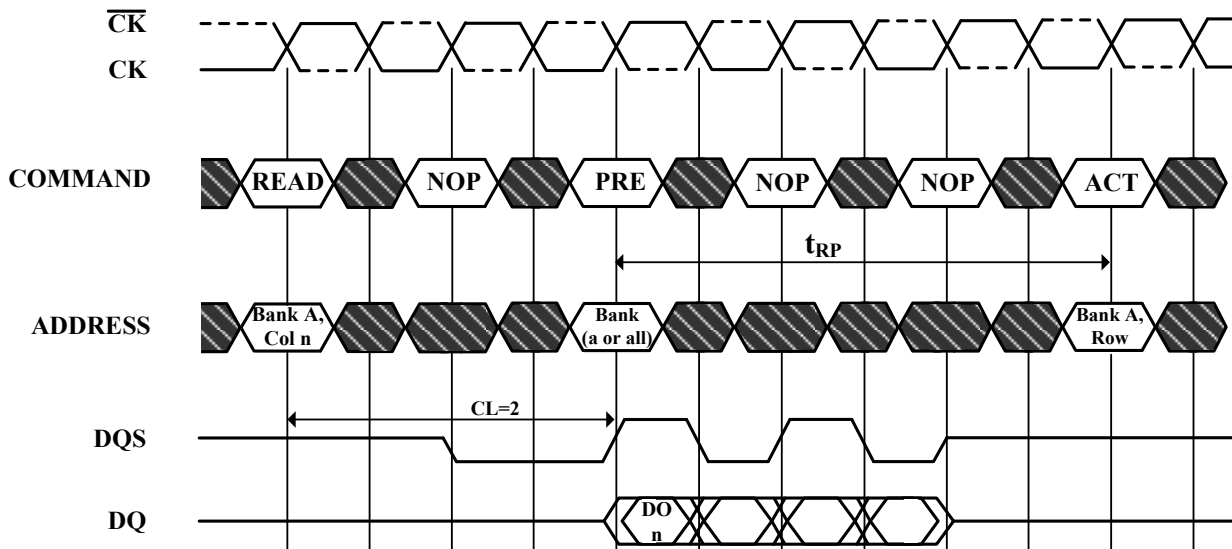

DO n (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

 Don't Care

**Figure 13. Read to Precharge Required CAS Latencies (CL=2)**


DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8  
3 subsequent elements of Data Out appear in the programmed order  
following DO n

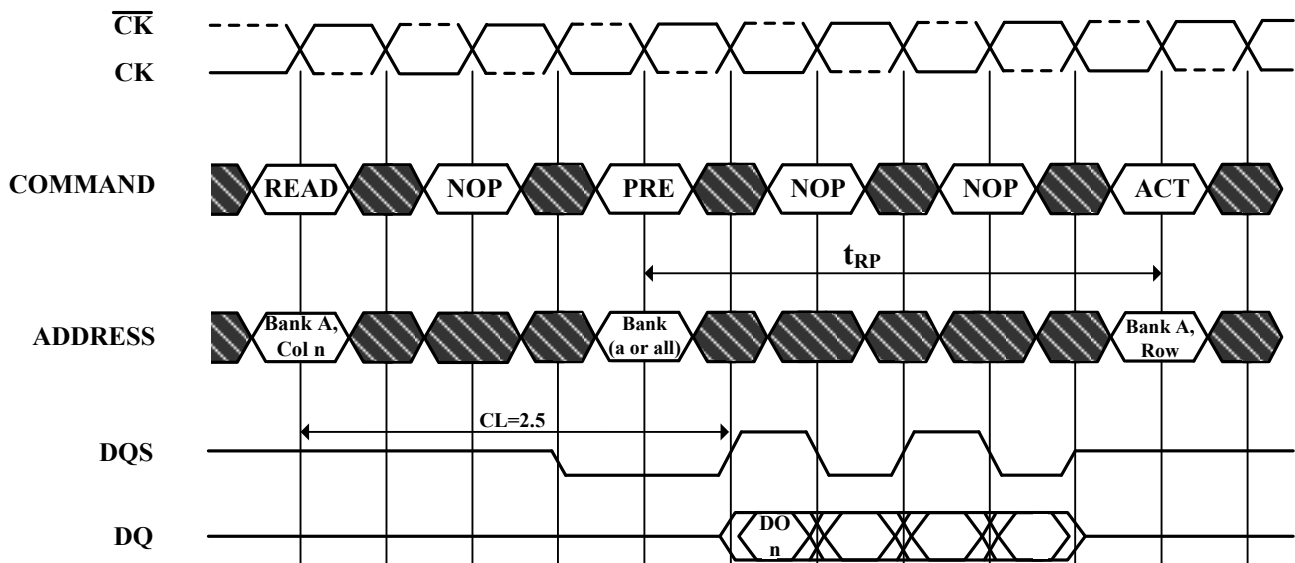
Precharge may be applied at  $(BL/2)$  tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE  
command for applicable banks

The Active command may be applied if tRC has been met

 Don't Care



**Read to Precharge Required CAS Latencies (CL=2.5)**


**DO n = Data Out from column n**

**Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8  
3 subsequent elements of Data Out appear in the programmed order  
following DO n**

**Precharge may be applied at (BL/2) tCK after the READ command**

**Note that Precharge may not be issued before tRAS ns after the ACTIVE  
command for applicable banks**

**The Active command may be applied if tRC has been met**

 **Don't Care**

**Read to Precharge Required CAS Latencies (CL=3)**


DO n = Data Out from column n

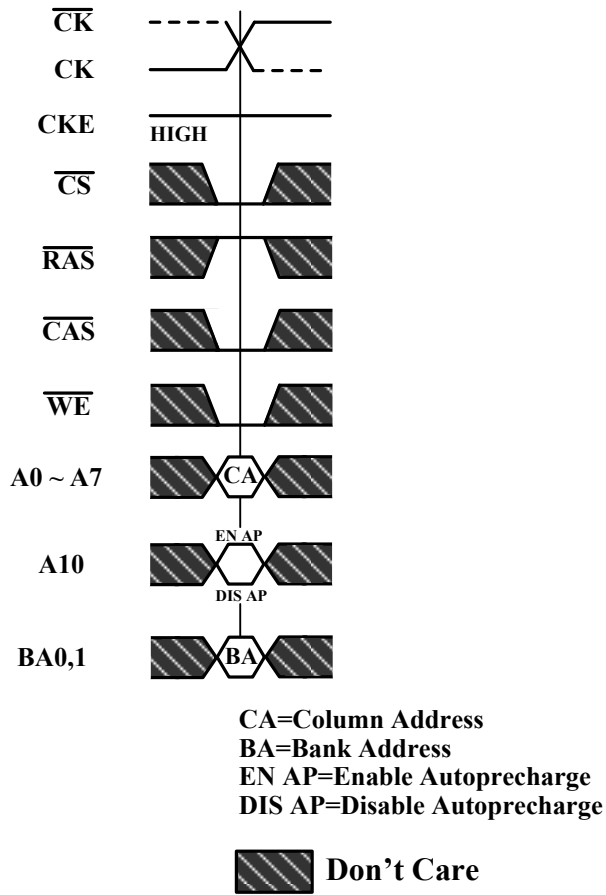
Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8  
 3 subsequent elements of Data Out appear in the programmed order  
 following DO n

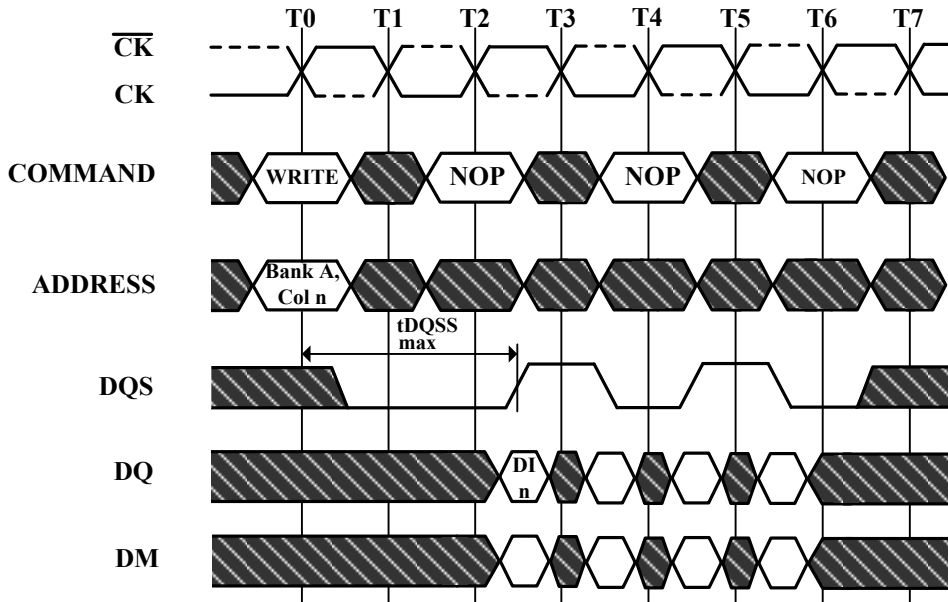
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE  
 command for applicable banks

The Active command may be applied if tRC has been met

 Don't Care

**Figure 14. Write Command**


**Figure 15. Write Max DQSS**


DI n = Data In for column n

3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

 Don't Care

**Figure 16. Write Min DQSS**

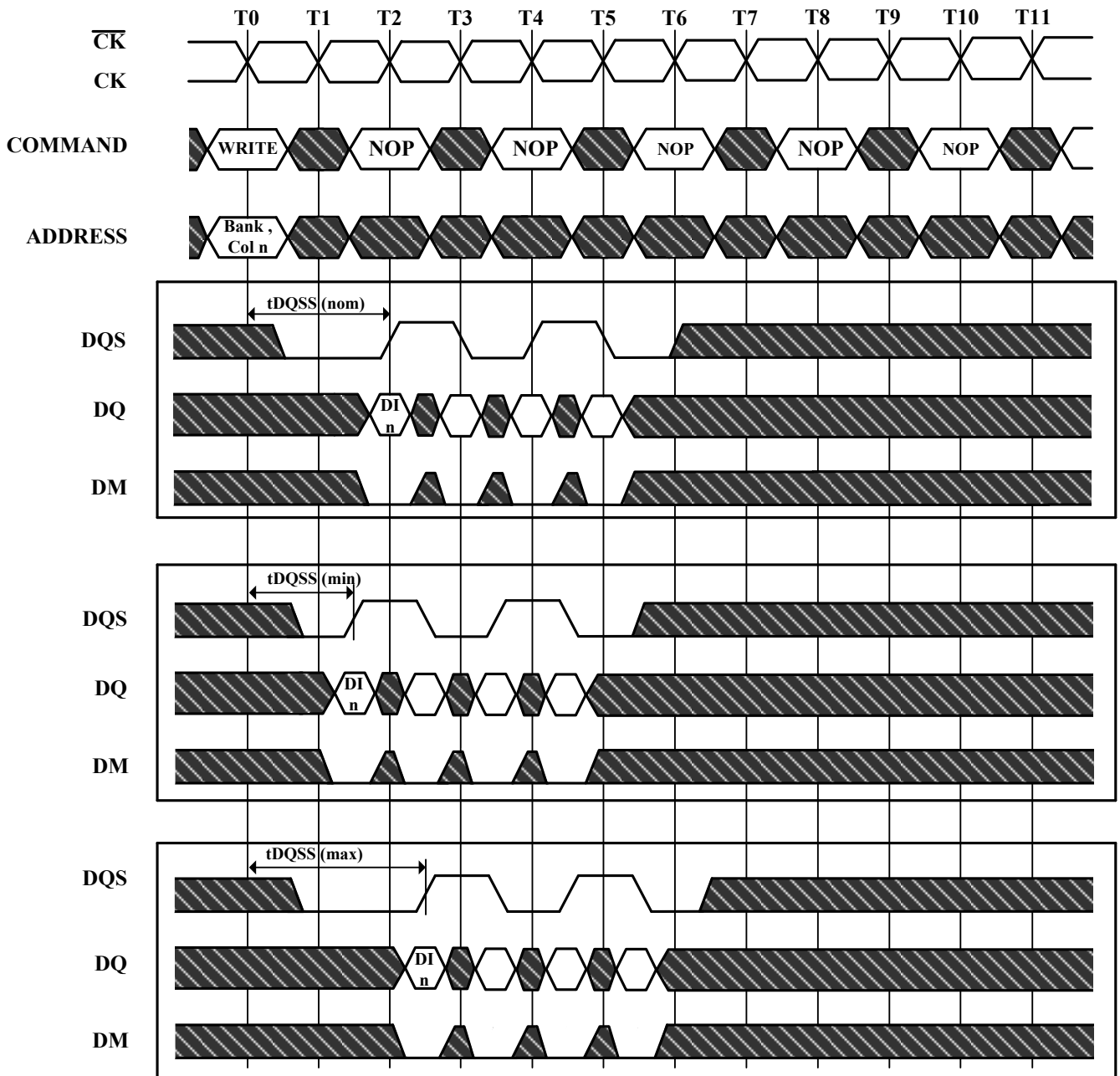

DI n = Data In for column n

3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

 Don't Care

**Figure 17. Write Burst Nom, Min, and Max tDQSS**


DI n = Data In for column n

3 subsequent elements of Data are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

DM=DM0 ~ DM3

 Don't Care

**Figure 18. Write to Write Max tDQSS**


DI n , etc. = Data In for column n,etc.

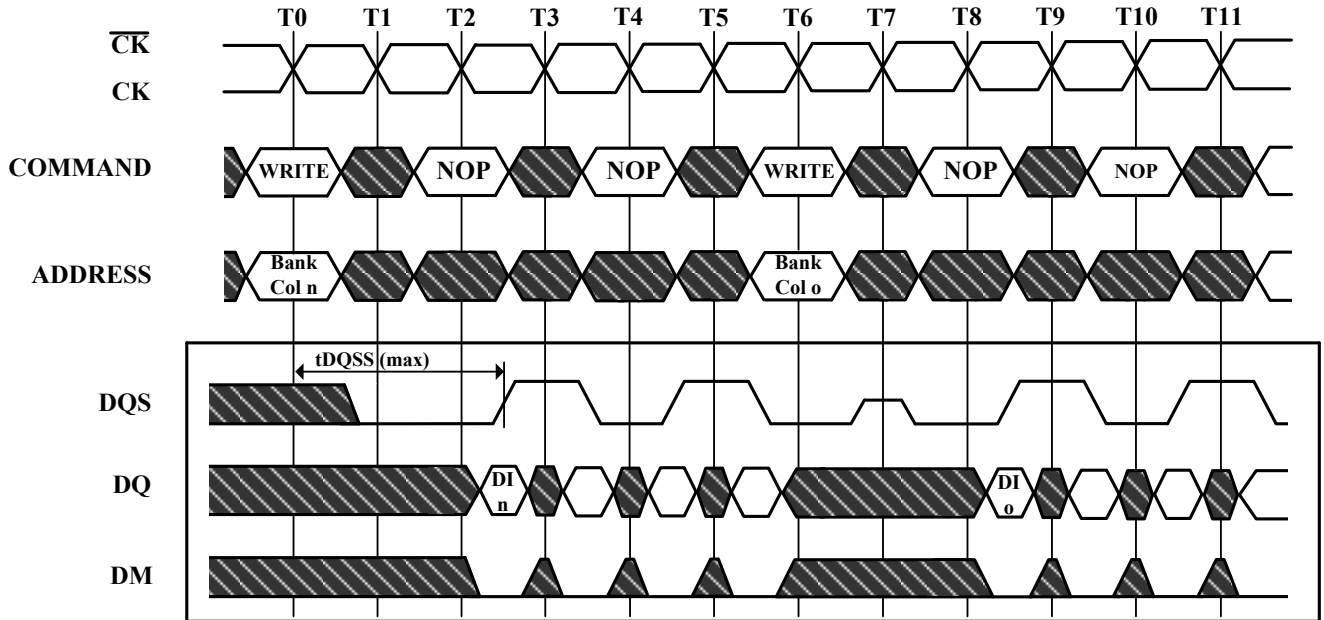
3 subsequent elements of Data In are applied in the programmed order following DI n

3 subsequent elements of Data In are applied in the programmed order following DI o

Non-interrupted bursts of 4 are shown

DM= DM0 ~ DM3

 Don't Care

**Figure 19. Write to Write Max tDQSS, Non Consecutive**


$DI_n$ , etc. = Data In for column n, etc.

3 subsequent elements of Data In are applied in the programmed order following  $DI_n$

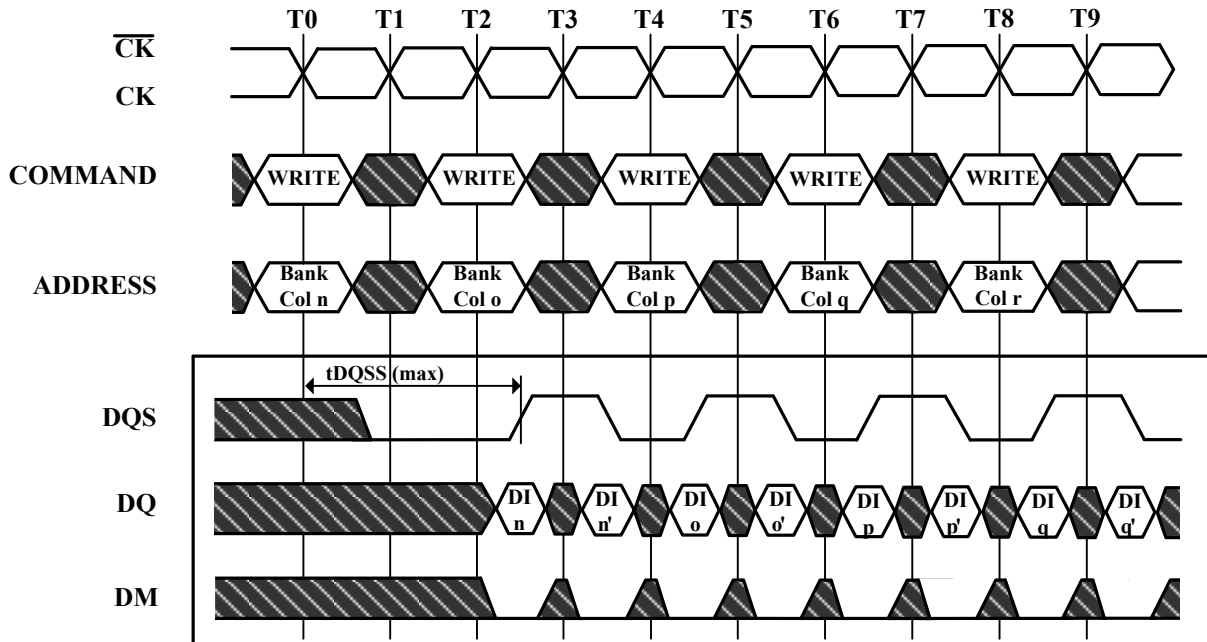
3 subsequent elements of Data In are applied in the programmed order following  $DI_o$

Non-interrupted bursts of 4 are shown

DM= DM0 ~ DM3

 Don't Care



**Figure 20. Random Write Cycles Max tDQSS**


DI n, etc. = Data In for column n, etc.

n', etc. = the next Data In following DI n, etc. according to the programmed burst order

Programmed Burst Length 2, 4, or 8 in cases shown

If burst of 4 or 8, the burst would be truncated

Each WRITE command may be to any bank and may be to the same or different devices

DM= DM0 ~ DM3

 Don't Care

**Figure 21. Write to Read Max tDQSS Non Interrupting**


DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 2 is shown

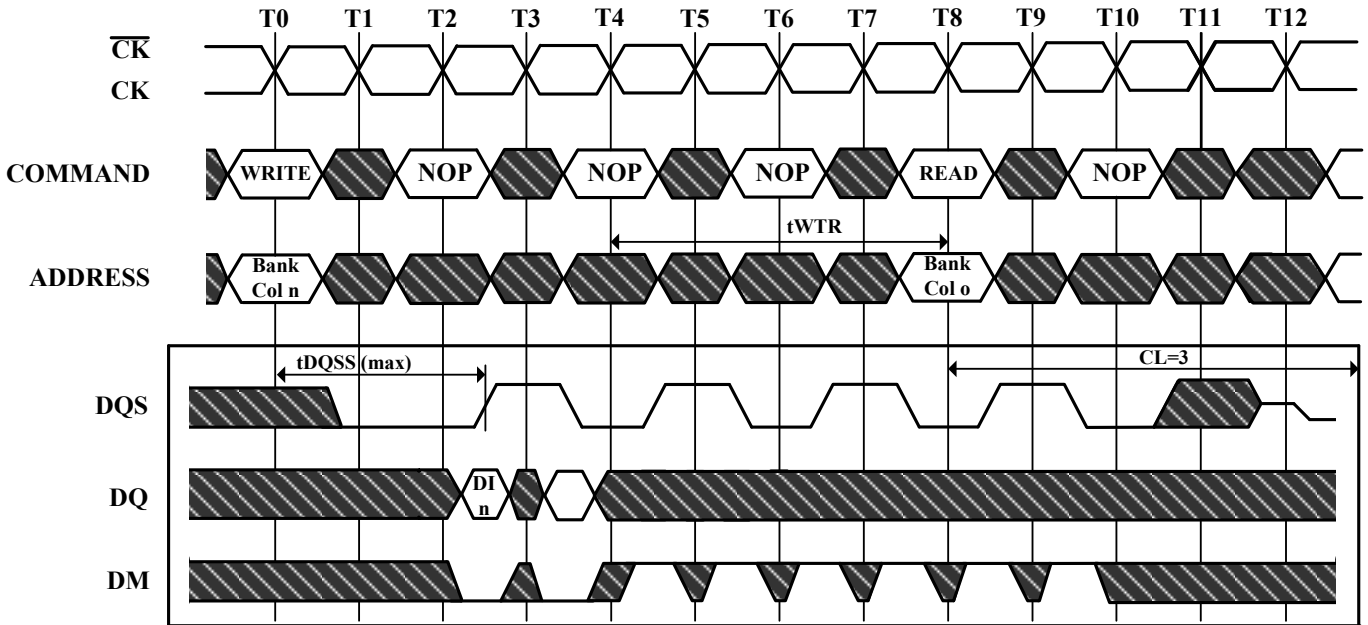
tWTR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= DM0 ~ DM3

 Don't Care

**Figure 22. Write to Read Max tDQSS Interrupting**


DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

An interrupted burst of 8 is shown, 2 data elements are written

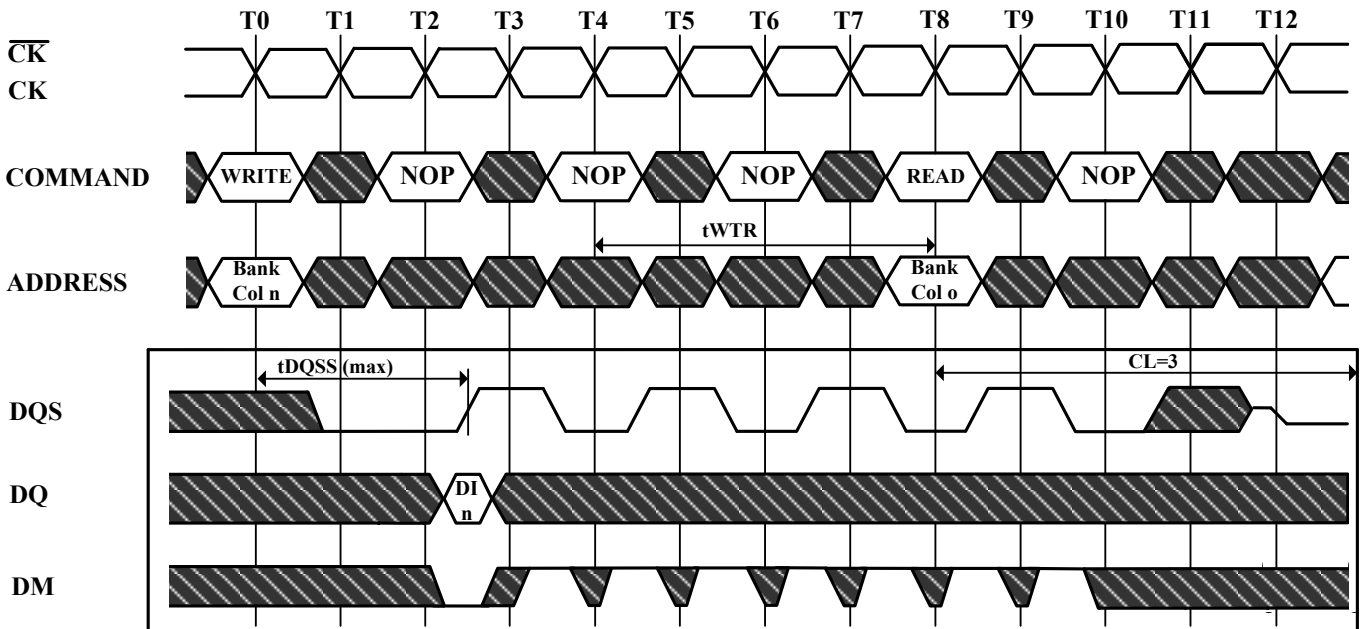
tWTR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= DM0 ~ DM3

 Don't Care

**Figure 23. Write to Read Max tDQSS, ODD Number of Data, Interrupting**


$DI_n$  = Data In for column n

An interrupted burst of 8 is shown, 1 data elements are written

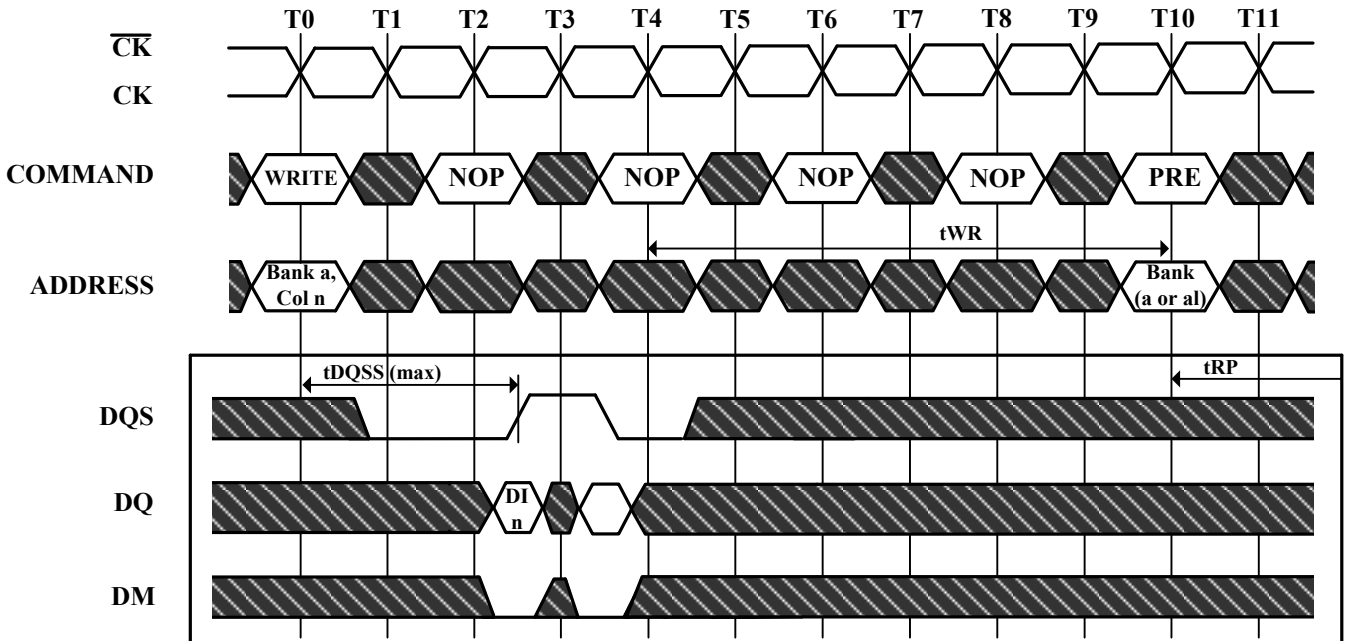
$t_{WTR}$  is referenced from the first positive CK edge after the last Data In Pair (not the last desired Data In element)

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= DM0 ~ DM3

 Don't Care

**Figure 24. Write to Precharge Max tDQSS, NON- Interrupting**


$DI_n$  = Data In for column n

1 subsequent elements of Data In are applied in the programmed order following  $DI_n$

A non-interrupted burst of 2 is shown

$t_{WR}$  is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

DM= DM0 ~ DM3

 Don't Care

**Figure 25. Write to Precharge Max tDQSS, Interrupting**


DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 2 data elements are written

tWR is referenced from the first positive CK edge after the last Data In Pair

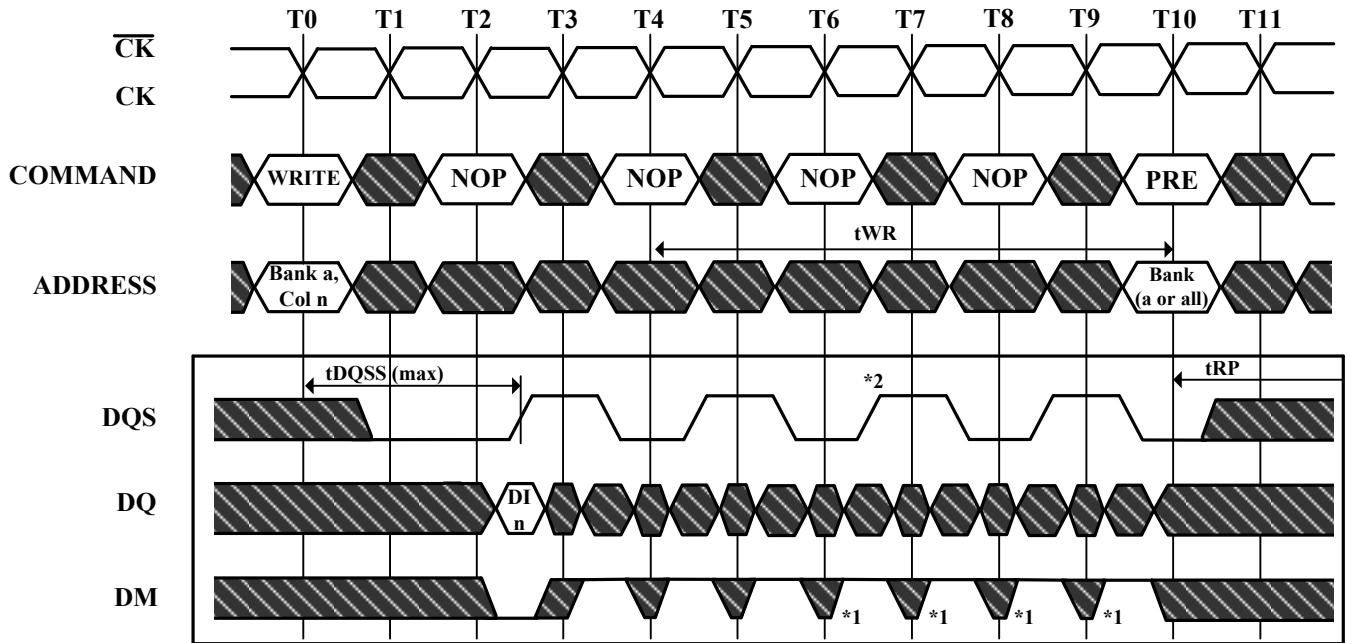
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

\*1 = can be don't care for programmed burst length of 4

\*2 = for programmed burst length of 4, DQS becomes don't care at this point

DM= DM0 ~ DM3

 Don't Care

**Figure 26. Write to Precharge Max tDQSS ODD Number of Data Interrupting**


DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 1 data element is written

$t_{WR}$  is referenced from the first positive CK edge after the last Data In Pair

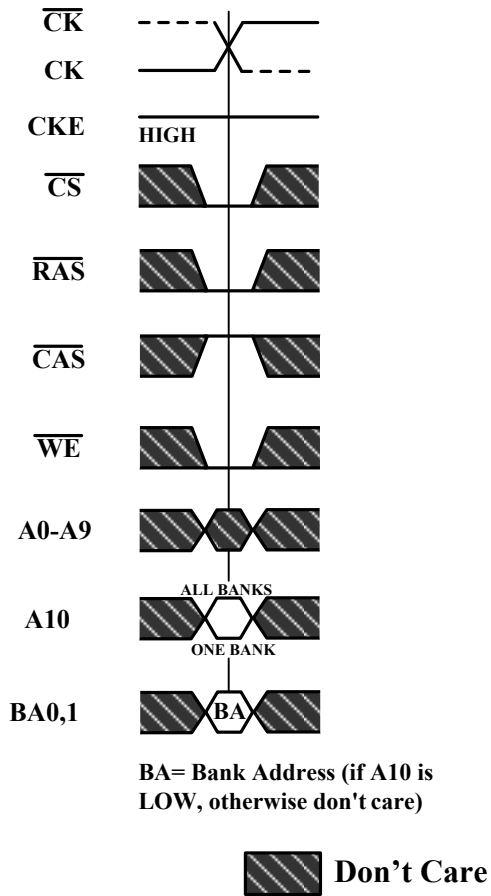
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

\*1 = can be don't care for programmed burst length of 4

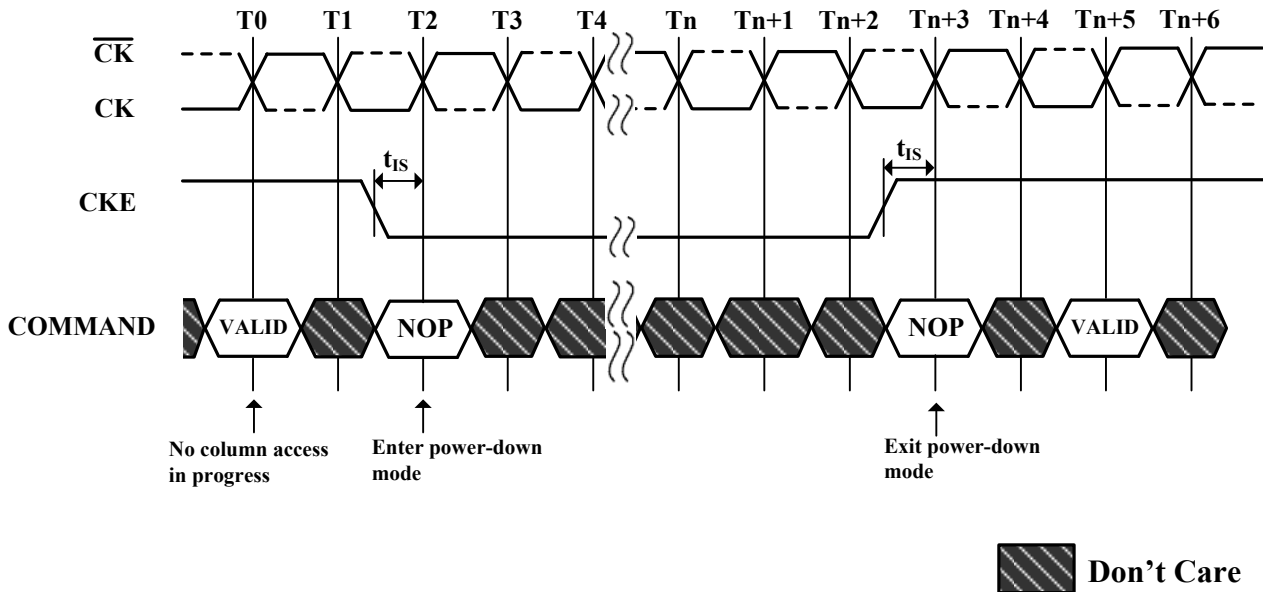
\*2 = for programmed burst length of 4, DQS becomes don't care at this point

DM= DM0 ~ DM3

 Don't Care

**Figure 27. Precharge Command**




**Figure 28. Power-Down**

**Figure 29. Clock Frequency Change in Precharge**


**Figure 30. Data input (Write) Timing**


DI<sub>n</sub> = Data In for column n

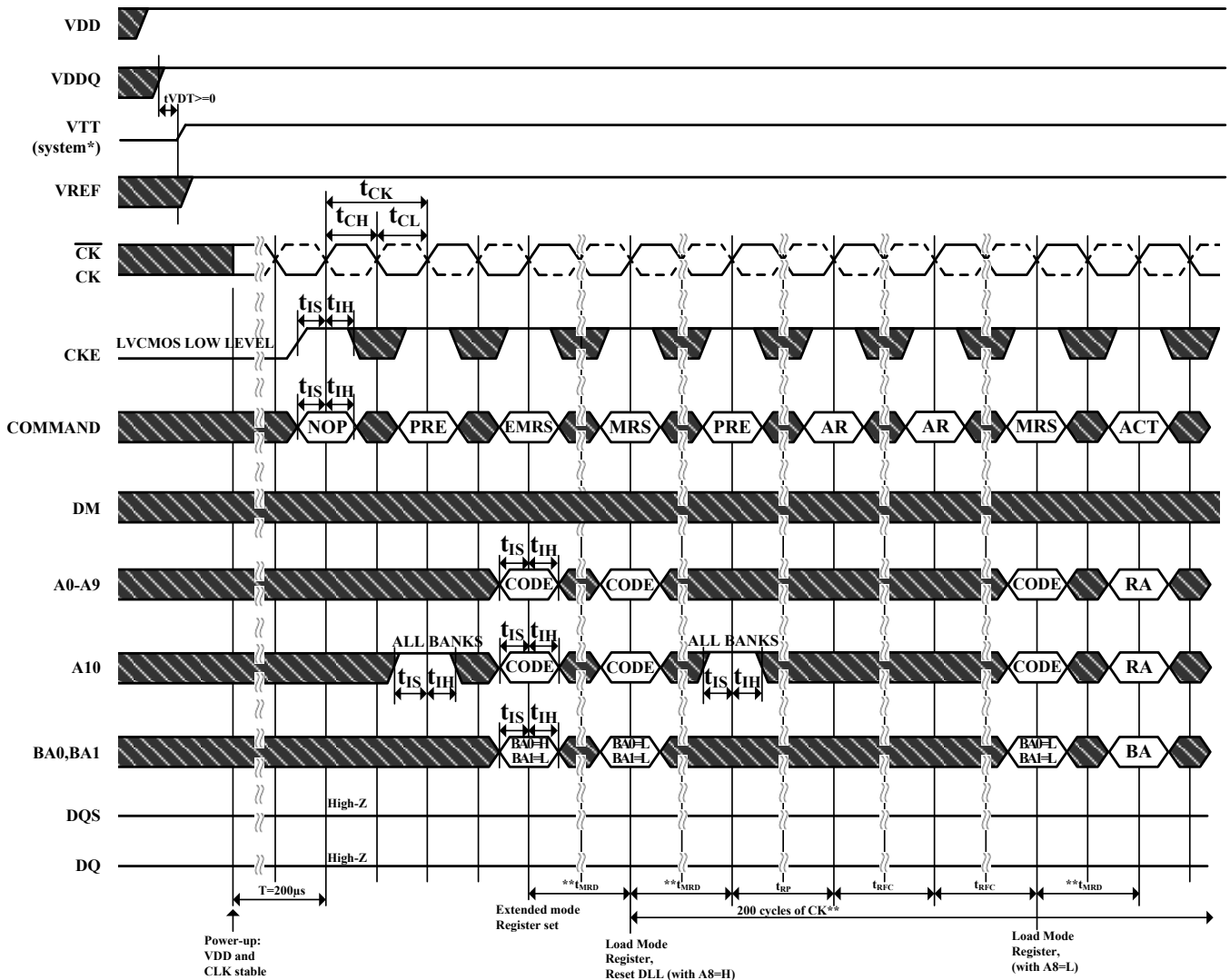
Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI<sub>n</sub>

 Don't Care

**Figure 31. Data Output (Read) Timing**


Burst Length = 4 in the case shown

**Figure 32. Initialize and Mode Register Sets**


\*=VTT is not applied directly to the device, however  $t_{VTD}$  must be greater than or equal to zero to avoid device latch-up.

\*\* =  $t_{MRD}$  is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied the two auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

 Don't Care

**Figure 33. Power Down Mode**


No column accesses are allowed to be in progress at the time Power-Down is entered

\*=If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is active Power Down.

 Don't Care

**Figure 34. Auto Refresh Mode**


\* = " Don't Care" , if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other valid commands may be possible after  $t_{RFC}$

DM, DQ and DQS signals are all " Don't Care" /High-Z for operations shown

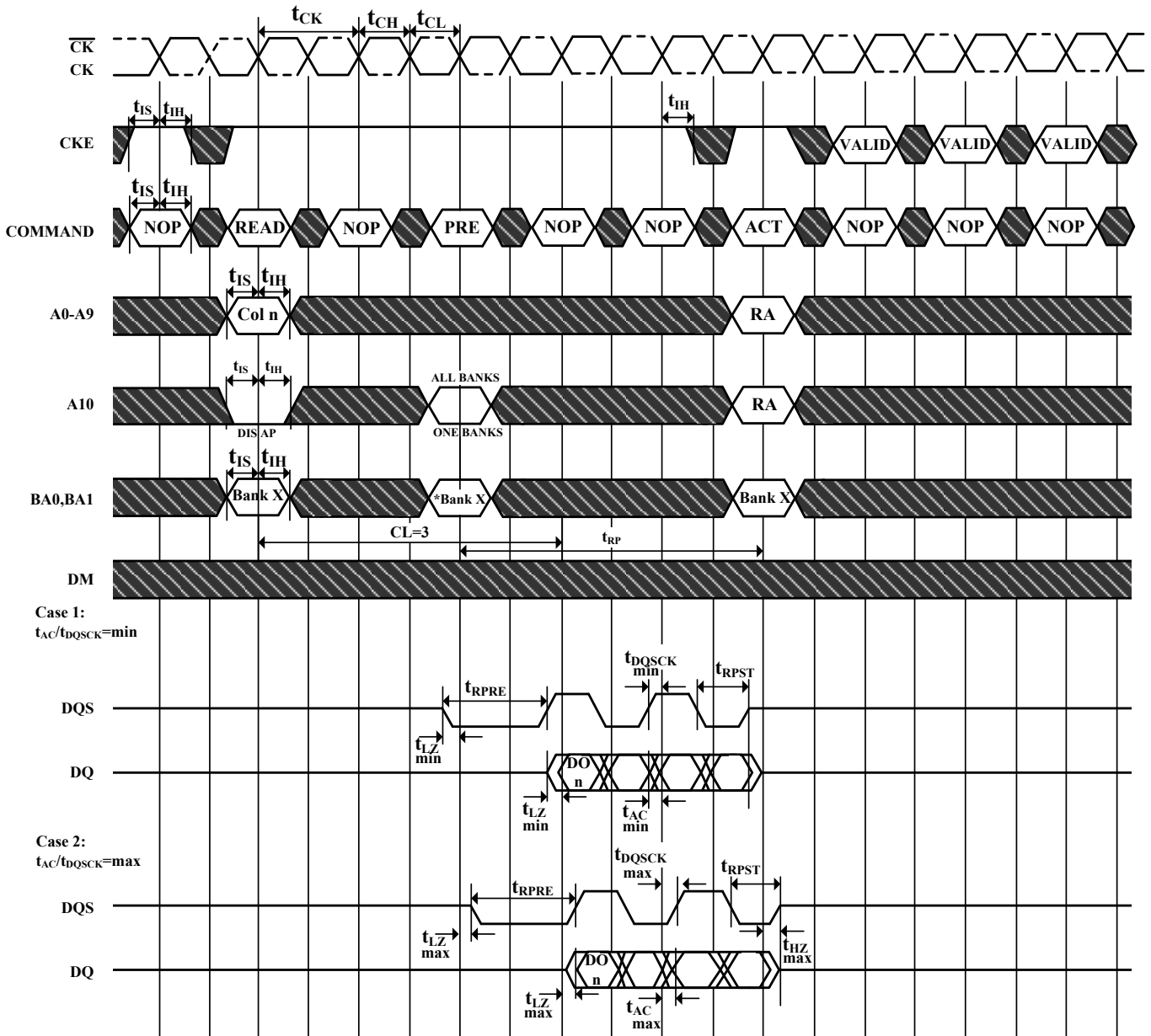
 Don't Care

**Figure 35. Self Refresh Mode**


\* = Device must be in the " All banks idle" state prior to entering Self Refresh mode

\*\* =  $t_{XSNR}$  is required before any non-READ command can be applied, and  $t_{XSRD}$  (200 cycles of CK) is required before a READ command can be applied.

 Don't Care

**Figure 36. Read without Auto Precharge**


DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

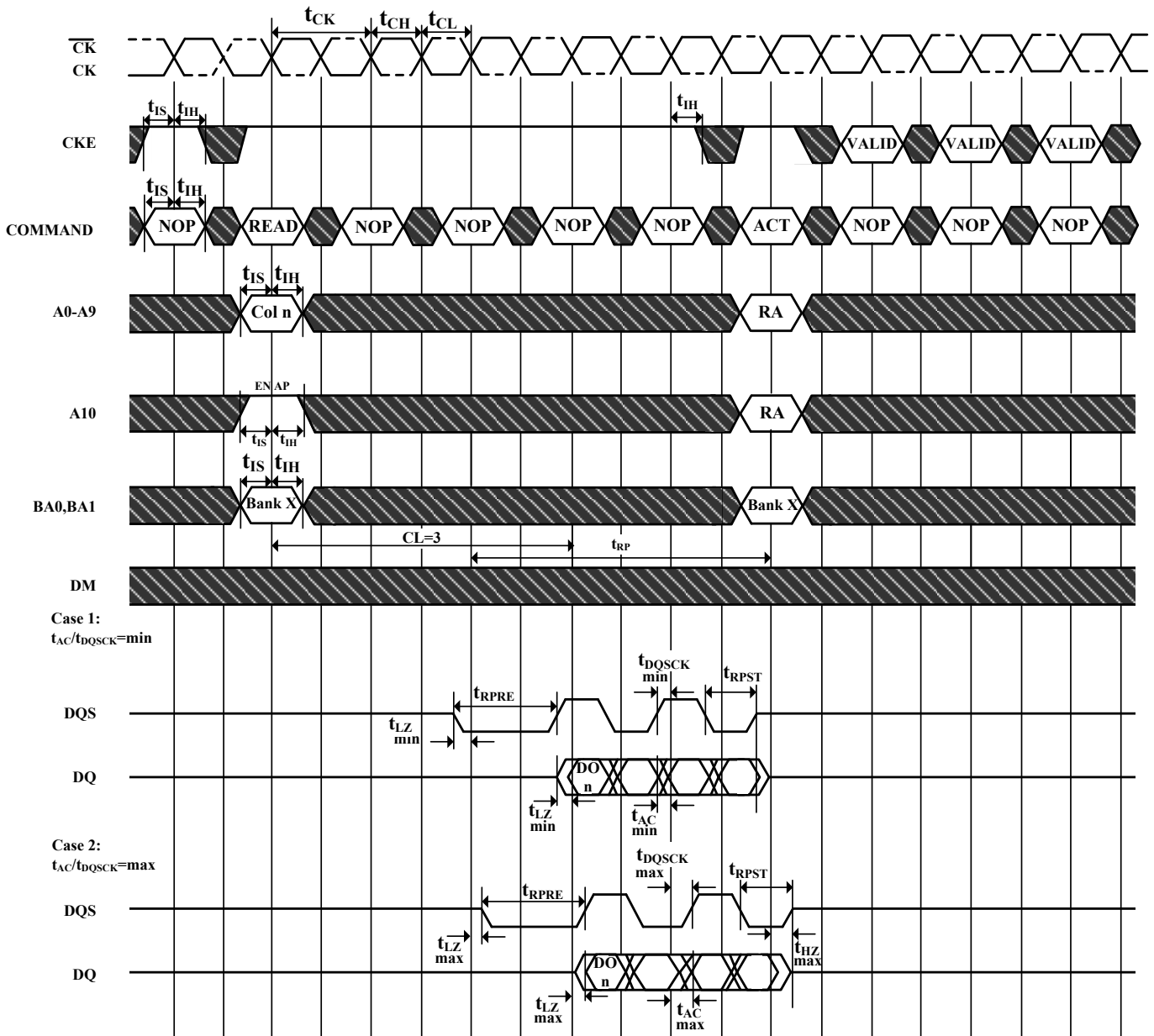
\* = " Don't Care " , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other commands may be valid at these times

Precharge may not be issued before  $t_{RAS}$  ns after the ACTIVE command for applicable banks

 **Don't Care**

**Figure 37. Read with Auto Precharge**


DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

The READ command may not be issued until tRAP has been satisfied. Support Fast Autoprecharge, tRAP = tRCD, But it still needs tRC to next ACT.

 Don't Care



**Figure 38. Bank Read Access**


DO n = Data Out from column n  
Burst Length = 4 in the case shown

↳ subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

\* = " Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Note that  $t_{RCD} > t_{RCD\ MIN}$  so that the same timing applies if Autoprecharge is enabled (in which case  $t_{RAS}$  would be limiting)

 Don't Care

**Figure 39. Write without Auto Precharge**


DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

\*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the  $\pm 25\%$  window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

 Don't Care

**Figure 40. Write with Auto Precharge**


DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although  $t_{DQSS}$  is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the +25% window of the corresponding positive clock edge

 Don't Care

**Figure 41. Bank Write Access**


DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

\*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although t<sub>DQSS</sub> is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the + 25% window of the corresponding positive clock edge

Precharge may not be issued before t<sub>RAS</sub> ns after the ACTIVE command for applicable banks

 Don't Care

**Figure 42. Write DM Operation**


DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

\*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

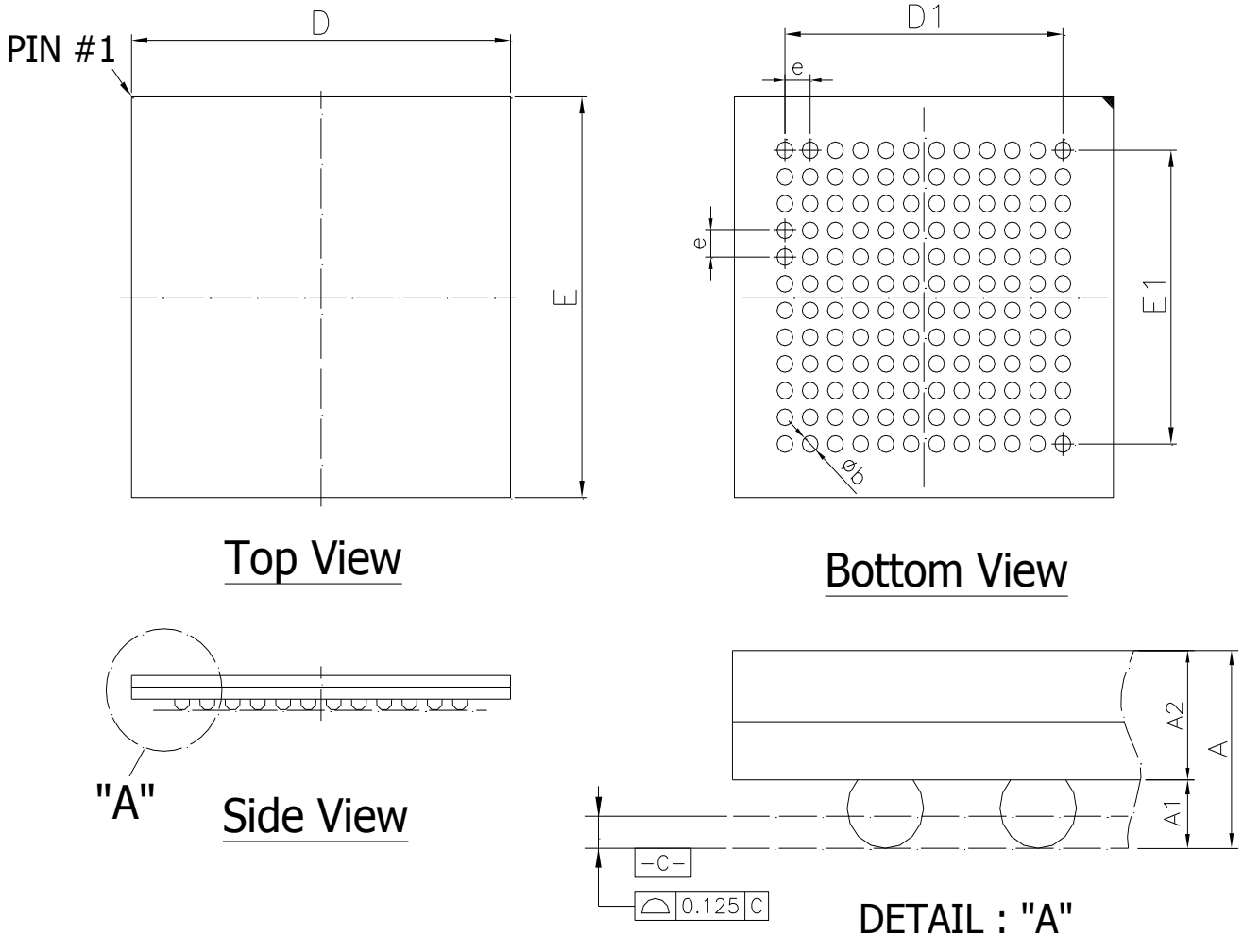
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the  $\pm 25\%$  window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

 **Don't Care**

Figure 43. 144 ball LFBGA Package Outline Drawing Information  
 Units: mm



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.055	--	--	1.40
A1	0.012	0.014	0.016	0.30	0.35	0.40
A2	0.036	0.038	0.040	0.91	0.96	1.01
D	0.469	0.472	0.476	11.90	12.00	12.10
E	0.469	0.472	0.476	11.90	12.00	12.10
D1	--	0.346	--	--	8.80	--
E1	--	0.346	--	--	8.80	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50

**PART NUMBERING SYSTEM**

AS4C	2M32D1A	5	B	C/I	N
DRAM	2M32=2Mx32 D1=DDR A = Die Revision	5=200MHz	B = FBGA	C=Commercial (0° C~70° C) I =Industrial (-40° C~85° C)	Indicates Pb and Halogen Free



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