

Automotive-grade N-channel 80 V, 1.7 mΩ typ., 180 A,
STripFET™ F7 Power MOSFETs in H²PAK-2 and H²PAK-6

Datasheet - production data

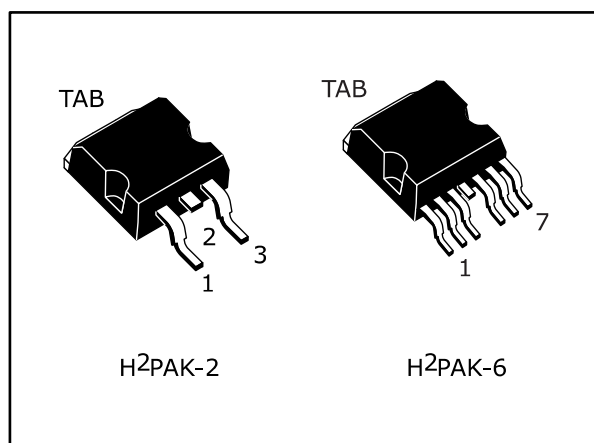
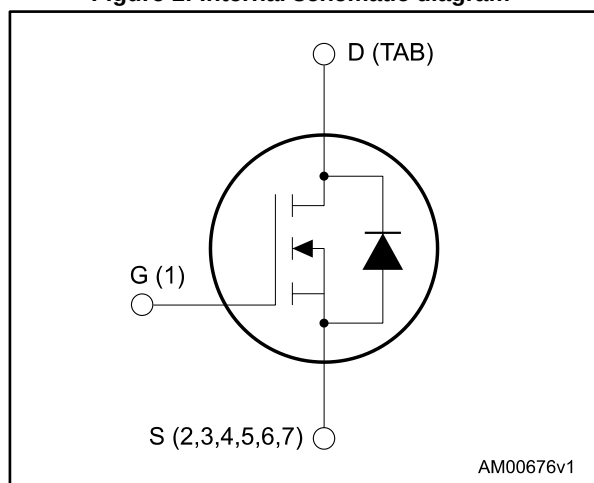


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH275N8F7-2AG	80 V	2.1 mΩ	180 A
STH275N8F7-6AG			

- AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness



Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STH275N8F7-2AG	275N8F7	H ² PAK-2	Tape and reel
STH275N8F7-6AG		H ² PAK-6	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	180	
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	315	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	0.775	J
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾ Limited by package.

⁽²⁾ Pulse width is limited by safe operating area.

⁽³⁾ Starting $T_j = 25\text{ }^\circ\text{C}$, $I_d = 65\text{ A}$, $V_{dd} = 50\text{ V}$, $T_j < T_{j-max}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	

Notes:

⁽¹⁾ When mounted on FR-4 board of 1 inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	80			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 80 V			1	μA
		V _{GS} = 0 V, V _{DS} = 80 V, T _C = 125 °C ⁽¹⁾			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = +20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 90 A		1.7	2.1	mΩ

Notes:

⁽¹⁾ Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	13600	-	pF
C _{oss}	Output capacitance		-	2050	-	
C _{rss}	Reverse transfer capacitance		-	236	-	
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 180 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	193	-	nC
Q _{gs}	Gate-source charge		-	96	-	
Q _{gd}	Gate-drain charge		-	46	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 40 V, I _D = 90 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 18: "Switching time waveform")	-	56	-	ns
t _r	Rise time		-	180	-	
t _{d(off)}	Turn-off delay time		-	98	-	
t _f	Fall time		-	42	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 90 \text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 180 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 64 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	78		ns
Q_{rr}	Reverse recovery charge		-	182		nC
I_{RRM}	Reverse recovery current		-	4.7		A

Notes:

⁽¹⁾ Pulse width limited by safe operating area.

⁽²⁾ Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

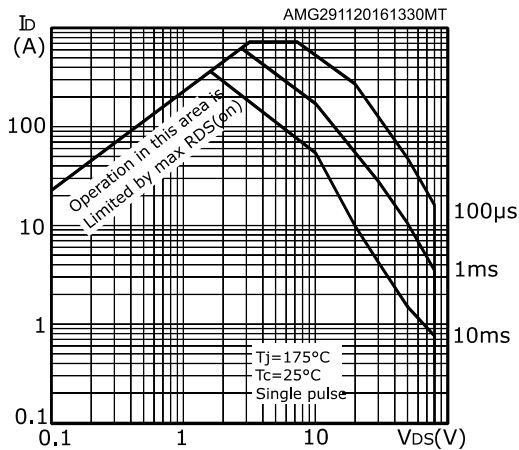


Figure 3: Thermal impedance

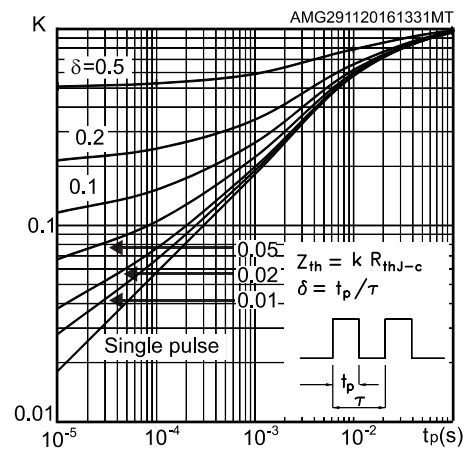


Figure 4: Gate charge vs gate-source voltage

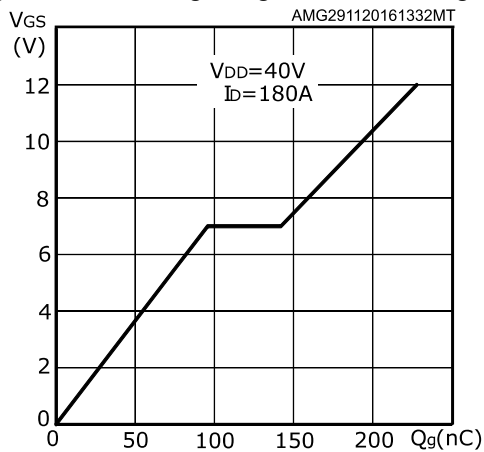


Figure 5: Output characteristics

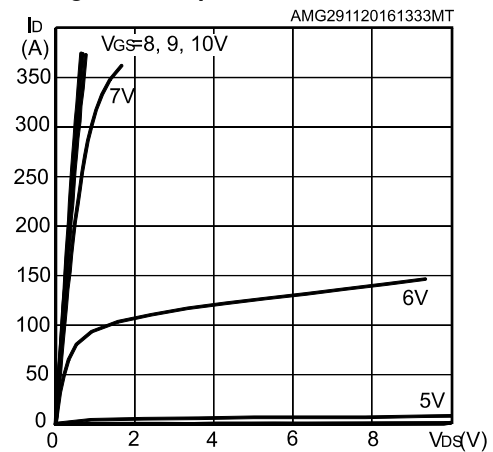


Figure 6: Transfer characteristics

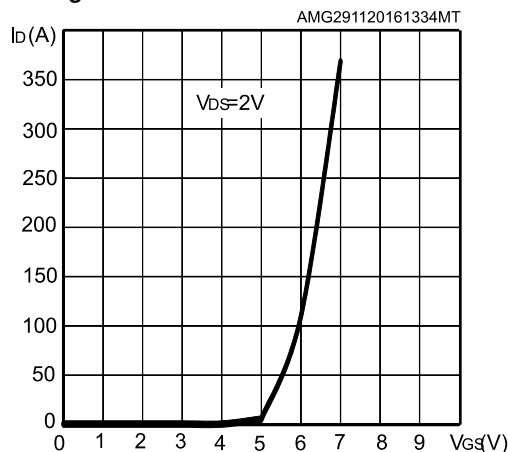
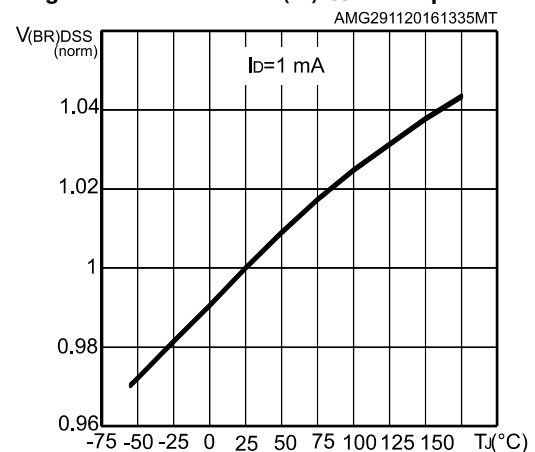
Figure 7: Normalized $V_{(BR)DSS}$ vs temperature

Figure 8: Static drain-source on-resistance

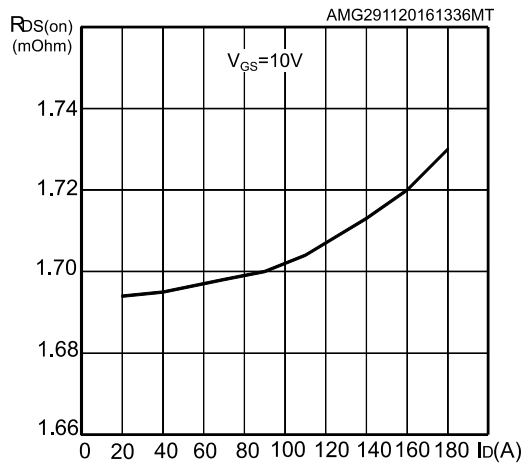


Figure 9: Capacitance variations

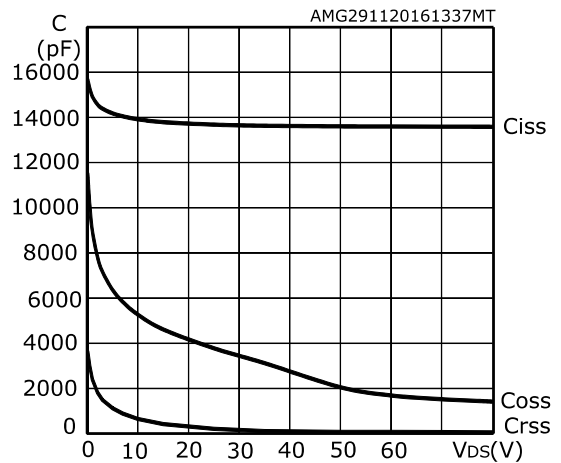


Figure 10: Source-drain diode forward characteristics

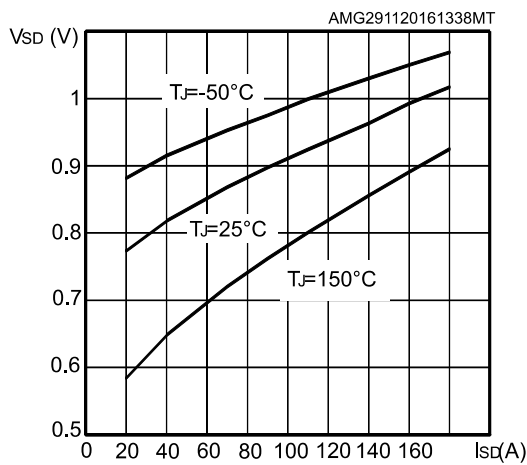


Figure 11: Normalized gate threshold voltage vs temperature

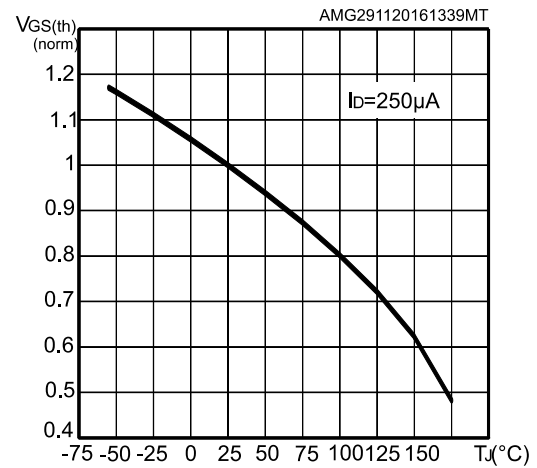
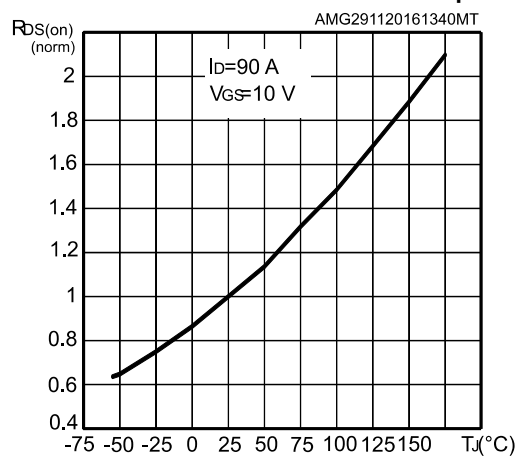
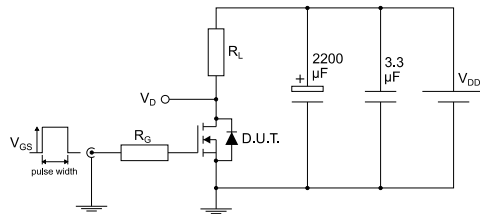


Figure 12: Normalized on-resistance vs temperature



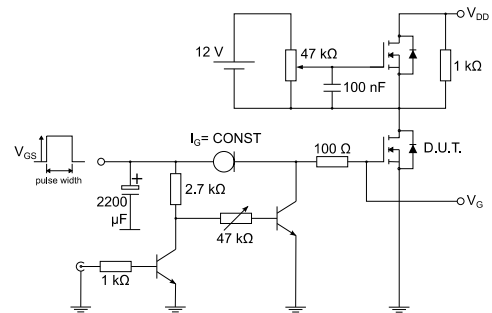
3 Test circuits

Figure 13: Test circuit for resistive load switching times



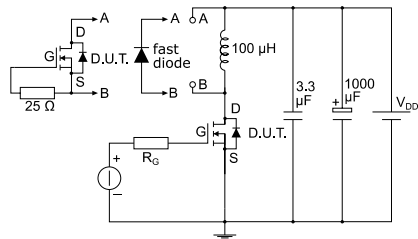
AM01468v1

Figure 14: Test circuit for gate charge behavior



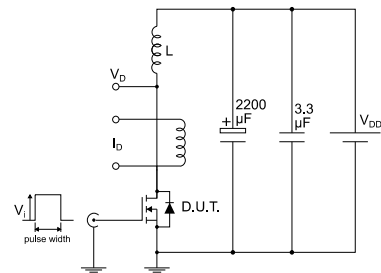
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



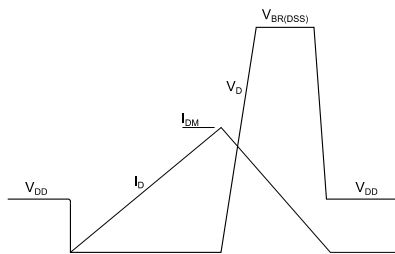
AM01470v1

Figure 16: Unclamped inductive load test circuit



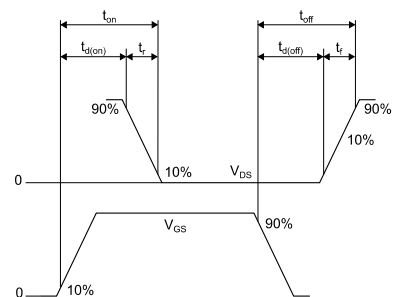
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform

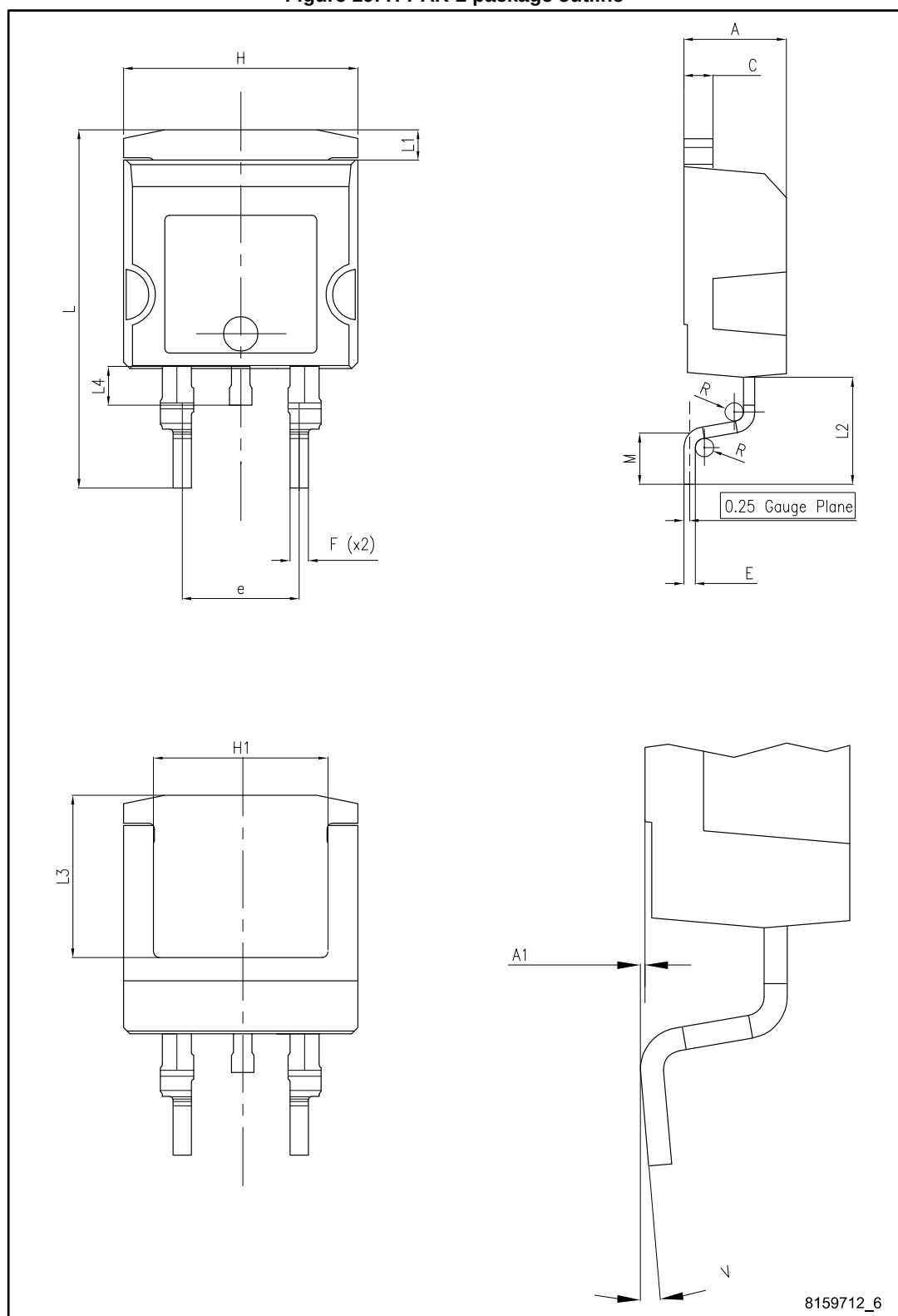


AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 H²PAK-2 package information

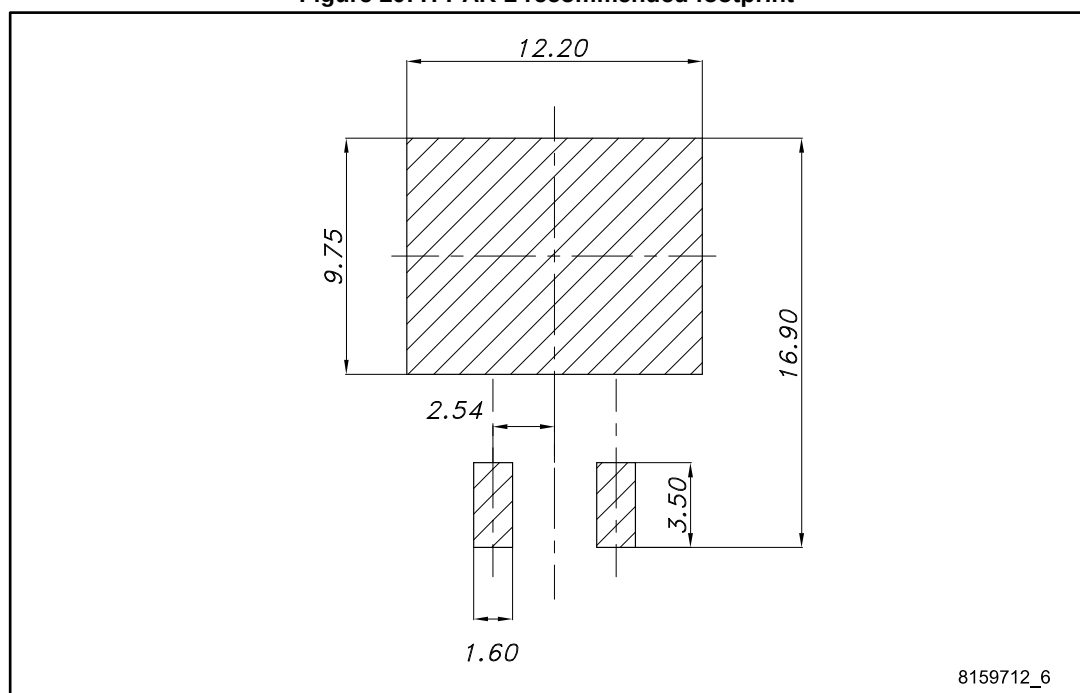
Figure 19: H²PAK-2 package outline

8159712_6

Table 8: H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-2 recommended footprint



4.2 H²PAK-6 package information

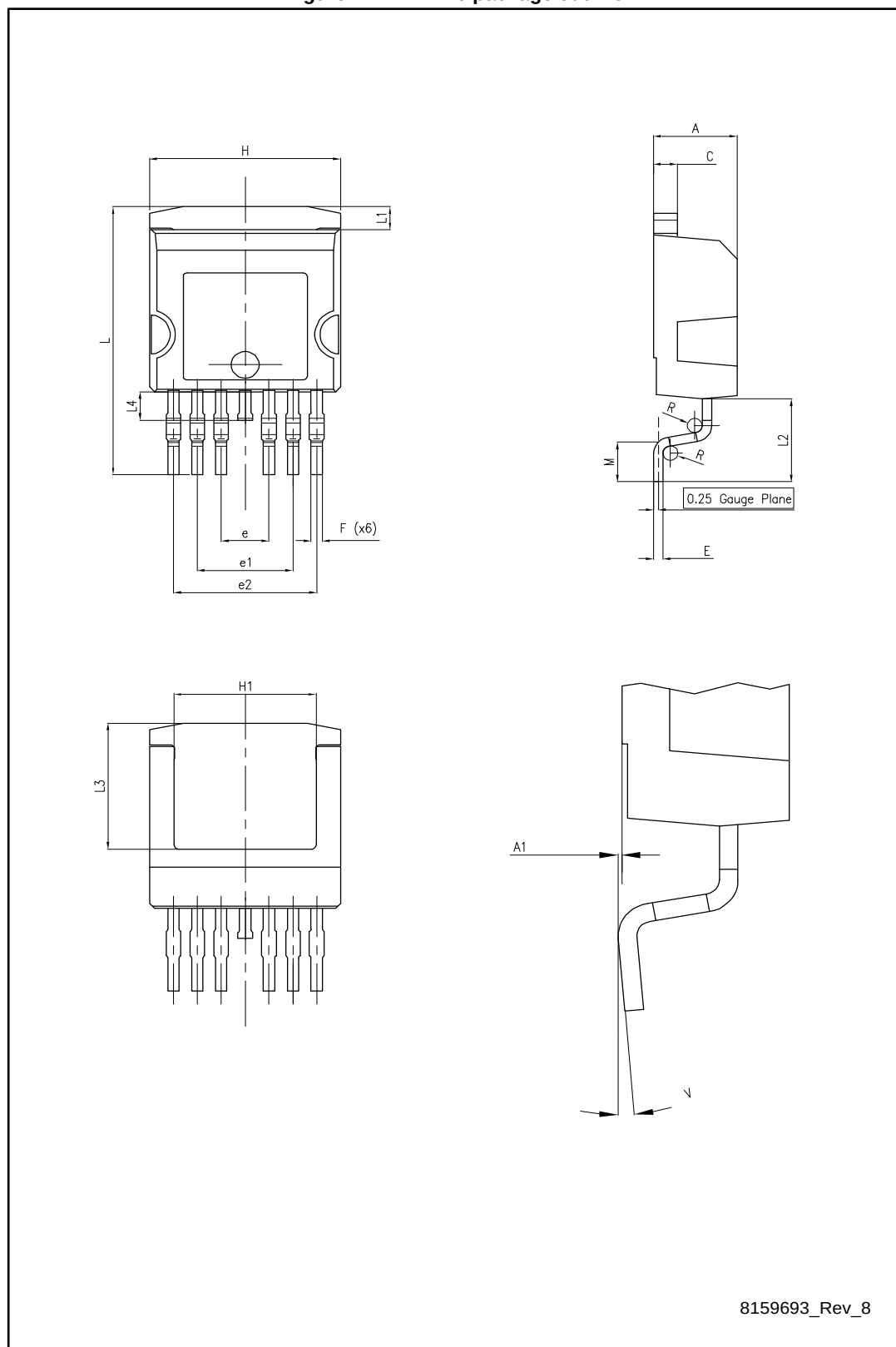
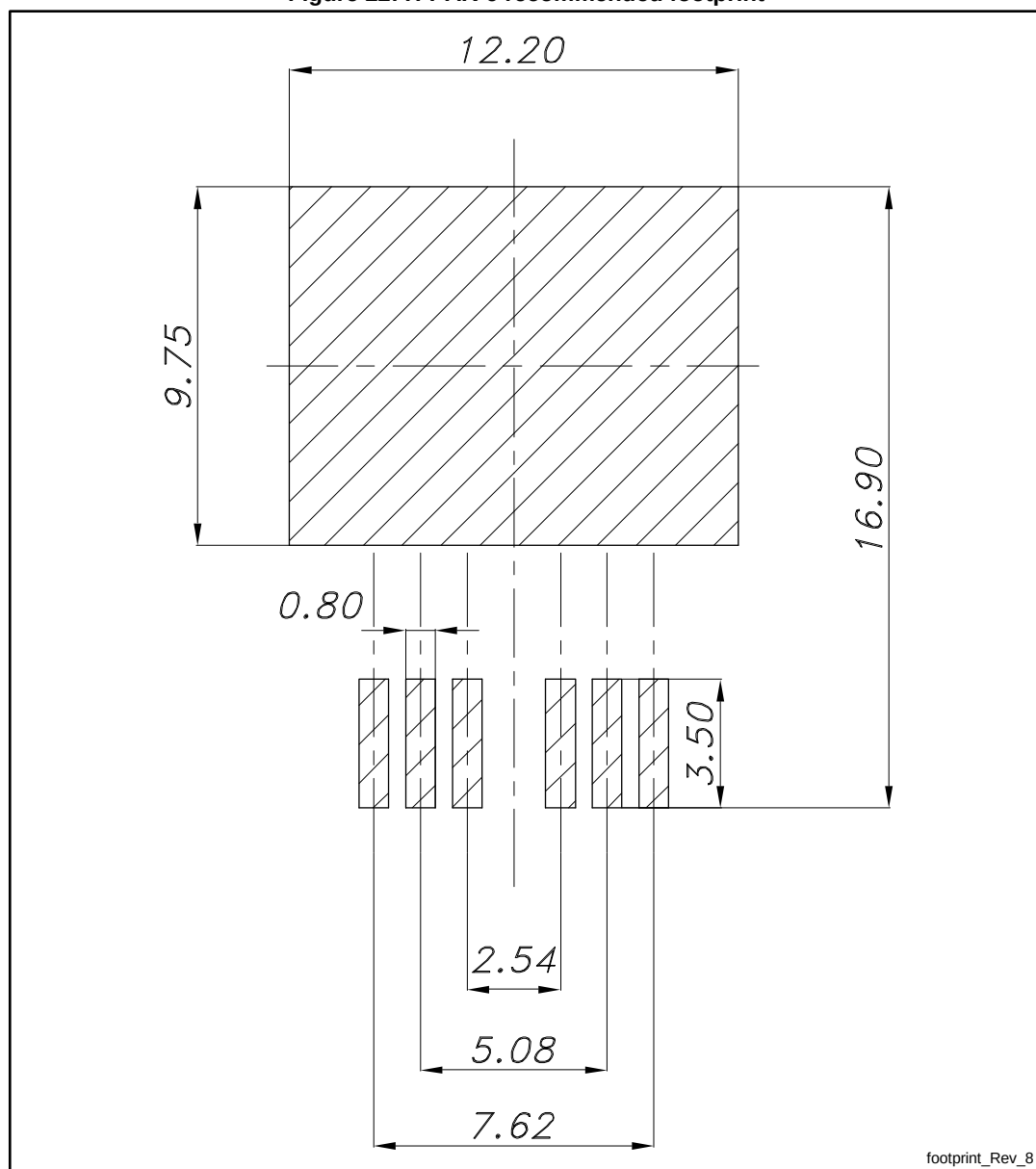
Figure 21: H²PAK-6 package outline

Table 9: H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	2.34	2.54	2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.50		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22: H²PAK-6 recommended footprint

Dimensions are in mm.

4.3 H²PAK packing information

Figure 23: Tape outline

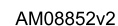


Figure 24: Reel outline

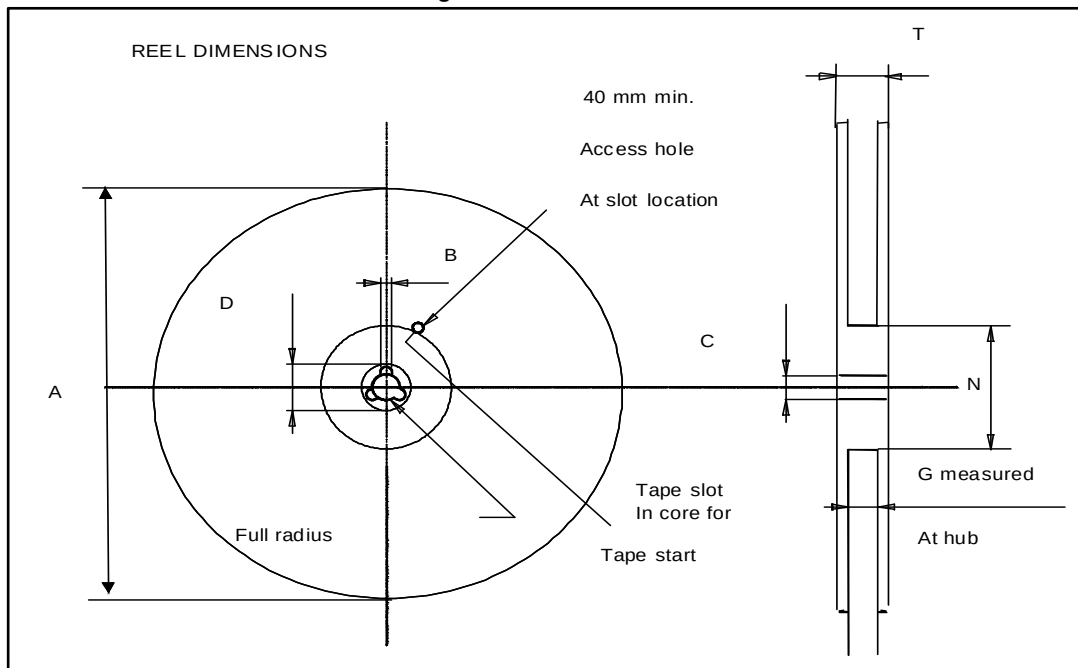


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
27-Nov-2014	1	First release.
05-Mar-2015	2	Document status promoted from preliminary to production data. Updated title and feature in cover page.
10-Mar-2016	3	Updated Table 4. Minor text changes.
10-Jan-2017	4	Updated title and features in cover page. Updated Table 2: "Absolute maximum ratings" , Table 4: "On/off states" and Table 6: "Switching times" . Minor text changes.

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