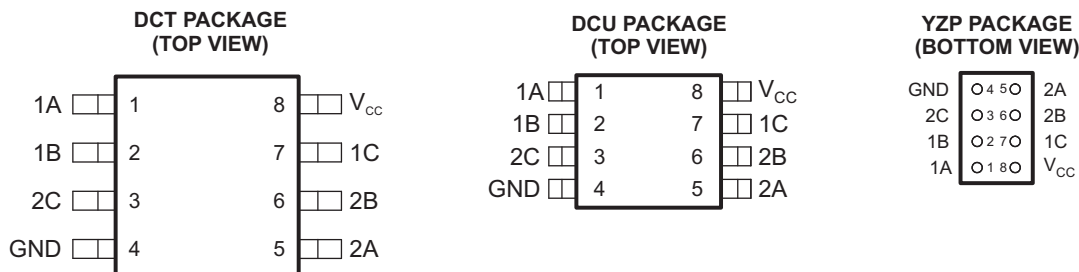


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- 1.65-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 0.8 ns at 3.3 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns ($V_{CC} = 3\text{ V}$, $C_L = 50\text{ pF}$)
- Rail-to-Rail Input/Output
- Low On-State Resistance, Typically $\approx 6\ \Omega$ ($V_{CC} = 4.5\text{ V}$)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽²⁾ |
|---------------|--|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74LVC2G66YZPR | ___C6_ |
| | SSOP – DCT | Reel of 3000 | SN74LVC2G66DCTR | C66___ |
| | VSSOP – DCU | Reel of 3000 | SN74LVC2G66DCUR | C66_ |
| | | Reel of 250 | SN74LVC2G66DCUT | |

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

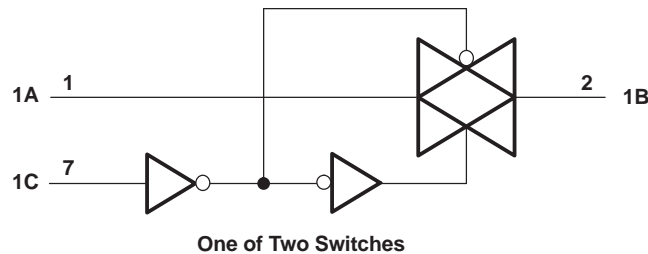
SN74LVC2G66 DUAL BILATERAL ANALOG SWITCH

SCES325J–JULY 2001–REVISED FEBRUARY 2007

**FUNCTION TABLE
(EACH SECTION)**

| CONTROL INPUT (C) | SWITCH |
|-------------------|--------|
| L | Off |
| H | On |

LOGIC DIAGRAM, EACH SWITCH (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|---|-------------------------------------|----------------|------|
| V_{CC} | Supply voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾⁽³⁾ | -0.5 | 6.5 | V |
| V_O | Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Control input clamp current | $V_I < 0$ | -50 | mA |
| $I_{I/OK}$ | I/O port diode current | $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$ | -50 | mA |
| I_T | On-state switch current | $V_{I/O} = 0$ to V_{CC} | ± 50 | mA |
| Continuous current through V_{CC} or GND | | | ± 100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁵⁾ | DCT package | 220 | °C/W |
| | | DCU package | 227 | |
| | | YZP package | 102 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|------------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 1.65 | 5.5 | V |
| V _{I/O} | I/O port voltage | 0 | V _{CC} | V |
| V _{IH} | High-level input voltage, control input | V _{CC} = 1.65 V to 1.95 V | V _{CC} × 0.65 | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.7 | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.7 | |
| V _{IL} | Low-level input voltage, control input | V _{CC} = 1.65 V to 1.95 V | V _{CC} × 0.35 | V |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.3 | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.3 | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.3 | |
| V _I | Control input voltage | 0 | 5.5 | V |
| Δt/Δv | Input transition rise/fall time | V _{CC} = 1.65 V to 1.95 V | 20 | ns/V |
| | | V _{CC} = 2.3 V to 2.7 V | 20 | |
| | | V _{CC} = 3 V to 3.6 V | 10 | |
| | | V _{CC} = 4.5 V to 5.5 V | 10 | |
| T _A | Operating free-air temperature | –40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC2G66

DUAL BILATERAL ANALOG SWITCH

SCES325J–JULY 2001–REVISED FEBRUARY 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|--|--|------------------------|--------|--------------------|---------------------------|------|
| r _{on} | On-state switch resistance | V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 1 and Figure 2) | I _S = 4 mA | 1.65 V | 12.5 | 30 | Ω |
| | | | I _S = 8 mA | 2.3 V | 9 | 20 | |
| | | | I _S = 24 mA | 3 V | 7.5 | 15 | |
| | | | I _S = 32 mA | 4.5 V | 6 | 10 | |
| r _{on(p)} | Peak on-state resistance | V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1 and Figure 2) | I _S = 4 mA | 1.65 V | 85 | 120 ⁽¹⁾ | Ω |
| | | | I _S = 8 mA | 2.3 V | 22 | 30 ⁽¹⁾ | |
| | | | I _S = 24 mA | 3 V | 12 | 20 | |
| | | | I _S = 32 mA | 4.5 V | 7.5 | 15 | |
| Δr _{on} | Difference of on-state resistance between switches | V _I = V _{CC} to GND, V _C = V _{IH} (see Figure 1 and Figure 2) | I _S = 4 mA | 1.65 V | | 7 | Ω |
| | | | I _S = 8 mA | 2.3 V | | 5 | |
| | | | I _S = 24 mA | 3 V | | 3 | |
| | | | I _S = 32 mA | 4.5 V | | 2 | |
| I _{S(off)} | Off-state switch leakage current | V _I = V _{CC} and V _O = GND or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 3) | 5.5 V | | | ±1 ±0.1 ⁽¹⁾ | μA |
| I _{S(on)} | On-state switch leakage current | V _I = V _{CC} or GND, V _C = V _{IH} , V _O = Open (see Figure 4) | 5.5 V | | | ±1 ±0.1 ⁽¹⁾ | μA |
| I _I | Control input current | V _C = V _{CC} or GND | 5.5 V | | | ±1 ±0.1 ⁽¹⁾ | μA |
| I _{CC} | Supply current | V _C = V _{CC} or GND | 5.5 V | | | 10 1 ⁽¹⁾ | μA |
| ΔI _{CC} | Supply-current change | V _C = V _{CC} – 0.6 V | 5.5 V | | | 500 | μA |
| C _{ic} | Control input capacitance | | 5 V | | 3.5 | | pF |
| C _{io(off)} | Switch input/output capacitance | | 5 V | | 6 | | pF |
| C _{io(on)} | Switch input/output capacitance | | 5 V | | 14 | | pF |

(1) T_A = 25°C

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|---------------------------------|--------------|-------------|----------------------------------|------|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} ⁽¹⁾ | A or B | B or A | | 2 | | 1.2 | | 0.8 | | 0.6 | ns |
| t _{en} ⁽²⁾ | C | A or B | 2.3 | 10 | 1.6 | 5.6 | 1.5 | 4.4 | 1.3 | 3.9 | ns |
| t _{dis} ⁽³⁾ | C | A or B | 2.5 | 10.5 | 1.2 | 6.9 | 2 | 7.2 | 1.1 | 6.3 | ns |

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Analog Switch Characteristics

T_A = 25°C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|---|--------------|-------------|--|-----------------|-------|------|
| Frequency response (switch on) | A or B | B or A | C _L = 50 pF, R _L = 600 Ω, f _{in} = sine wave (see Figure 6) | 1.65 V | 35 | MHz |
| | | | | 2.3 V | 120 | |
| | | | | 3 V | 175 | |
| | | | | 4.5 V | 195 | |
| | | | C _L = 5 pF, R _L = 50 Ω, f _{in} = sine wave (see Figure 6) | 1.65 V | >300 | |
| | | | | 2.3 V | >300 | |
| | | | | 3 V | >300 | |
| | | | | 4.5 V | >300 | |
| Crosstalk ⁽¹⁾ (between switches) | A or B | B or A | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Figure 7) | 1.65 V | –58 | dB |
| | | | | 2.3 V | –58 | |
| | | | | 3 V | –58 | |
| | | | | 4.5 V | –58 | |
| | | | C _L = 5 pF, R _L = 50 Ω, f _{in} = 1 MHz (sine wave) (see Figure 7) | 1.65 V | –42 | |
| | | | | 2.3 V | –42 | |
| | | | | 3 V | –42 | |
| | | | | 4.5 V | –42 | |
| Crosstalk (control input to signal output) | C | A or B | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave) (see Figure 8) | 1.65 V | 35 | mV |
| | | | | 2.3 V | 50 | |
| | | | | 3 V | 70 | |
| | | | | 4.5 V | 100 | |
| Feedthrough attenuation (switch off) | A or B | B or A | C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave) (see Figure 9) | 1.65 V | –58 | dB |
| | | | | 2.3 V | –58 | |
| | | | | 3 V | –58 | |
| | | | | 4.5 V | –58 | |
| | | | C _L = 5 pF, R _L = 50 Ω, f _{in} = 1 MHz (sine wave) (see Figure 9) | 1.65 V | –42 | |
| | | | | 2.3 V | –42 | |
| | | | | 3 V | –42 | |
| | | | | 4.5 V | –42 | |
| Sine-wave distortion | A or B | B or A | C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave) (see Figure 10) | 1.65 V | 0.1 | % |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |
| | | | C _L = 50 pF, R _L = 10 kΩ, f _{in} = 10 kHz (sine wave) (see Figure 10) | 1.65 V | 0.15 | |
| | | | | 2.3 V | 0.025 | |
| | | | | 3 V | 0.015 | |
| | | | | 4.5 V | 0.01 | |

(1) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | V _{CC} = 5 V | UNIT |
|---|-----------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C _{pd} Power dissipation capacitance | f = 10 MHz | 8 | 9 | 9.5 | 11 | pF |

PARAMETER MEASUREMENT INFORMATION

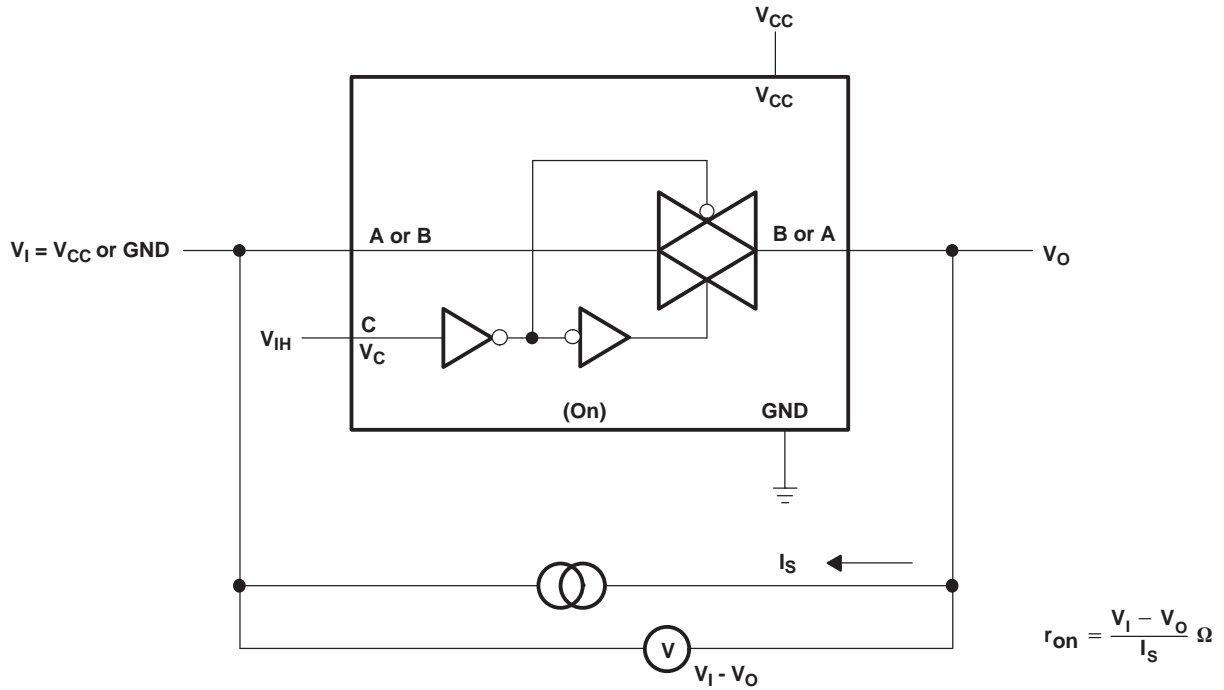


Figure 1. On-State Resistance Test Circuit

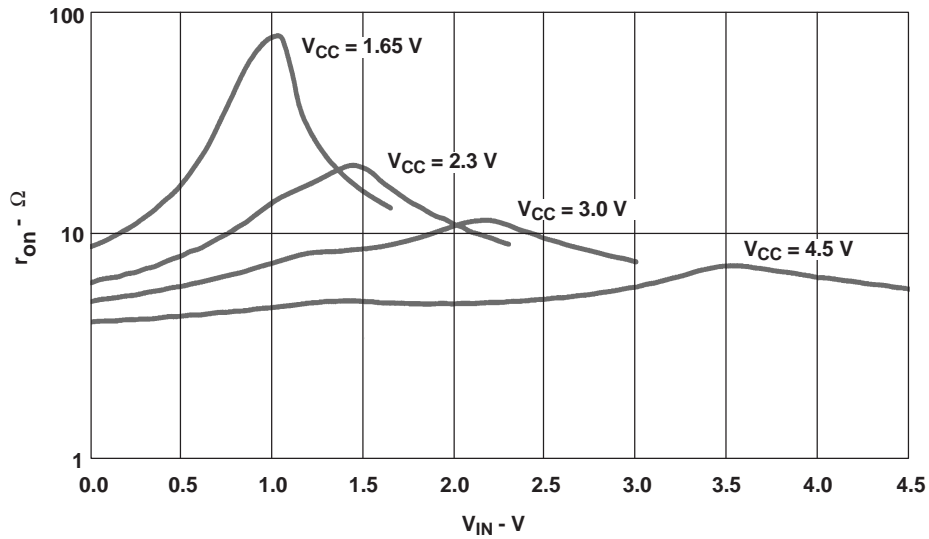


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION

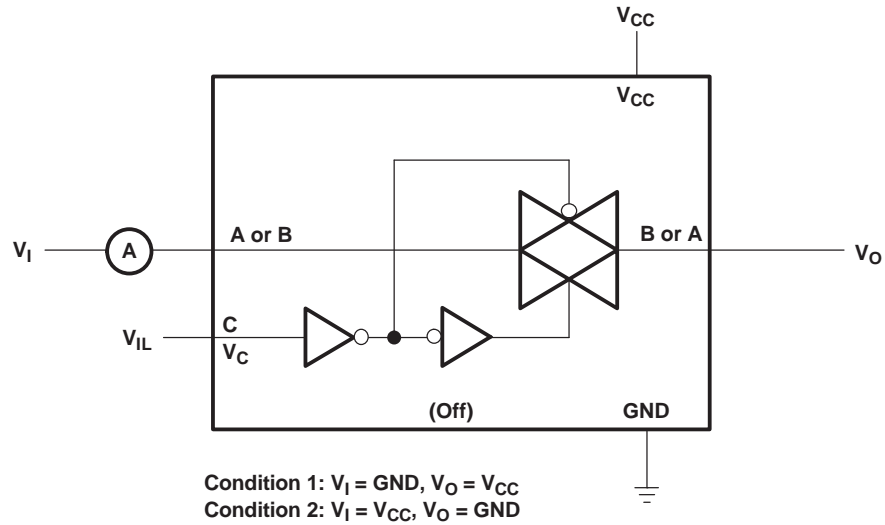


Figure 3. Off-State Switch Leakage-Current Test Circuit

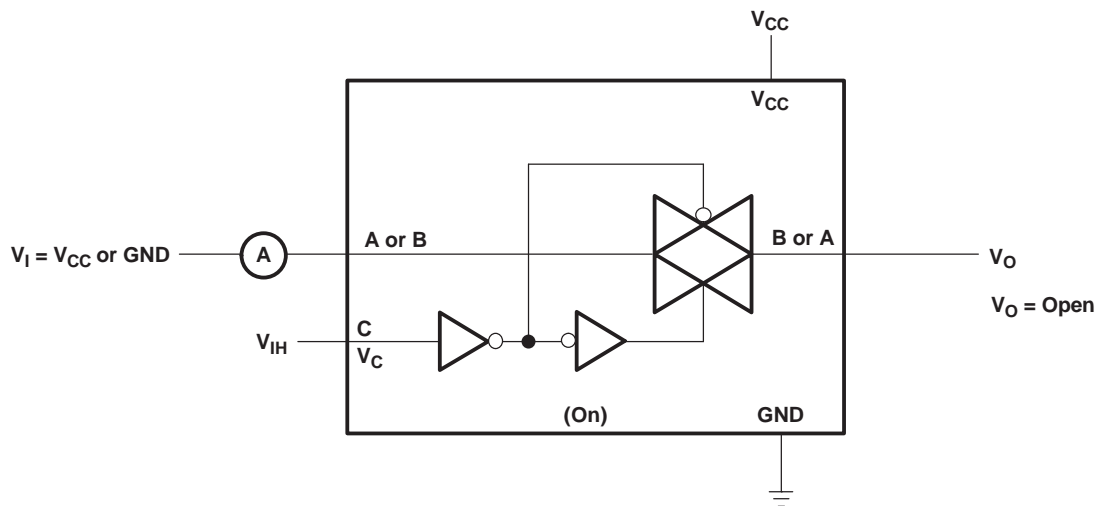
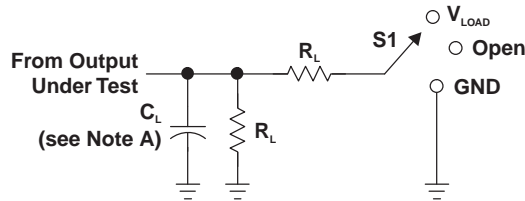


Figure 4. On-State Leakage-Current Test Circuit

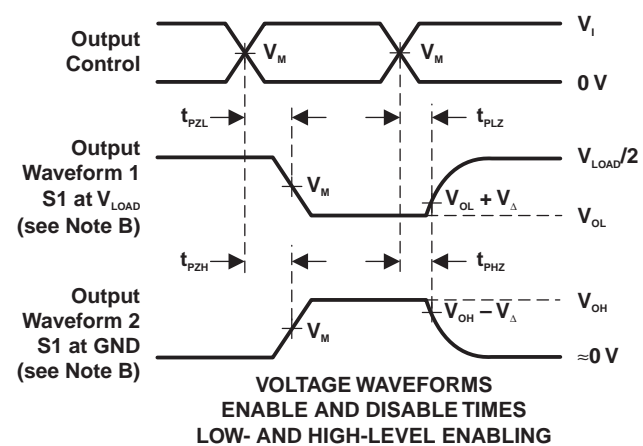
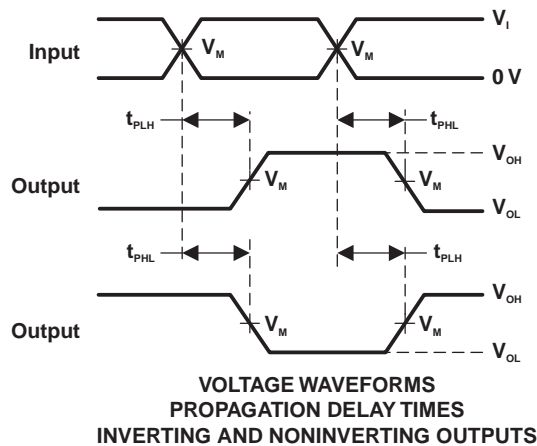
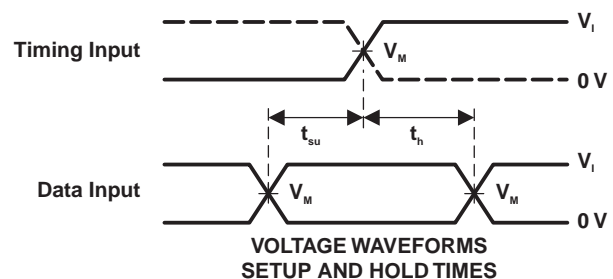
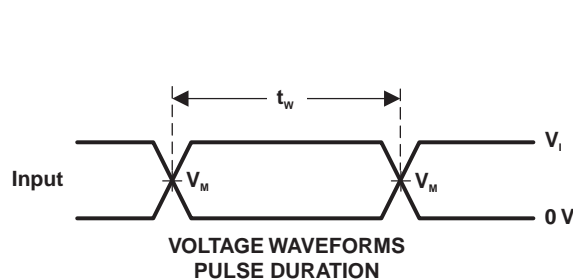
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_f/t_r | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators have the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

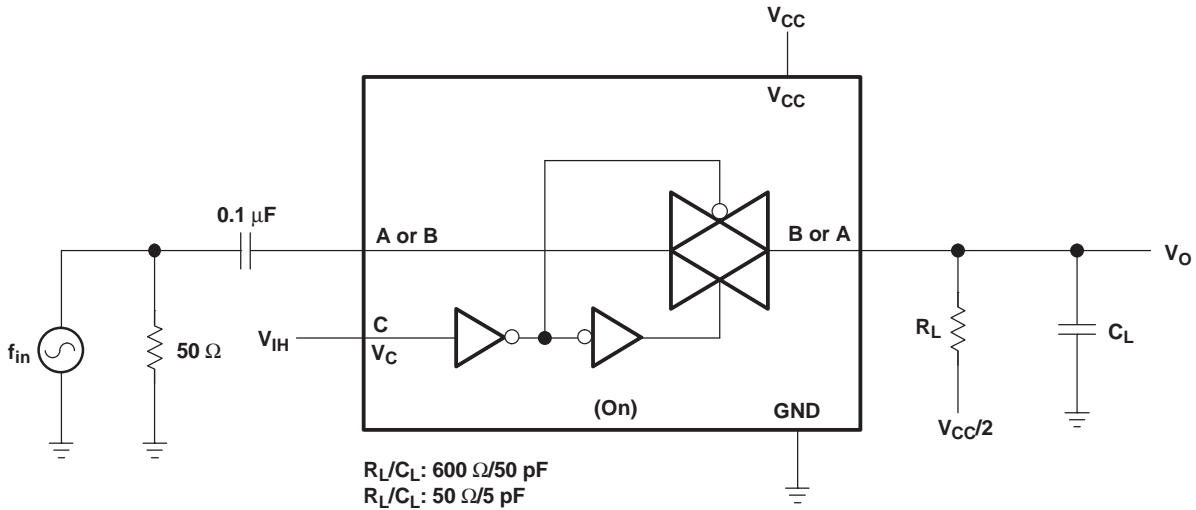


Figure 6. Frequency Response (Switch On)

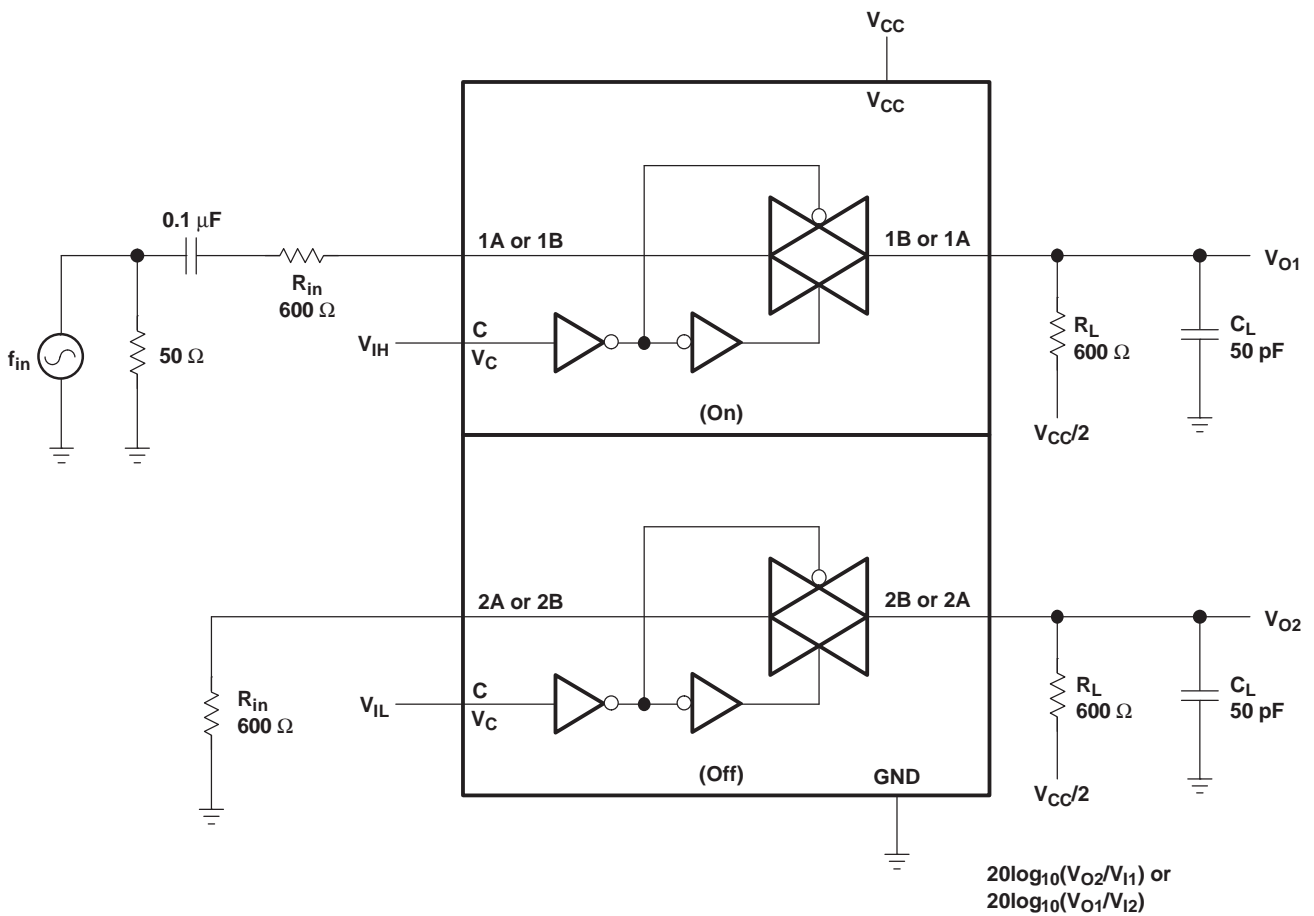


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

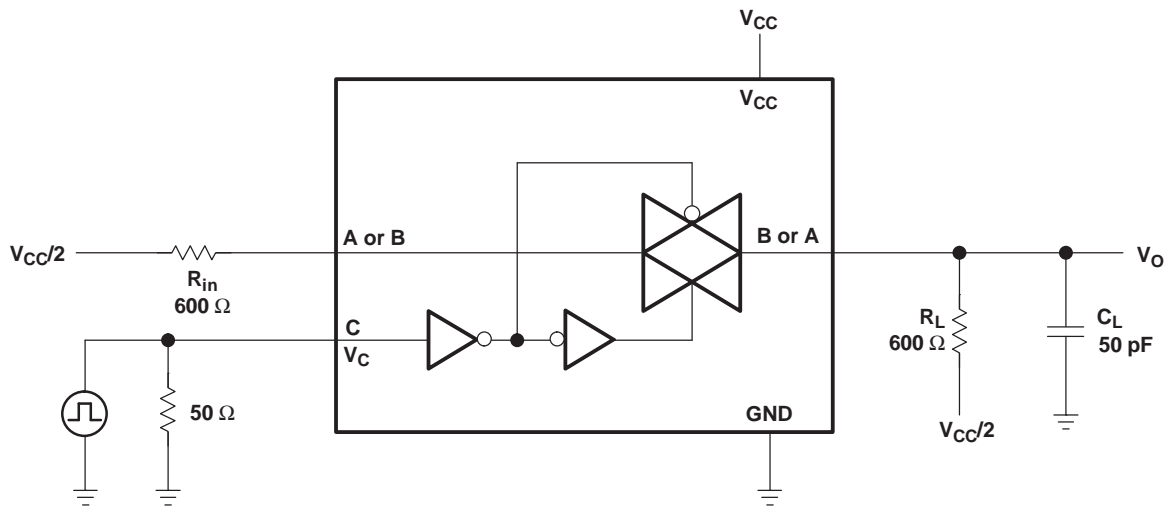


Figure 8. Crosstalk (Control Input, Switch Output)

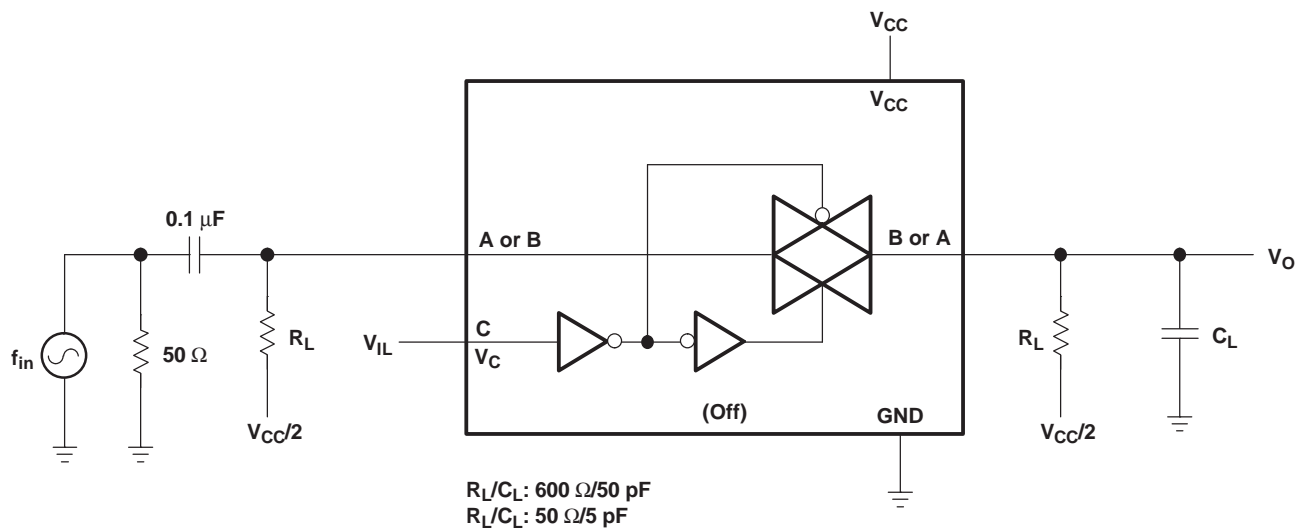


Figure 9. Feedthrough (Switch Off)

PARAMETER MEASUREMENT INFORMATION

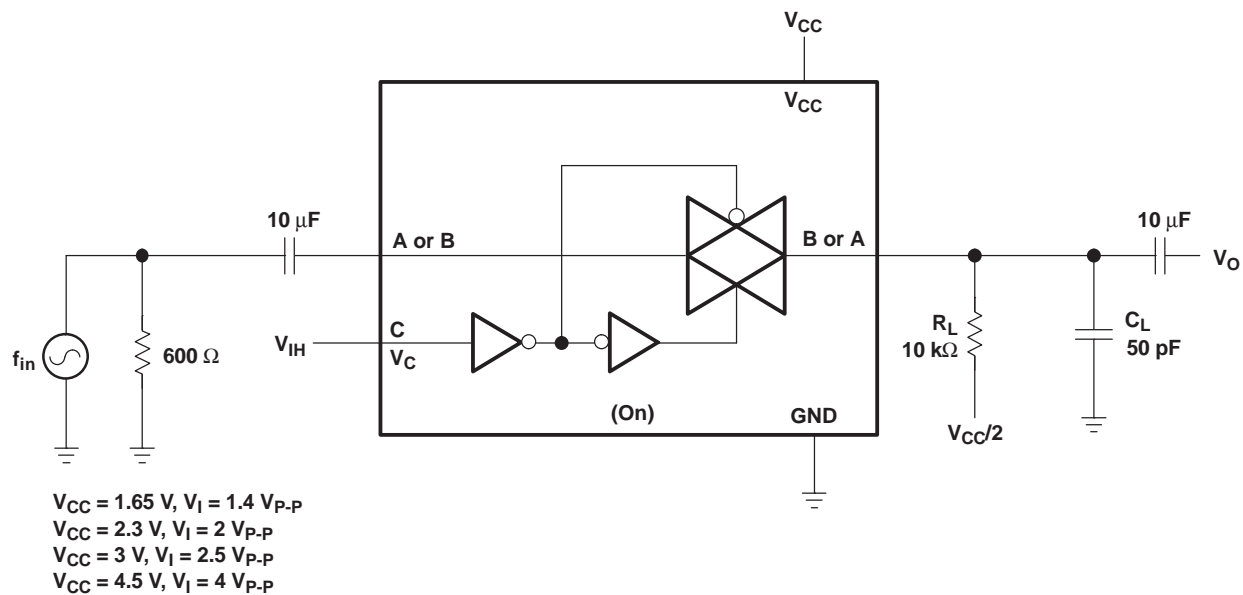


Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LVC2G66DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66 Z | Samples |
| SN74LVC2G66DCTRE4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66 Z | Samples |
| SN74LVC2G66DCTRG4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66 Z | Samples |
| SN74LVC2G66DCUR | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | (66 ~ C66R) CZ | Samples |
| SN74LVC2G66DCURE4 | ACTIVE | US8 | DCU | 8 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| SN74LVC2G66DCURG4 | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66R | Samples |
| SN74LVC2G66DCUT | ACTIVE | US8 | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66R | Samples |
| SN74LVC2G66DCUTE4 | ACTIVE | US8 | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66R | Samples |
| SN74LVC2G66DCUTG4 | ACTIVE | US8 | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C66R | Samples |
| SN74LVC2G66YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (C62 ~ C67 ~ C6N) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G66 :

- Automotive: [SN74LVC2G66-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC2G66DCUR | US8 | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G66DCURG4 | US8 | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC2G66YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

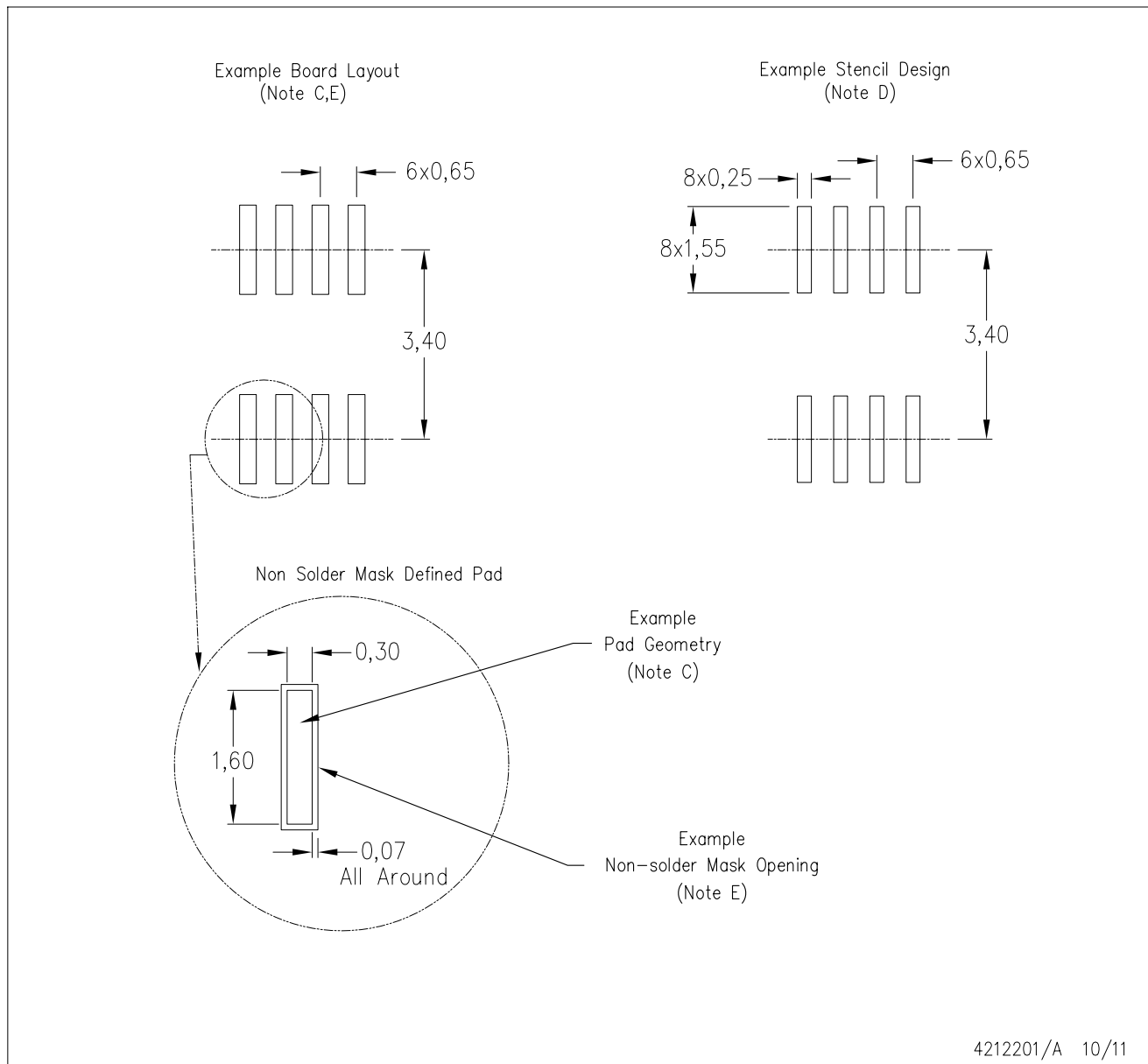
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC2G66DCUR | US8 | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G66DCURG4 | US8 | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC2G66YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

DCT (R-PDSO-G8)

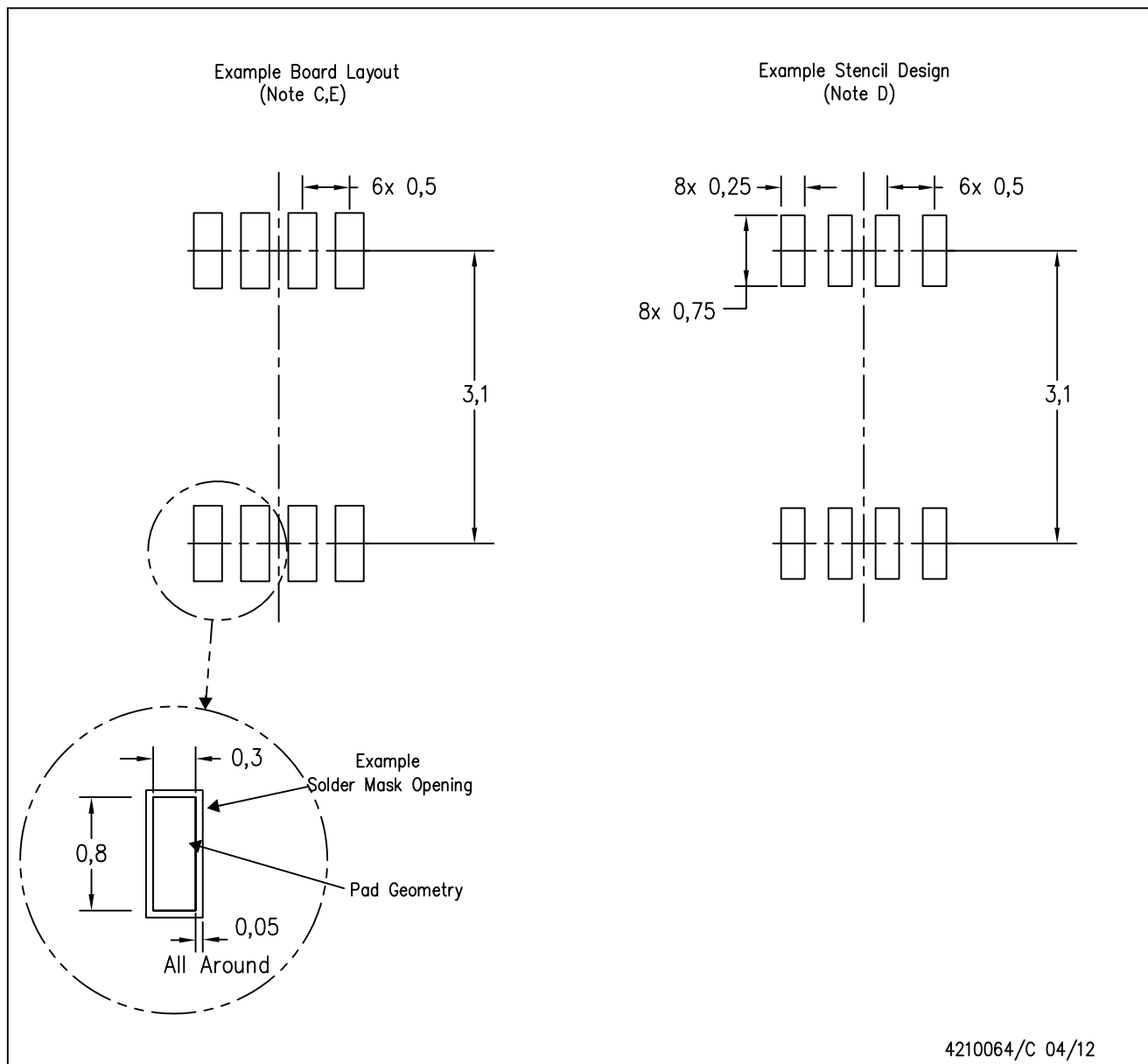
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

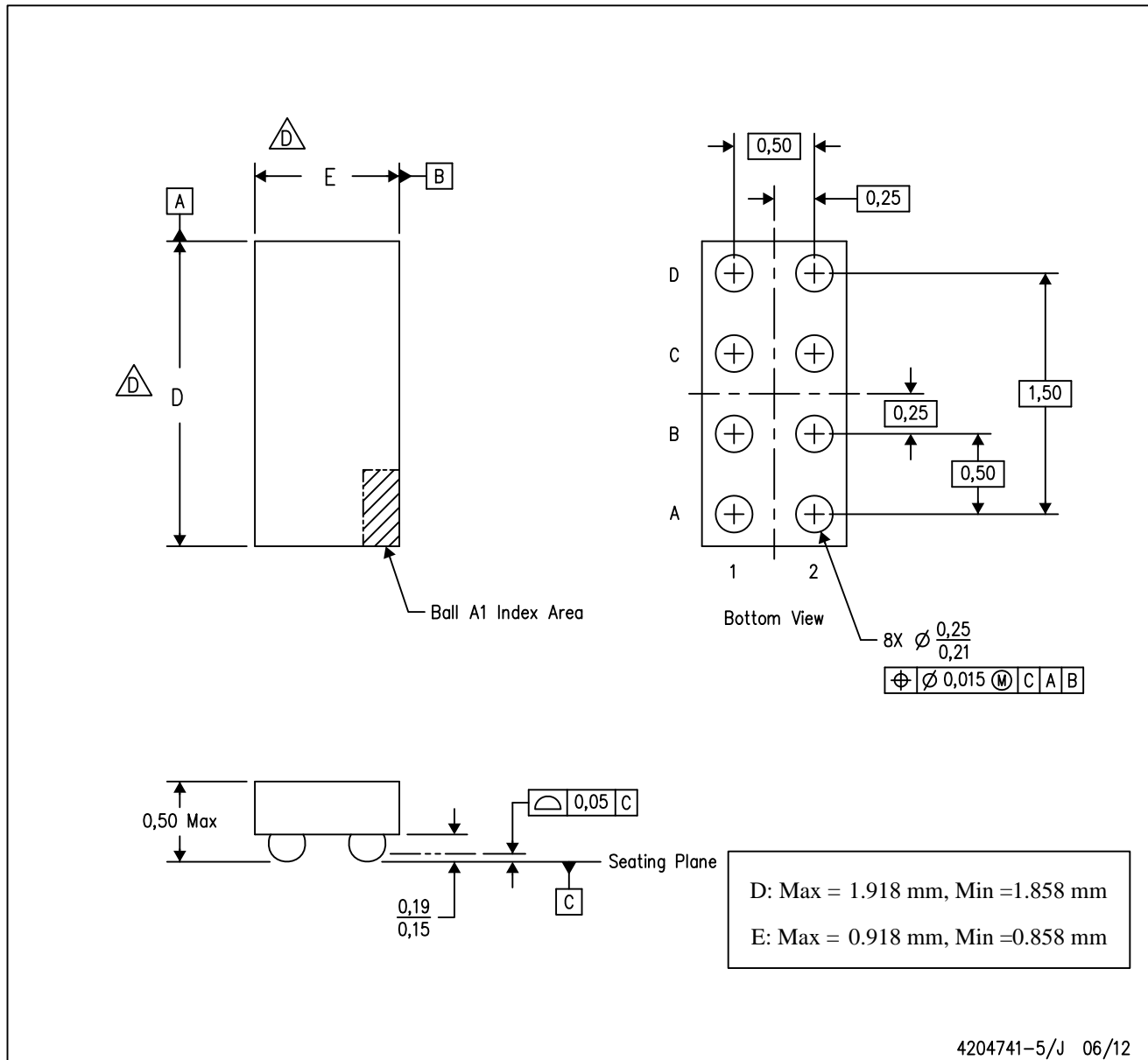


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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - \triangle The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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