# LPC4350/30/20/10

## 32-bit ARM Cortex-M4/M0 flashless MCU; up to 264 kB SRAM; Ethernet; two HS USBs; advanced configurable peripherals

Rev. 4.6 — 14 March 2016 Product data sheet

## 1. General description

The LPC4350/30/20/10 are ARM Cortex-M4 based microcontrollers for embedded applications which include an ARM Cortex-M0 coprocessor, up to 264 kB of SRAM, advanced configurable peripherals such as the State Configurable Timer/PWM (SCTimer/PWM) and the Serial General-Purpose I/O (SGPIO) interface, two high-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals. The LPC4350/30/20/10 operate at CPU frequencies of up to 204 MHz.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core.

The ARM Cortex-M0 coprocessor is an energy-efficient and easy-to-use 32-bit core which is code- and tool-compatible with the Cortex-M4 core. The Cortex-M0 coprocessor offers up to 204 MHz performance with a simple instruction set and reduced code size. In LPC43x0, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

See Section 17 “References” for additional documentation.

## 2. Features and benefits

- Cortex-M4 Processor core
  - ARM Cortex-M4 processor, running at frequencies of up to 204 MHz.
  - Built-in Memory Protection Unit (MPU) supporting eight regions.
  - Built-in Nested Vectored Interrupt Controller (NVIC).
  - Hardware floating-point unit.
  - Non-maskable Interrupt (NMI) input.
  - JTAG and Serial Wire Debug (SWD), serial trace, eight breakpoints, and four watch points.
  - Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
  - System tick timer.

- Cortex-M0 Processor core
  - ARM Cortex-M0 co-processor capable of off-loading the main ARM Cortex-M4 application processor.
  - Running at frequencies of up to 204 MHz.
  - JTAG and built-in NVIC.
- On-chip memory
  - Up to 264 kB SRAM for code and data use.
  - Multiple SRAM blocks with separate bus access. Two SRAM blocks can be powered down individually.
  - 64 kB ROM containing boot code and on-chip software drivers.
  - 64 bit + 256 bit general-purpose One-Time Programmable (OTP) memory.
- Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC (IRC) oscillator trimmed to 1.5 % accuracy over temperature and voltage.
  - Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
  - Clock output.
- Configurable digital peripherals
  - Serial GPIO (SGPIO) interface.
  - State Configurable Timer (SCTimer/PWM) subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like the timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces
  - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY (USB1).
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Up to two C_CAN 2.0B controllers with one channel each. Use of C_CAN controller excludes operation of all other peripherals connected to the same bus bridge. See Figure 1 and Ref. 2.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One SPI controller.


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- One Fast-mode Plus $I^2C$-bus interface with monitor mode and with open-drain I/O pins conforming to the full $I^2C$-bus specification. Supports data rates of up to 1 Mbit/s.
- One standard $I^2C$-bus interface with monitor mode and with standard I/O pins.
- Two $I^2S$ interfaces, each with DMA support and with one input and one output.

- Digital peripherals
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024 H $\times$ 768 V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - Secure Digital Input Output (SD/MMC) card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
  - Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
  - Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control Pulse Width Modulator (PWM) for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer (WWDT).
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Alarm timer; can be battery powered.
- Analog peripherals
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Power
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.


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- Brownout detect with four separate thresholds for interrupt and forced reset.
- Power-On Reset (POR).
- Available as LBGA256, TFBGA180, and TFBGA100 packages and as LQFP144 package.

## 3. Applications

- Motor control
- Power management
- White goods
- RFID readers
- Embedded audio applications
- Industrial automation
- e-metering


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# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC4350FET256 | LBGA256 | Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm | SOT740-2 |
| LPC4350FET180 | TFBGA180 | Thin fine-pitch ball grid array package; 180 balls | SOT570-3 |
| LPC4330FET256 | LBGA256 | Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm | SOT740-2 |
| LPC4330FET180 | TFBGA180 | Thin fine-pitch ball grid array package; 180 balls | SOT570-3 |
| LPC4330FET100 | TFBGA100 | Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm | SOT926-1 |
| LPC4330FBD144 | LQFP144 | Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm | SOT486-1 |
| LPC4320FET100 | TFBGA100 | Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm | SOT926-1 |
| LPC4320FBD144 | LQFP144 | Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm | SOT486-1 |
| LPC4310FET100 | TFBGA100 | Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm | SOT926-1 |
| LPC4310FBD144 | LQFP144 | Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm | SOT486-1 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Total SRAM | LCD | Ethernet | USB0 (Host, Device, OTG) | USB1 (Host, Device)/ ULPI interface | ADC channels | Motor control PWM | QEI | GPIO | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| LPC4350FET256 | 264 kB | yes | yes | yes | yes/yes | 8 | yes | yes | 164 | LBGA256 |
| LPC4350FET180 | 264 kB | yes | yes | yes | yes/yes | 8 | yes | yes | 118 | TFBGA180 |
| LPC4330FET256 | 264 kB | no | yes | yes | yes/yes | 8 | yes | yes | 164 | LBGA256 |
| LPC4330FET180 | 264 kB | no | yes | yes | yes/yes | 8 | yes | yes | 118 | TFBGA180 |
| LPC4330FET100 | 264 kB | no | yes | yes | yes/no | 4 | no | no | 49 | TFBGA100 |
| LPC4330FBD144 | 264 kB | no | yes | yes | yes/no | 8 | yes | no | 83 | LQFP144 |
| LPC4320FET100 | 200 kB | no | no | yes | no | 4 | no | no | 49 | TFBGA100 |
| LPC4320FBD144 | 200 kB | no | no | yes | no | 8 | yes | no | 83 | LQFP144 |
| LPC4310FET100 | 168 kB | no | no | no | no | 4 | no | no | 49 | TFBGA100 |
| LPC4310FBD144 | 168 kB | no | no | no | no | 8 | yes | no | 83 | LQFP144 |


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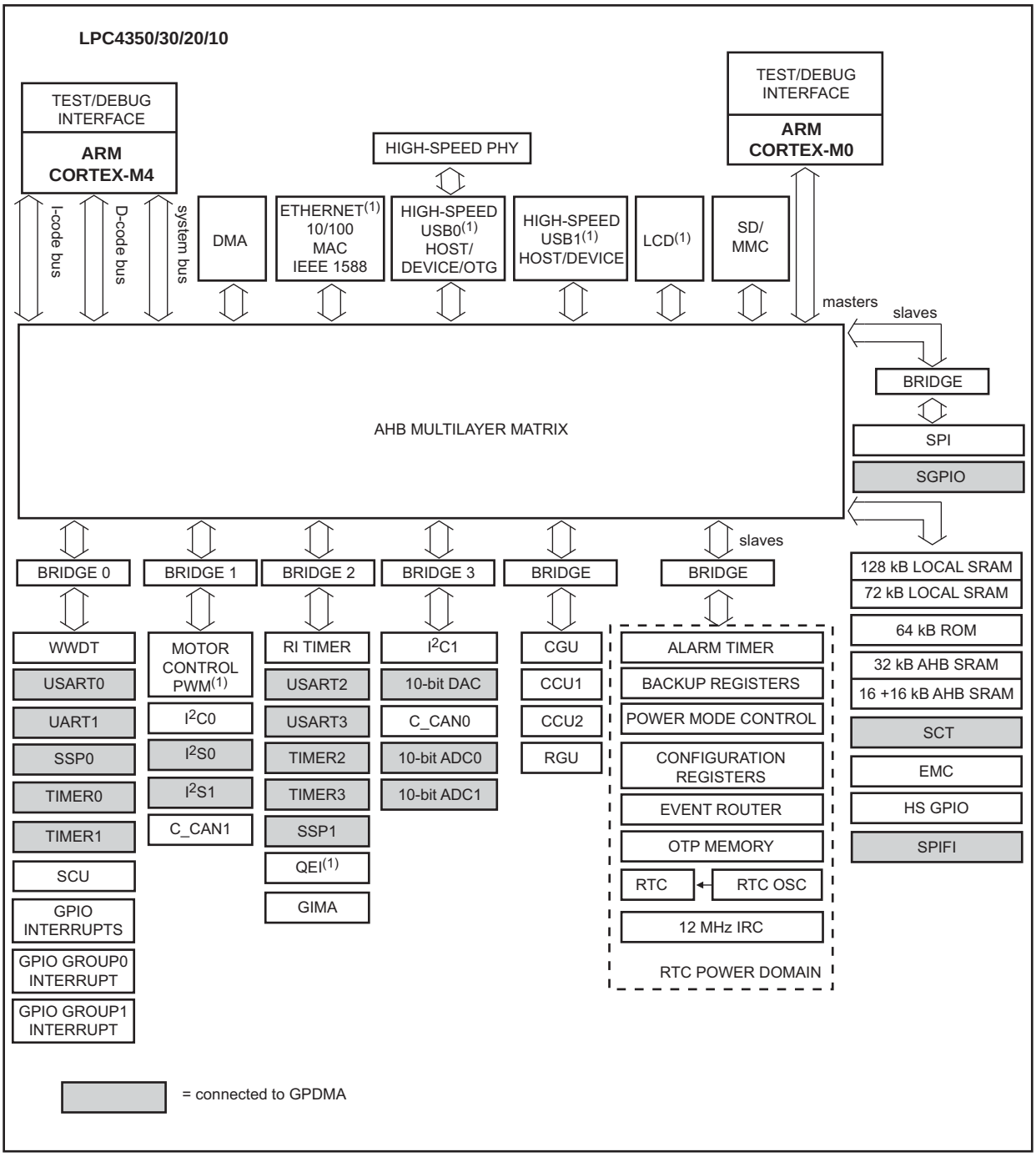
# 5. Block diagram




(1) Not available on all parts (see Table 2).

**Fig 1. LPC4350/30/20/10 Block diagram**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# 6. Pinning information

## 6.1 Pinning

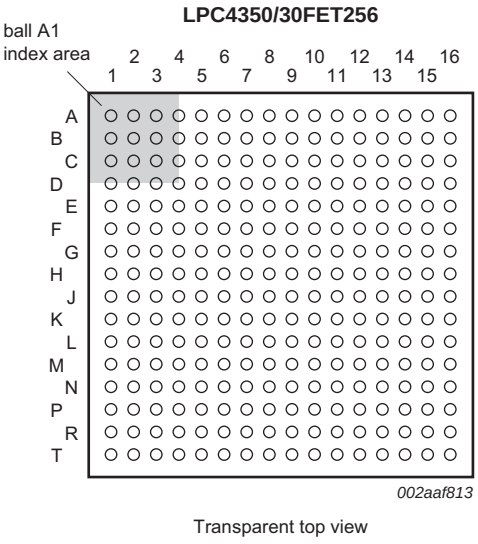


Fig 2. Pin configuration LBGA256 package

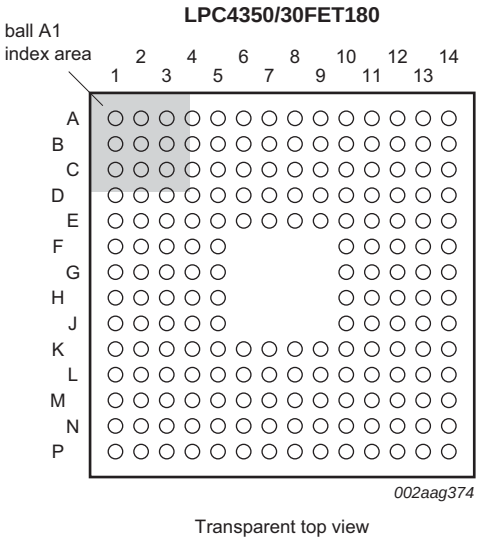


Fig 3. Pin configuration TFBGA180 package

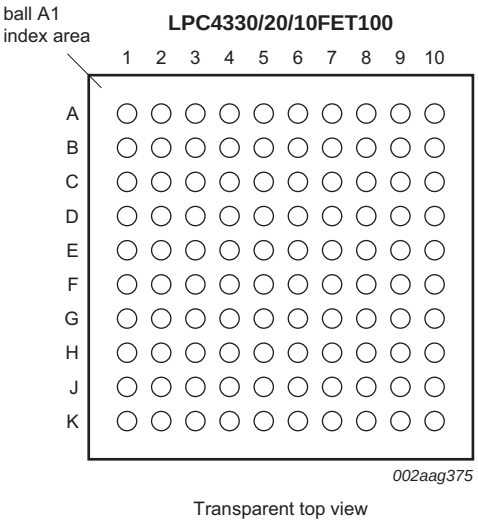


Fig 4. Pin configuration TFBGA100 package

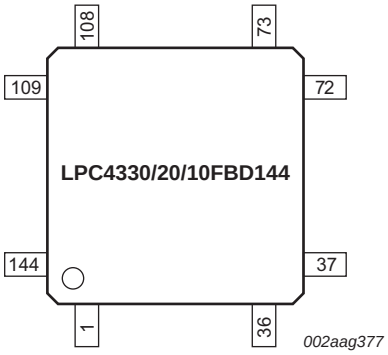


Fig 5. Pin configuration LQFP144 package


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## 6.2 Pin description

On the LPC4350/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.


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**Table 3. Pin description**

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| **Multiplexed digital pins** | | | | | | | | |
| P0_0 | L3 | K3 | G2 | 32 | [2] | N; PU | I/O | **GPIO0[0] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | I | **ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface). |
| | | | | | | | I/O | **SGPIO0 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| | | | | | | | I/O | **I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| P0_1 | M2 | K2 | G1 | 34 | [2] | N; PU | I/O | **GPIO0[1] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave in for SSP1. |
| | | | | | | | I | **ENET_COL —** Ethernet Collision detect (MII interface). |
| | | | | | | | I/O | **SGPIO1 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | | **ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface). |
| | | | | | | | I/O | **I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| P1_0 | P2 | L1 | H1 | 38 | [2] | N; PU | I/O | **GPIO0[4] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1. |
| | | | | | | | I/O | **EMC_A5 —** External memory address line 5. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_1 | R2 | N1 | K2 | 42 | [2] | N; PU | I/O | **GPIO0[8] —** General purpose digital input/output pin. Boot pin (see Table 5). |
| | | | | | | | O | **CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1. |
| | | | | | | | I/O | **EMC_A6 —** External memory address line 6. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P1_2 | R3 | N2 | K1 | 43 | [2] | N; PU | I/O | **GPIO0[9] —** General purpose digital input/output pin. Boot pin (see Table 5). |
| | | | | | | | O | **CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1. |
| | | | | | | | I/O | **EMC_A7 —** External memory address line 7. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P1_3 | P5 | M2 | J1 | 44 | [2] | N; PU | I/O | **GPIO0[10] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC_OE}}$ —** LOW active Output Enable signal. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_RST —** SD/MMC reset signal for MMC4.4 card. |
| P1_4 | T3 | P2 | J2 | 47 | [2] | N; PU | I/O | **GPIO0[11] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3. |
| | | | | | | | I/O | **SGPIO11 —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC_BLS0}}$ —** LOW active Byte Lane select signal 0. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave in for SSP1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_VOLT1 —** SD/MMC bus voltage select output 1. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_5 | R5 | N3 | J4 | 48 | [2] | N; PU | I/O | **GPIO1[8] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **$\overline{\text{EMC_CS0}}$ —** LOW active Chip Select 0 signal. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | I/O | **SGPIO15 —** General purpose digital input/output pin. |
| | | | | | | | O | **SD_POW —** SD/MMC power monitor output. |
| P1_6 | T4 | P3 | K4 | 49 | [2] | N; PU | I/O | **GPIO1[9] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **$\overline{\text{EMC_WE}}$ —** LOW active Write Enable signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO14 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SD_CMD —** SD/MMC command signal. |
| P1_7 | T5 | N4 | G4 | 50 | [2] | N; PU | I/O | **GPIO1[0] —** General purpose digital input/output pin. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART1. |
| | | | | | | | O | **CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D0 —** External memory data line 0. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB_PPWR}}$ used on other NXP LPC parts. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_8 | R7 | M5 | H5 | 51 | [2] | N; PU | I/O | **GPIO1[1] —** General purpose digital input/output pin. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART1. |
| | | | | | | | O | **CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D1 —** External memory data line 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_VOLT0 —** SD/MMC bus voltage select output 0. |
| P1_9 | T7 | N5 | J5 | 52 | [2] | N; PU | I/O | **GPIO1[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **U1_RTS —** Request to Send output for UART1. |
| | | | | | | | O | **CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2. |
| | | | | | | | I/O | **EMC_D2 —** External memory data line 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_DAT0 —** SD/MMC data bus line 0. |
| P1_10 | R8 | N6 | H6 | 53 | [2] | N; PU | I/O | **GPIO1[3] —** General purpose digital input/output pin. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART1. |
| | | | | | | | O | **CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3. |
| | | | | | | | I/O | **EMC_D3 —** External memory data line 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_DAT1 —** SD/MMC data bus line 1. |
| P1_11 | T9 | P8 | J7 | 55 | [2] | N; PU | I/O | **GPIO1[4] —** General purpose digital input/output pin. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART1. |
| | | | | | | | O | **CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D4 —** External memory data line 4. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_DAT2 —** SD/MMC data bus line 2. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_12 | R9 | P7 | K7 | 56 | [2] | N; PU | I/O | **GPIO1[5] —** General purpose digital input/output pin. |
| | | | | | | | I | **U1_DCD —** Data Carrier Detect input for UART1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_D5 —** External memory data line 5. |
| | | | | | | | I | **T0_CAP1 —** Capture input 1 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SD_DAT3 —** SD/MMC data bus line 3. |
| P1_13 | R10 | L8 | H8 | 60 | [2] | N; PU | I/O | **GPIO1[6] —** General purpose digital input/output pin. |
| | | | | | | | O | **U1_TXD —** Transmitter output for UART1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_D6 —** External memory data line 6. |
| | | | | | | | I | **T0_CAP0 —** Capture input 0 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | I | **SD_CD —** SD/MMC card detect input. |
| P1_14 | R11 | K7 | J8 | 61 | [2] | N; PU | I/O | **GPIO1[7] —** General purpose digital input/output pin. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_D7 —** External memory data line 7. |
| | | | | | | | O | **T0_MAT2 —** Match output 2 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| P1_15 | T12 | P11 | K8 | 62 | [2] | N; PU | I/O | **GPIO0[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **U2_TXD —** Transmitter output for USART2. |
| | | | | | | | I/O | **SGPIO2 —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface). |
| | | | | | | | O | **T0_MAT1 —** Match output 1 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_16 | M7 | L5 | H9 | 64 | [2] | N; PU | I/O | **GPIO0[3] —** General purpose digital input/output pin. |
| | | | | | | | I | **U2_RXD —** Receiver input for USART2. |
| | | | | | | | I/O | **SGPIO3 —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_CRS —** Ethernet Carrier Sense (MII interface). |
| | | | | | | | O | **T0_MAT0 —** Match output 0 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface). |
| P1_17 | M8 | L6 | H10 | 66 | [3] | N; PU | I/O | **GPIO0[12] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **U2_UCLK —** Serial clock input/output for USART2 in synchronous mode. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **ENET_MDIO —** Ethernet MIIM data input and output. |
| | | | | | | | I | **T0_CAP3 —** Capture input 3 of timer 0. |
| | | | | | | | O | **CAN1_TD —** CAN1 transmitter output. |
| | | | | | | | I/O | **SGPIO11 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| P1_18 | N12 | N10 | J10 | 67 | [2] | N; PU | I/O | **GPIO0[13] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface). |
| | | | | | | | O | **T0_MAT3 —** Match output 3 of timer 0. |
| | | | | | | | I | **CAN1_RD —** CAN1 receiver input. |
| | | | | | | | I/O | **SGPIO12 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| P1_19 | M11 | N9 | K9 | 68 | [2] | N; PU | I | **ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface). |
| | | | | | | | I/O | **SSP1_SCK —** Serial clock for SSP1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CLKOUT —** Clock output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S0_RX_MCLK —** I2S receive master clock. |
| | | | | | | | I/O | **I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P1_20 | M10 | J10 | K10 | 70 | [2] | N; PU | I/O | **GPIO0[15] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface). |
| | | | | | | | I | **T0_CAP2 —** Capture input 2 of timer 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| P2_0 | T16 | N14 | G10 | 75 | [2] | N; PU | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| | | | | | | | O | **U0_TXD —** Transmitter output for USART0. |
| | | | | | | | I/O | **EMC_A13 —** External memory address line 13. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts. |
| | | | | | | | I/O | **GPIO5[0] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP0 —** Capture input 0 of timer 3. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| P2_1 | N15 | M13 | G7 | 81 | [2] | N; PU | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| | | | | | | | I | **U0_RXD —** Receiver input for USART0. |
| | | | | | | | I/O | **EMC_A12 —** External memory address line 12. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | I/O | **GPIO5[1] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP1 —** Capture input 1 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P2_2 | M15 | L13 | F5 | 84 | [2] | N; PU | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **U0_UCLK —** Serial clock input/output for USART0 in synchronous mode. |
| | | | | | | | I/O | **EMC_A11 —** External memory address line 11. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | I/O | **GPIO5[2] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | I | **T3_CAP2 —** Capture input 2 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| P2_3 | J12 | G11 | D8 | 87 | [3] | N; PU | I/O | **SGPIO12 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2C1_SDA —** $I^2C1$ data input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. |
| | | | | | | | I | **CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2. |
| | | | | | | | I/O | **GPIO5[3] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT0 —** Match output 0 of timer 3. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts. |
| P2_4 | K11 | L9 | D9 | 88 | [3] | N; PU | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2C1_SCL —** $I^2C1$ clock input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| | | | | | | | I | **CTIN_0 —** SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3. |
| | | | | | | | I/O | **GPIO5[4] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT1 —** Match output 1 of timer 3. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P2_5 | K14 | J12 | D10 | 91 | [3] | N; PU | I/O | **SGPIO14 —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0. |
| | | | | | | | I | **USB1_VBUS —** Monitors the presence of USB1 bus power.<br>**Note:** This signal must be HIGH for USB reset to occur. |
| | | | | | | | I | **ADCTRIG1 —** ADC trigger input 1. |
| | | | | | | | I/O | **GPIO5[5] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT2 —** Match output 2 of timer 3. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| P2_6 | K16 | J14 | G9 | 95 | [2] | N; PU | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0. |
| | | | | | | | I/O | **EMC_A10 —** External memory address line 10. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| | | | | | | | I/O | **GPIO5[6] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_7 —** SCTimer/PWM input 7. |
| | | | | | | | I | **T3_CAP3 —** Capture input 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| P2_7 | H14 | G12 | C10 | 96 | [2] | N; PU | I/O | **GPIO0[7] —** General purpose digital input/output pin. If this pin is pulled LOW at reset, the part enters ISP mode using USART0. |
| | | | | | | | O | **CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3. |
| | | | | | | | I/O | **U3_UCLK —** Serial clock input/output for USART3 in synchronous mode. |
| | | | | | | | I/O | **EMC_A9 —** External memory address line 9. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT3 —** Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P2_8 | J16 | H14 | C6 | 98 | [2] | N; PU | I/O | **SGPIO15 —** General purpose digital input/output pin. Boot pin (see Table 5). |
| | | | | | | | O | **CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0. |
| | | | | | | | I/O | **U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3. |
| | | | | | | | I/O | **EMC_A8 —** External memory address line 8. |
| | | | | | | | I/O | **GPIO5[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P2_9 | H16 | G14 | B10 | 102 | [2] | N; PU | I/O | **GPIO1[10] —** General purpose digital input/output pin. Boot pin (see Table 5. |
| | | | | | | | O | **CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0. |
| | | | | | | | I/O | **U3_BAUD —** Baud pin for USART3. |
| | | | | | | | I/O | **EMC_A0 —** External memory address line 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P2_10 | G16 | F14 | E8 | 104 | [2] | N; PU | I/O | **GPIO0[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0. |
| | | | | | | | O | **U2_TXD —** Transmitter output for USART2. |
| | | | | | | | I/O | **EMC_A1 —** External memory address line 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P2_11 | F16 | E13 | A9 | 105 | [2] | N; PU | I/O | **GPIO1[11] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3. |
| | | | | | | | I | **U2_RXD —** Receiver input for USART2. |
| | | | | | | | I/O | **EMC_A2 —** External memory address line 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P2_12 | E15 | D13 | B9 | 106 | [2] | N; PU | I/O | **GPIO1[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A3 —** External memory address line 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **U2_UCLK —** Serial clock input/output for USART2 in synchronous mode. |
| P2_13 | C16 | E14 | A10 | 108 | [2] | N; PU | I/O | **GPIO1[13] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A4 —** External memory address line 4. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2. |
| P3_0 | F13 | D12 | A8 | 112 | [2] | N; PU | I/O | **I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | | | | | | O | **I2S0_RX_MCLK —** I2S receive master clock. |
| | | | | | | | I/O | **I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |
| | | | | | | | O | **I2S0_TX_MCLK —** I2S transmit master clock. |
| | | | | | | | I/O | **SSP0_SCK —** Serial clock for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P3_1 | G11 | D10 | F7 | 114 | [2] | N; PU | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| | | | | | | | I/O | **I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| | | | | | | | I | **CAN0_RD —** CAN receiver input. |
| | | | | | | | O | **USB1_IND1 —** USB1 Port indicator LED control output 1. |
| | | | | | | | I/O | **GPIO5[8] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD15 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| P3_2 | F11 | D9 | G6 | 116 | [2] | OL; PU | I/O | **I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| | | | | | | | I/O | **I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| | | | | | | | O | **CAN0_TD —** CAN transmitter output. |
| | | | | | | | O | **USB1_IND0 —** USB1 Port indicator LED control output 0. |
| | | | | | | | I/O | **GPIO5[9] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD14 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| P3_3 | B14 | B13 | A7 | 118 | [4] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **SPI_SCK —** Serial clock for SPI. |
| | | | | | | | I/O | **SSP0_SCK —** Serial clock for SSP0. |
| | | | | | | | O | **SPIFI_SCK —** Serial clock for SPIFI. |
| | | | | | | | O | **CGU_OUT1 —** CGU spare clock output 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S0_TX_MCLK —** I2S transmit master clock. |
| | | | | | | | I/O | **I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P3_4 | A15 | C14 | B8 | 119 | [2] | N; PU | I/O | **GPIO1[14] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SPIFI_SIO3 —** I/O lane 3 for SPIFI. |
| | | | | | | | O | **U1_TXD —** Transmitter output for UART 1. |
| | | | | | | | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| | | | | | | | I/O | **I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| | | | | | | | O | **LCD_VD13 —** LCD data. |
| P3_5 | C12 | C11 | B7 | 121 | [2] | N; PU | I/O | **GPIO1[15] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SPIFI_SIO2 —** I/O lane 2 for SPIFI. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART 1. |
| | | | | | | | I/O | **I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| | | | | | | | I/O | **I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| | | | | | | | O | **LCD_VD12 —** LCD data. |
| P3_6 | B13 | B12 | C7 | 122 | [2] | N; PU | I/O | **GPIO0[6] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SPI_MISO —** Master In Slave Out for SPI. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |
| | | | | | | | I/O | **SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P3_7 | C11 | C10 | D7 | 123 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **SPI_MOSI —** Master Out Slave In for SPI. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | | I/O | **SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0. |
| | | | | | | | I/O | **GPIO5[10] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P3_8 | C10 | C9 | E7 | 124 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **SPI_SSEL —** Slave Select for SPI. Note that this pin in an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | I/O | **SPIFI_CS —** SPIFI serial flash chip select. |
| | | | | | | | I/O | **GPIO5[11] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P4_0 | D5 | D4 | - | 1 | [2] | N; PU | I/O | **GPIO2[0] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOA0 —** Motor control PWM channel 0, output A. |
| | | | | | | | I | **NMI —** External interrupt input to NMI. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD13 —** LCD data. |
| | | | | | | | I/O | **U3_UCLK —** Serial clock input/output for USART3 in synchronous mode. |
| | | | | | | | - | **R —** Function reserved. |
| P4_1 | A1 | D3 | - | 3 | [5] | N; PU | I/O | **GPIO2[1] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3. |
| | | | | | | | O | **LCD_VD0 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. |
| | | | | | | | I | **ENET_COL —** Ethernet Collision detect (MII interface). |
| | | | | | | | AI | **ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P4_2 | D3 | A2 | - | 8 | [2] | N; PU | I/O | **GPIO2[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0. |
| | | | | | | | O | **LCD_VD3 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD12 —** LCD data. |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| P4_3 | C2 | B2 | - | 7 | [5] | N; PU | I/O | **GPIO2[3] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0. |
| | | | | | | | O | **LCD_VD2 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD21 —** LCD data. |
| | | | | | | | I/O | **U3_BAUD —** Baud pin for USART3. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | AI | **ADC0_0 —** DAC output; ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| P4_4 | B1 | A1 | - | 9 | [5] | N; PU | I/O | **GPIO2[4] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0. |
| | | | | | | | O | **LCD_VD1 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD20 —** LCD data. |
| | | | | | | | I/O | **U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| | | | | | | | O | **DAC —** DAC output. Shared between 10-bit ADC0/1 and DAC.. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P4_5 | D2 | C2 | - | 10 | [2] | N; PU | I/O | **GPIO2[5] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3. |
| | | | | | | | O | **LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO11 —** General purpose digital input/output pin. |
| P4_6 | C1 | B1 | - | 11 | [2] | N; PU | I/O | **GPIO2[6] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3. |
| | | | | | | | O | **LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO12 —** General purpose digital input/output pin. |
| P4_7 | H4 | F4 | - | 14 | [2] | O; PU | O | **LCD_DCLK —** LCD panel clock. |
| | | | | | | | I | **GP_CLKIN —** General-purpose clock input to the CGU. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |
| | | | | | | | I/O | **I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |
| P4_8 | E2 | D2 | - | 15 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2. |
| | | | | | | | O | **LCD_VD9 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD22 —** LCD data. |
| | | | | | | | O | **CAN1_TD —** CAN1 transmitter output. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P4_9 | L2 | J2 | - | 33 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | O | **LCD_VD11 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[13] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD15 —** LCD data. |
| | | | | | | | I | **CAN1_RD —** CAN1 receiver input. |
| | | | | | | | I/O | **SGPIO14 —** General purpose digital input/output pin. |
| P4_10 | M3 | L3 | - | 35 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0. |
| | | | | | | | O | **LCD_VD10 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **LCD_VD14 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO15 —** General purpose digital input/output pin. |
| P5_0 | N3 | L2 | - | 37 | [2] | N; PU | I/O | **GPIO2[9] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOB2 —** Motor control PWM channel 2, output B. |
| | | | | | | | I/O | **EMC_D12 —** External memory data line 12. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART 1. |
| | | | | | | | I | **T1_CAP0 —** Capture input 0 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_1 | P3 | M1 | - | 39 | [2] | N; PU | I/O | **GPIO2[10] —** General purpose digital input/output pin. |
| | | | | | | | I | **MCI2 —** Motor control PWM channel 2, input. |
| | | | | | | | I/O | **EMC_D13 —** External memory data line 13. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1. |
| | | | | | | | I | **T1_CAP1 —** Capture input 1 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P5_2 | R4 | M3 | - | 46 | [2] | N; PU | I/O | **GPIO2[11] —** General purpose digital input/output pin. |
| | | | | | | | I | **MCI1 —** Motor control PWM channel 1, input. |
| | | | | | | | I/O | **EMC_D14 —** External memory data line 14. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1. |
| | | | | | | | I | **T1_CAP2 —** Capture input 2 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_3 | T8 | P6 | - | 54 | [2] | N; PU | I/O | **GPIO2[12] —** General purpose digital input/output pin. |
| | | | | | | | I | **MCI0 —** Motor control PWM channel 0, input. |
| | | | | | | | I/O | **EMC_D15 —** External memory data line 15. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART 1. |
| | | | | | | | I | **T1_CAP3 —** Capture input 3 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_4 | P9 | N7 | - | 57 | [2] | N; PU | I/O | **GPIO2[13] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOB0 —** Motor control PWM channel 0, output B. |
| | | | | | | | I/O | **EMC_D8 —** External memory data line 8. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART 1. |
| | | | | | | | O | **T1_MAT0 —** Match output 0 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_5 | P10 | N8 | - | 58 | [2] | N; PU | I/O | **GPIO2[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOA1 —** Motor control PWM channel 1, output A. |
| | | | | | | | I/O | **EMC_D9 —** External memory data line 9. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_DCD —** Data Carrier Detect input for UART 1. |
| | | | | | | | O | **T1_MAT1 —** Match output 1 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P5_6 | T13 | M11 | - | 63 | [2] | N; PU | I/O | **GPIO2[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOB1 —** Motor control PWM channel 1, output B. |
| | | | | | | | I/O | **EMC_D10 —** External memory data line 10. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_TXD —** Transmitter output for UART 1. |
| | | | | | | | O | **T1_MAT2 —** Match output 2 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P5_7 | R12 | N11 | - | 65 | [2] | N; PU | I/O | **GPIO2[7] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOA2 —** Motor control PWM channel 2, output A. |
| | | | | | | | I/O | **EMC_D11 —** External memory data line 11. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART 1. |
| | | | | | | | O | **T1_MAT3 —** Match output 3 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_0 | M12 | M10 | H7 | 73 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **I2S0_RX_MCLK —** I2S receive master clock. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_1 | R15 | P14 | G5 | 74 | [2] | N; PU | I/O | **GPIO3[0] —** General purpose digital input/output pin. |
| | | | | | | | O | **EMC_DYCS1 —** SDRAM chip select 1. |
| | | | | | | | I/O | **U0_UCLK —** Serial clock input/output for USART0 in synchronous mode. |
| | | | | | | | I/O | **I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP0 —** Capture input 2 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P6_2 | L13 | K11 | J9 | 78 | [2] | N; PU | I/O | **GPIO3[1] —** General purpose digital input/output pin. |
| | | | | | | | O | **EMC_CKEOUT1 —** SDRAM clock enable 1. |
| | | | | | | | I/O | **U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0. |
| | | | | | | | I/O | **I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP1 —** Capture input 1 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_3 | P15 | N13 | - | 79 | [2] | N; PU | I/O | **GPIO3[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB_PPWR}}$ used on other NXP LPC parts. |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC_CS1}}$ —** LOW active Chip Select 1 signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP2 —** Capture input 2 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_4 | R16 | M14 | F6 | 80 | [2] | N; PU | I/O | **GPIO3[3] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | O | **U0_TXD —** Transmitter output for USART0. |
| | | | | | | | O | **$\overline{\text{EMC_CAS}}$ —** LOW active SDRAM Column Address Strobe. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P6_5 | P16 | L14 | F9 | 82 | [2] | N; PU | I/O | **GPIO3[4] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1. |
| | | | | | | | I | **U0_RXD —** Receiver input for USART0. |
| | | | | | | | O | **$\overline{\text{EMC_RAS}}$ —** LOW active SDRAM Row Address Strobe. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_6 | L14 | K12 | - | 83 | [2] | N; PU | I/O | **GPIO0[5] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC_BLS1}}$ —** LOW active Byte Lane select signal 1. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP3 —** Capture input 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_7 | J13 | H11 | - | 85 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A15 —** External memory address line 15. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | I/O | **GPIO5[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **T2_MAT0 —** Match output 0 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_8 | H13 | F12 | - | 86 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A14 —** External memory address line 14. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| | | | | | | | I/O | **GPIO5[16] —** General purpose digital input/output pin. |
| | | | | | | | O | **T2_MAT1 —** Match output 1 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P6_9 | J15 | H13 | F8 | 97 | [2] | N; PU | I/O | **GPIO3[5] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_DYCS0 —** SDRAM chip select 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T2_MAT2 —** Match output 2 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_10 | H15 | G13 | - | 100 | [2] | N; PU | I/O | **GPIO3[6] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCABORT —** Motor control PWM, LOW-active fast abort. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_DQMOUT1 —** Data mask 1 used with SDRAM and static devices. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_11 | H12 | F11 | C9 | 101 | [2] | N; PU | I/O | **GPIO3[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_CKEOUT0 —** SDRAM clock enable 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T2_MAT3 —** Match output 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| P6_12 | G15 | F13 | - | 103 | [2] | N; PU | I/O | **GPIO2[8] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P7_0 | B16 | B14 | - | 110 | [2] | N; PU | I/O | **GPIO3[8] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_LE —** Line end signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| P7_1 | C14 | C13 | - | 113 | [2] | N; PU | I/O | **GPIO3[9] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3. |
| | | | | | | | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | O | **LCD_VD7 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U2_TXD —** Transmitter output for USART2. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| P7_2 | A16 | A14 | - | 115 | [2] | N; PU | I/O | **GPIO3[10] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1. |
| | | | | | | | I/O | **I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | | | | | O | **LCD_VD18 —** LCD data. |
| | | | | | | | O | **LCD_VD6 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U2_RXD —** Receiver input for USART2. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| P7_3 | C13 | C12 | - | 117 | [2] | N; PU | I/O | **GPIO3[11] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD17 —** LCD data. |
| | | | | | | | O | **LCD_VD5 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P7_4 | C8 | C6 | - | 132 | [5] | N; PU | I/O | **GPIO3[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD16 —** LCD data. |
| | | | | | | | O | **LCD_VD4 —** LCD data. |
| | | | | | | | O | **TRACEDATA[0] —** Trace data, bit 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| P7_5 | A7 | A7 | - | 133 | [5] | N; PU | I/O | **GPIO3[13] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD8 —** LCD data. |
| | | | | | | | O | **LCD_VD23 —** LCD data. |
| | | | | | | | O | **TRACEDATA[1] —** Trace data, bit 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| P7_6 | C7 | F5 | - | 134 | [2] | N; PU | I/O | **GPIO3[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **TRACEDATA[2] —** Trace data, bit 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P7_7 | B6 | D5 | - | 140 | [5] | N; PU | I/O | **GPIO3[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_PWR —** LCD panel power enable. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **TRACEDATA[3] —** Trace data, bit 3. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | AI | **ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| P8_0 | E5 | E4 | - | - | [3] | N; PU | I/O | **GPIO4[0] —** General purpose digital input/output pin. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **MCI2 —** Motor control PWM channel 2, input. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT0 —** Match output 0 of timer 0. |
| P8_1 | H5 | G4 | - | - | [3] | N; PU | I/O | **GPIO4[1] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **MCI1 —** Motor control PWM channel 1, input. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT1 —** Match output 1 of timer 0. |
| P8_2 | K4 | J4 | - | - | [3] | N; PU | I/O | **GPIO4[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **MCI0 —** Motor control PWM channel 0, input. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT2 —** Match output 2 of timer 0. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P8_3 | J3 | H3 | - | - | [2] | N; PU | I/O | **GPIO4[3] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D2 —** ULPI link bidirectional data line 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD12 —** LCD data. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT3 —** Match output 3 of timer 0. |
| P8_4 | J2 | H2 | - | - | [2] | N; PU | I/O | **GPIO4[4] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D1 —** ULPI link bidirectional data line 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD7 —** LCD data. |
| | | | | | | | O | **LCD_VD16 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP0 —** Capture input 0 of timer 0. |
| P8_5 | J1 | H1 | - | - | [2] | N; PU | I/O | **GPIO4[5] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D0 —** ULPI link bidirectional data line 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD6 —** LCD data. |
| | | | | | | | O | **LCD_VD8 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP1 —** Capture input 1 of timer 0. |
| P8_6 | K3 | J3 | - | - | [2] | N; PU | I/O | **GPIO4[6] —** General purpose digital input/output pin. |
| | | | | | | | I | **USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD5 —** LCD data. |
| | | | | | | | O | **LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP2 —** Capture input 2 of timer 0. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P8_7 | K1 | J1 | - | - | [2] | N; PU | I/O | **GPIO4[7] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD4 —** LCD data. |
| | | | | | | | O | **LCD_PWR —** LCD panel power enable. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP3 —** Capture input 3 of timer 0. |
| P8_8 | L1 | K1 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CGU_OUT0 —** CGU spare clock output 0. |
| | | | | | | | O | **I2S1_TX_MCLK —** I2S1 transmit master clock. |
| P9_0 | T1 | P1 | - | - | [2] | N; PU | I/O | **GPIO4[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCABORT —** Motor control PWM, LOW-active fast abort. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_CRS —** Ethernet Carrier Sense (MII interface). |
| | | | | | | | I/O | **SGPIO0 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |
| P9_1 | N6 | P4 | - | - | [2] | N; PU | I/O | **GPIO4[13] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOA2 —** Motor control PWM channel 2, output A. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | I | **ENET_RX_ER —** Ethernet receive error (MII interface). |
| | | | | | | | I/O | **SGPIO1 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P9_2 | N8 | M6 | - | - | [2] | N; PU | I/O | **GPIO4[14] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOB2 —** Motor control PWM channel 2, output B. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| | | | | | | | I | **ENET_RXD3 —** Ethernet receive data 3 (MII interface). |
| | | | | | | | I/O | **SGPIO2 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| P9_3 | M6 | P5 | - | - | [2] | N; PU | I/O | **GPIO4[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOA0 —** Motor control PWM channel 0, output A. |
| | | | | | | | O | **USB1_IND1 —** USB1 Port indicator LED control output 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RXD2 —** Ethernet receive data 2 (MII interface). |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. |
| P9_4 | N10 | M8 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **MCOB0 —** Motor control PWM channel 0, output B. |
| | | | | | | | O | **USB1_IND0 —** USB1 Port indicator LED control output 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[17] —** General purpose digital input/output pin. |
| | | | | | | | O | **ENET_TXD2 —** Ethernet transmit data 2 (MII interface). |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| P9_5 | M9 | L7 | - | 69 | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **MCOA1 —** Motor control PWM channel 1, output A. |
| | | | | | | | O | **USB1_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active high).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB_PPWR}}$ used on other NXP LPC parts. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[18] —** General purpose digital input/output pin. |
| | | | | | | | O | **ENET_TXD3 —** Ethernet transmit data 3 (MII interface). |
| | | | | | | | I/O | **SGPIO3 —** General purpose digital input/output pin. |
| | | | | | | | O | **U0_TXD —** Transmitter output for USART0. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P9_6 | L11 | M9 | - | 72 | [2] | N; PU | I/O | **GPIO4[11] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOB1 —** Motor control PWM channel 1, output B. |
| | | | | | | | I | **USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_COL —** Ethernet Collision detect (MII interface). |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| | | | | | | | I | **U0_RXD —** Receiver input for USART0. |
| PA_0 | L12 | L10 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S1_RX_MCLK —** I2S1 receive master clock. |
| | | | | | | | O | **CGU_OUT1 —** CGU spare clock output 1. |
| | | | | | | | - | **R —** Function reserved. |
| PA_1 | J14 | H12 | - | - | [3] | N; PU | I/O | **GPIO4[8] —** General purpose digital input/output pin. |
| | | | | | | | I | **QEI_IDX —** Quadrature Encoder Interface INDEX input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U2_TXD —** Transmitter output for USART2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PA_2 | K15 | J13 | - | - | [3] | N; PU | I/O | **GPIO4[9] —** General purpose digital input/output pin. |
| | | | | | | | I | **QEI_PHB —** Quadrature Encoder Interface PHB input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U2_RXD —** Receiver input for USART2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PA_3 | H11 | E10 | - | - | [3] | N; PU | I/O | **GPIO4[10] —** General purpose digital input/output pin. |
| | | | | | | | I | **QEI_PHA —** Quadrature Encoder Interface PHA input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PA_4 | G13 | E12 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A23 —** External memory address line 23. |
| | | | | | | | I/O | **GPIO5[19] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PB_0 | B15 | D14 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3. |
| | | | | | | | O | **LCD_VD23 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[20] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PB_1 | A14 | A13 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULP data line direction. |
| | | | | | | | O | **LCD_VD22 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[21] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PB_2 | B12 | B11 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D7 —** ULPI link bidirectional data line 7. |
| | | | | | | | O | **LCD_VD21 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[22] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PB_3 | A13 | A12 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D6 —** ULPI link bidirectional data line 6. |
| | | | | | | | O | **LCD_VD20 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[23] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PB_4 | B11 | B10 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D5 —** ULPI link bidirectional data line 5. |
| | | | | | | | O | **LCD_VD15 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[24] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PB_5 | A12 | A11 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D4 —** ULPI link bidirectional data line 4. |
| | | | | | | | O | **LCD_VD14 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[25] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_7 —** SCTimer/PWM input 7. |
| | | | | | | | O | **LCD_PWR —** LCD panel power enable. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PB_6 | A6 | C5 | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D3 —** ULPI link bidirectional data line 3. |
| | | | | | | | O | **LCD_VD13 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO5[26] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_6 —** ADC0 and ADC1, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PC_0 | D4 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **ENET_RX_CLK —** Ethernet Receive Clock (MII interface). |
| | | | | | | | O | **LCD_DCLK —** LCD panel clock. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_CLK —** SD/MMC card clock. |
| | | | | | | | AI | **ADC1_1 —** ADC1 and ADC0, input channel 1. Configure the pin as input (USB_ULPI_CLK) and use the ADC function select register in the SCU to select the ADC. |
| PC_1 | E4 | - | - | - | [2] | N; PU | I/O | **USB1_ULPI_D7 —** ULPI link bidirectional data line 7. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART 1. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| | | | | | | | I/O | **GPIO6[0] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP0 —** Capture input 0 of timer 3. |
| | | | | | | | O | **SD_VOLT0 —** SD/MMC bus voltage select output 0. |
| PC_2 | F6 | - | - | - | [2] | N; PU | I/O | **USB1_ULPI_D6 —** ULPI link bidirectional data line 6. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART 1. |
| | | | | | | | O | **ENET_TXD2 —** Ethernet transmit data 2 (MII interface). |
| | | | | | | | I/O | **GPIO6[1] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_RST —** SD/MMC reset signal for MMC4.4 card. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PC_3 | F5 | - | - | - | [5] | N; PU | I/O | **USB1_ULPI_D5 —** ULPI link bidirectional data line 5. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1. |
| | | | | | | | O | **ENET_TXD3 —** Ethernet transmit data 3 (MII interface). |
| | | | | | | | I/O | **GPIO6[2] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_VOLT1 —** SD/MMC bus voltage select output 1. |
| | | | | | | | AI | **ADC1_0 —** DAC output; ADC1 and ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PC_4 | F4 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D4 —** ULPI link bidirectional data line 4. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | | **ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface). |
| | | | | | | | I/O | **GPIO6[3] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP1 —** Capture input 1 of timer 3. |
| | | | | | | | I/O | **SD_DAT0 —** SD/MMC data bus line 0. |
| PC_5 | G4 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D3 —** ULPI link bidirectional data line 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **ENET_TX_ER —** Ethernet Transmit Error (MII interface). |
| | | | | | | | I/O | **GPIO6[4] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP2 —** Capture input 2 of timer 3. |
| | | | | | | | I/O | **SD_DAT1 —** SD/MMC data bus line 1. |
| PC_6 | H6 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D2 —** ULPI link bidirectional data line 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RXD2 —** Ethernet receive data 2 (MII interface). |
| | | | | | | | I/O | **GPIO6[5] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP3 —** Capture input 3 of timer 3. |
| | | | | | | | I/O | **SD_DAT2 —** SD/MMC data bus line 2. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PC_7 | G5 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D1 —** ULPI link bidirectional data line 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RXD3 —** Ethernet receive data 3 (MII interface). |
| | | | | | | | I/O | **GPIO6[6] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT0 —** Match output 0 of timer 3. |
| | | | | | | | I/O | **SD_DAT3 —** SD/MMC data bus line 3. |
| PC_8 | N4 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D0 —** ULPI link bidirectional data line 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface). |
| | | | | | | | I/O | **GPIO6[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT1 —** Match output 1 of timer 3. |
| | | | | | | | I | **SD_CD —** SD/MMC card detect input. |
| PC_9 | K2 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RX_ER —** Ethernet receive error (MII interface). |
| | | | | | | | I/O | **GPIO6[8] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT2 —** Match output 2 of timer 3. |
| | | | | | | | O | **SD_POW —** SD/MMC power monitor output. |
| PC_10 | M5 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[9] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT3 —** Match output 3 of timer 3. |
| | | | | | | | I/O | **SD_CMD —** SD/MMC command signal. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PC_11 | L5 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction. |
| | | | | | | | I | **U1_DCD —** Data Carrier Detect input for UART 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[10] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_DAT4 —** SD/MMC data bus line 4. |
| PC_12 | L6 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[11] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SGPIO11 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | | | | | I/O | **SD_DAT5 —** SD/MMC data bus line 5. |
| PC_13 | M1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **U1_TXD —** Transmitter output for UART 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[12] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SGPIO12 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | I/O | **SD_DAT6 —** SD/MMC data bus line 6. |
| PC_14 | N1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[13] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| | | | | | | | O | **ENET_TX_ER —** Ethernet Transmit Error (MII interface). |
| | | | | | | | I/O | **SD_DAT7 —** SD/MMC data bus line 7. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_0 | N2 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3. |
| | | | | | | | O | **EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[14] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| PD_1 | P1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_CKEOUT2 —** SDRAM clock enable 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **SD_POW —** SD/MMC power monitor output. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| PD_2 | R1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1. |
| | | | | | | | I/O | **EMC_D16 —** External memory data line 16. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[16] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| PD_3 | P4 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_6 —** SCTimer/PWM output 7. Match output 2 of timer 1. |
| | | | | | | | I/O | **EMC_D17 —** External memory data line 17. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[17] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_4 | T2 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2. |
| | | | | | | | I/O | **EMC_D18 —** External memory data line 18. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[18] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| PD_5 | P6 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D19 —** External memory data line 19. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[19] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| PD_6 | R6 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D20 —** External memory data line 20. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[20] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| PD_7 | T6 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2. |
| | | | | | | | I/O | **EMC_D21 —** External memory data line 21. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[21] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO11 —** General purpose digital input/output pin. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_8 | P8 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3. |
| | | | | | | | I/O | **EMC_D22 —** External memory data line 22. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[22] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO12 —** General purpose digital input/output pin. |
| PD_9 | T11 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3. |
| | | | | | | | I/O | **EMC_D23 —** External memory data line 23. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[23] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| PD_10 | P11 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2. |
| | | | | | | | O | **$\overline{\text{EMC_BLS3}}$ —** LOW active Byte Lane select signal 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[24] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PD_11 | N9 | M7 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **$\overline{\text{EMC_CS3}}$ —** LOW active Chip Select 3 signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[25] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D0 —** ULPI link bidirectional data line 0. |
| | | | | | | | O | **CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_12 | N11 | P9 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **$\overline{\text{EMC_CS2}}$ —** LOW active Chip Select 2 signal. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[26] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| PD_13 | T14 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_0 —** SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3. |
| | | | | | | | O | **$\overline{\text{EMC_BLS2}}$ —** LOW active Byte Lane select signal 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[27] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| PD_14 | R13 | L11 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **$\overline{\text{EMC_DYCS2}}$ —** SDRAM chip select 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[28] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |
| PD_15 | T15 | P13 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A17 —** External memory address line 17. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[29] —** General purpose digital input/output pin. |
| | | | | | | | I | **SD_WP —** SD/MMC card write protect input. |
| | | | | | | | O | **CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PD_16 | R14 | P12 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A16 —** External memory address line 16. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[30] —** General purpose digital input/output pin. |
| | | | | | | | O | **SD_VOLT2 —** SD/MMC bus voltage select output 2. |
| | | | | | | | O | **CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| PE_0 | P14 | N12 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A18 —** External memory address line 18. |
| | | | | | | | I/O | **GPIO7[0] —** General purpose digital input/output pin. |
| | | | | | | | O | **CAN1_TD —** CAN1 transmitter output. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_1 | N14 | M12 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A19 —** External memory address line 19. |
| | | | | | | | I/O | **GPIO7[1] —** General purpose digital input/output pin. |
| | | | | | | | I | **CAN1_RD —** CAN1 receiver input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_2 | M14 | L12 | - | - | [2] | N; PU | I | **ADCTRIG0 —** ADC trigger input 0. |
| | | | | | | | I | **CAN0_RD —** CAN receiver input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A20 —** External memory address line 20. |
| | | | | | | | I/O | **GPIO7[2] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PE_3 | K12 | K10 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CAN0_TD —** CAN transmitter output. |
| | | | | | | | I | **ADCTRIG1 —** ADC trigger input 1. |
| | | | | | | | I/O | **EMC_A21 —** External memory address line 21. |
| | | | | | | | I/O | **GPIO7[3] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_4 | K13 | J11 | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **NMI —** External interrupt input to NMI. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **EMC_A22 —** External memory address line 22. |
| | | | | | | | I/O | **GPIO7[4] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_5 | N16 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0. |
| | | | | | | | O | **U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1. |
| | | | | | | | I/O | **EMC_D24 —** External memory data line 24. |
| | | | | | | | I/O | **GPIO7[5] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_6 | M16 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART 1. |
| | | | | | | | I/O | **EMC_D25 —** External memory data line 25. |
| | | | | | | | I/O | **GPIO7[6] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PE_7 | F15 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART1. |
| | | | | | | | I/O | **EMC_D26 —** External memory data line 26. |
| | | | | | | | I/O | **GPIO7[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_8 | F14 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART 1. |
| | | | | | | | I/O | **EMC_D27 —** External memory data line 27. |
| | | | | | | | I/O | **GPIO7[8] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_9 | E16 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1. |
| | | | | | | | I | **U1_DCD —** Data Carrier Detect input for UART 1. |
| | | | | | | | I/O | **EMC_D28 —** External memory data line 28. |
| | | | | | | | I/O | **GPIO7[9] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_10 | E14 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1. |
| | | | | | | | I/O | **EMC_D29 —** External memory data line 29. |
| | | | | | | | I/O | **GPIO7[10] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PE_11 | D16 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3. |
| | | | | | | | O | **U1_TXD —** Transmitter output for UART 1. |
| | | | | | | | I/O | **EMC_D30 —** External memory data line 30. |
| | | | | | | | I/O | **GPIO7[11] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_12 | D15 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART 1. |
| | | | | | | | I/O | **EMC_D31 —** External memory data line 31. |
| | | | | | | | I/O | **GPIO7[12] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_13 | G14 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3. |
| | | | | | | | I/O | **I2C1_SDA —** $I^2C1$ data input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | O | **EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices. |
| | | | | | | | I/O | **GPIO7[13] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_14 | C15 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_DYCS3 —** SDRAM chip select 3. |
| | | | | | | | I/O | **GPIO7[14] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PE_15 | E13 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0. |
| | | | | | | | I/O | **I2C1_SCL —** $I^2C1$ clock input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | O | **EMC_CKEOUT3 —** SDRAM clock enable 3. |
| | | | | | | | I/O | **GPIO7[15] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PF_0 | D12 | - | - | - | [2] | O; PU | I/O | **SSP0_SCK —** Serial clock for SSP0. |
| | | | | | | | I | **GP_CLKIN —** General-purpose clock input to the CGU. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S1_TX_MCLK —** I2S1 transmit master clock. |
| PF_1 | E11 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[16] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO0 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| PF_2 | D11 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. |
| | | | | | | | I/O | **SSP0_MISO —** Master In Slave Out for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[17] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO1 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_3 | E10 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| | | | | | | | I/O | **SSP0_MOSI —** Master Out Slave in for SSP0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[18] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO2 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| PF_4 | D10 | D6 | H4 | 120 | [2] | O; PU | I/O | **SSP1_SCK —** Serial clock for SSP1. |
| | | | | | | | I | **GP_CLKIN —** General-purpose clock input to the CGU. |
| | | | | | | | O | **TRACECLK —** Trace clock. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S0_TX_MCLK —** I2S transmit master clock. |
| | | | | | | | I/O | **I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| PF_5 | E9 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_UCLK —** Serial clock input/output for USART3 in synchronous mode. |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | O | **TRACEDATA[0] —** Trace data, bit 0. |
| | | | | | | | I/O | **GPIO7[19] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC1_4 —** ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_6 | E7 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | O | **TRACEDATA[1] —** Trace data, bit 1. |
| | | | | | | | I/O | **GPIO7[20] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | | | | | AI | **ADC1_3 —** ADC1 and ADC0, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_7 | B7 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_BAUD —** Baud pin for USART3. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave in for SSP1. |
| | | | | | | | O | **TRACEDATA[2] —** Trace data, bit 2. |
| | | | | | | | I/O | **GPIO7[21] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | AI/O | **ADC1_7 —** ADC1 and ADC0, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_8 | E6 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U0_UCLK —** Serial clock input/output for USART0 in synchronous mode. |
| | | | | | | | I | **CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0. |
| | | | | | | | O | **TRACEDATA[3] —** Trace data, bit 3. |
| | | | | | | | I/O | **GPIO7[22] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_2 —** ADC0 and ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |


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**Table 3. Pin description** *...continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_9 | D6 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0. |
| | | | | | | | O | **CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[23] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO3 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_10 | A3 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **U0_TXD —** Transmitter output for USART0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[24] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **SD_WP —** SD/MMC card write protect input. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_11 | A2 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **U0_RXD —** Receiver input for USART0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO7[25] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **SD_VOLT2 —** SD/MMC bus voltage select output 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| **Clock pins** | | | | | | | | |
| CLK0 | N5 | M4 | K3 | 45 | [4] | O; PU | O | **EMC_CLK0 —** SDRAM clock 0. |
| | | | | | | | O | **CLKOUT —** Clock output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_CLK —** SD/MMC card clock. |
| | | | | | | | O | **EMC_CLK01 —** SDRAM clock 0 and clock 1 combined. |
| | | | | | | | I/O | **SSP1_SCK —** Serial clock for SSP1. |
| | | | | | | | I | **ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface). |
| CLK1 | T10 | - | - | - | [4] | O; PU | O | **EMC_CLK1 —** SDRAM clock 1. |
| | | | | | | | O | **CLKOUT —** Clock output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CGU_OUT0 —** CGU spare clock output 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **I2S1_TX_MCLK —** I2S1 transmit master clock. |
| CLK2 | D14 | P10 | K6 | 99 | [4] | O; PU | O | **EMC_CLK3 —** SDRAM clock 3. |
| | | | | | | | O | **CLKOUT —** Clock output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SD_CLK —** SD/MMC card clock. |
| | | | | | | | O | **EMC_CLK23 —** SDRAM clock 2 and clock 3 combined. |
| | | | | | | | O | **I2S0_TX_MCLK —** I2S transmit master clock. |
| | | | | | | | I/O | **I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |
| CLK3 | P12 | - | - | - | [4] | O; PU | O | **EMC_CLK2 —** SDRAM clock 2. |
| | | | | | | | O | **CLKOUT —** Clock output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CGU_OUT1 —** CGU spare clock output 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the $I^2S$-bus specification. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| **Debug pins** | | | | | | | | |
| DBGEN | L4 | K4 | A6 | 28 | [2] | I; PU | I | JTAG interface control signal. Also used for boundary scan. To use the part in functional mode, connect this pin in one of the following ways:<br>• Leave DBGEN open. The DBGEN pin is pulled up internally by a 50 kΩ resistor.<br>• Tie DBGEN to VDDIO.<br>• Pull DBGEN up to VDDIO with an external pull-up resistor. |
| TCK/SWDCLK | J5 | G5 | H2 | 27 | [2] | I; F | I | Test Clock for JTAG interface (default) or Serial Wire (SW) clock. |
| $\overline{\text{TRST}}$ | M4 | L4 | B4 | 29 | [2] | I; PU | I | Test Reset for JTAG interface. |
| TMS/SWDIO | K6 | K5 | C4 | 30 | [2] | I; PU | I | Test Mode Select for JTAG interface (default) or SW debug data input/output. |
| TDO/SWO | K5 | J5 | H3 | 31 | [2] | O | O | Test Data Out for JTAG interface (default) or SW trace output. |
| TDI | J4 | H4 | G3 | 26 | [2] | I; PU | I | Test Data In for JTAG interface. |
| **USB0 pins** | | | | | | | | |
| USB0_DP | F2 | E2 | E1 | 18 | [6] | - | I/O | USB0 bidirectional D+ line. |
| USB0_DM | G2 | F2 | E2 | 20 | [6] | - | I/O | USB0 bidirectional D− line. |
| USB0_VBUS | F1 | E1 | E3 | 21 | [6] [7] | - | I/O | VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 64 kΩ (typical) ± 16 kΩ. |
| USB0_ID | H2 | G2 | F1 | 22 | [8] | - | I | Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For OTG this pin has an internal pull-up resistor. |
| USB0_RREF | H1 | G1 | F3 | 24 | [8] | - | | 12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference. |
| **USB1 pins** | | | | | | | | |
| USB1_DP | F12 | D11 | E9 | 89 | [9] | - | I/O | USB1 bidirectional D+ line. |
| USB1_DM | G12 | E11 | E10 | 90 | [9] | - | I/O | USB1 bidirectional D− line. |
| **$I^2C$-bus pins** | | | | | | | | |
| I2C0_SCL | L15 | K13 | D6 | 92 | [10] | I; F | I/O | $I^2C$ clock input/output. Open-drain output (for $I^2C$-bus compliance). |
| I2C0_SDA | L16 | K14 | E6 | 93 | [10] | I; F | I/O | $I^2C$ data input/output. Open-drain output (for $I^2C$-bus compliance). |
| **Reset and wake-up pins** | | | | | | | | |
| $\overline{\text{RESET}}$ | D9 | C7 | B6 | 128 | [11] | I; IA | I | External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin does not have an internal pull-up. |
| WAKEUP0 | A9 | A9 | A4 | 130 | [11] | I; IA | I | External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| WAKEUP1 | A10 | C8 | - | - | [11] | I; IA | I | External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up. |
| WAKEUP2 | C9 | E5 | - | - | [11] | I; IA | I | External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up. |
| WAKEUP3 | D8 | - | - | - | [11] | I; IA | I | External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up. |
| **ADC pins** | | | | | | | | |
| ADC0_0/ ADC1_0/DAC | E3 | B6 | A2 | 6 | [8] | I; IA | I | ADC input channel 0. Shared between 10-bit ADC0/1 and DAC. |
| ADC0_1/ ADC1_1 | C3 | C4 | A1 | 2 | [8] | I; IA | I | ADC input channel 1. Shared between 10-bit ADC0/1. |
| ADC0_2/ ADC1_2 | A4 | B3 | B3 | 143 | [8] | I; IA | I | ADC input channel 2. Shared between 10-bit ADC0/1. |
| ADC0_3/ ADC1_3 | B5 | B4 | A3 | 139 | [8] | I; IA | I | ADC input channel 3. Shared between 10-bit ADC0/1. |
| ADC0_4/ ADC1_4 | C6 | A5 | - | 138 | [8] | I; IA | I | ADC input channel 4. Shared between 10-bit ADC0/1. |
| ADC0_5/ ADC1_5 | B3 | C3 | - | 144 | [8] | I; IA | I | ADC input channel 5. Shared between 10-bit ADC0/1. |
| ADC0_6/ ADC1_6 | A5 | A4 | - | 142 | [8] | I; IA | I | ADC input channel 6. Shared between 10-bit ADC0/1. |
| ADC0_7/ ADC1_7 | C5 | B5 | - | 136 | [8] | I; IA | I | ADC input channel 7. Shared between 10-bit ADC0/1. |
| **RTC** | | | | | | | | |
| RTC_ALARM | A11 | A10 | C3 | 129 | [11] | O | O | RTC controlled output. This pin has an internal pull-up. The reset state of this pin is LOW after POR. For all other types of reset, the reset state depends on the state of the RTC alarm interrupt. |
| RTCX1 | A8 | A8 | A5 | 125 | [8] | - | I | Input to the RTC 32 kHz ultra-low power oscillator circuit. |
| RTCX2 | B8 | B7 | B5 | 126 | [8] | - | O | Output from the RTC 32 kHz ultra-low power oscillator circuit. |
| **Crystal oscillator pins** | | | | | | | | |
| XTAL1 | D1 | C1 | B1 | 12 | [8] | - | I | Input to the oscillator circuit and internal clock generator circuits. |
| XTAL2 | E1 | D1 | C1 | 13 | [8] | - | O | Output from the oscillator amplifier. |
| **Power and ground pins** | | | | | | | | |
| USB0_VDDA 3V3_DRIVER | F3 | E3 | D1 | 16 | | - | - | Separate analog 3.3 V power supply for driver. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| USB0 _VDDA3V3 | G3 | F3 | D2 | 17 | | - | - | USB 3.3 V separate power supply voltage. |
| USB0_VSSA _TERM | H3 | G3 | D3 | 19 | | - | - | Dedicated analog ground for clean reference for termination resistors. |
| USB0_VSSA _REF | G1 | F1 | F2 | 23 | | - | - | Dedicated clean analog ground for generation of reference currents and voltages. |
| VDDA | B4 | A6 | B2 | 137 | | - | - | Analog power supply and ADC reference voltage. |
| VBAT | B10 | B9 | C5 | 127 | | - | - | RTC power supply: 3.3 V on this pin supplies power to the RTC. |
| VDDREG | F10, F9, L8, L7 | D8, E8 | E4, E5, F4 | 94, 131, 59, 25 | | | - | Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages. |
| VPP | E8 | - | - | - | [12] | - | - | OTP programming voltage. |
| VDDIO | D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13 | H5, H10, K8, G10 | F10, K5 | 5, 36, 41, 71, 77, 107, 111, 141 | [12] | - | - | I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages. |
| VDD | - | - | - | - | | | | Power supply for main regulator, I/O, and OTP. |
| VSS | G9, H7, J10, J11, K8 | F10, D7, E6, E7, E9, K6, K9 | - | - | [13] [14] | - | - | Ground. |


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**Table 3. Pin description** *…continued*

*LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.*

| Symbol | LBGA256 | TFBGA180 | TFBGA100 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| VSSIO | C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13 | - | C8, D4, D5, G8, J3, J6 | 4, 40, 76, 109 | [13] [14] | - | - | Ground. |
| VSSA | B2 | A3 | C2 | 135 | | - | - | Analog ground. |
| **Not connected** | | | | | | | | |
| - | B9 | B8 | - | - | | - | - | n.c. |

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input; OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels, and hysteresis; high drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides high-speed digital I/O functions with TTL levels and hysteresis.

[5] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V). When configured as an ADC input or DAC output, the pin is not 5 V tolerant and the digital section of the pad must be disabled by setting the pin to an input function and disabling the pull-up resistor through the pin's SFSP register.

[6] 5 V tolerant transparent analog pad.

[7] For maximum load $C_L$ = 6.5 µF and maximum pull-down resistance $R_{pd}$ = 80 kΩ, the VBUS signal takes about 2 s to fall from VBUS = 5 V to VBUS = 0.2 V when it is no longer driven.

[8] Transparent analog pad. Not 5 V tolerant.

[9] Pad provides USB functions 5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only).

[10] Open-drain 5 V tolerant digital I/O pad, compatible with I2C-bus Fast Mode Plus specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I2C-bus is floating and does not disturb the I2C lines.

[11] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output and hysteresis.

[12] VPP is internally connected to VDDIO for all packages with the exception of the LBGA256 package.

[13] On the LQFP144 package, VSSIO and VSS are connected to a common ground plane.

[14] On the TFBGA100 package, VSS is internally connected to VSSIO.


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# 7. Functional description

## 7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-CODE bus, and the D-code bus. The I-CODE and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC4350/30/20/10 use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

An ARM Cortex-M0 co-processor is included in the LPC4350/30/20/10, capable of off-loading the main ARM Cortex-M4 application processor. Most peripheral interrupts are connected to both processors. The processors communicate with each other via an interprocessor communication protocol.

## 7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core. The processor includes an NVIC with up to 53 interrupts.

## 7.3 ARM Cortex-M0 co-processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low-power consumption. The ARM Cortex-M0 co-processor uses a 3-stage pipeline von-Neumann architecture and a small but powerful instruction set providing high-end processing hardware. In LPC43x0, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier. The co-processor incorporates an NVIC with 32 interrupts.

## 7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.


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## 7.5 AHB multilayer matrix

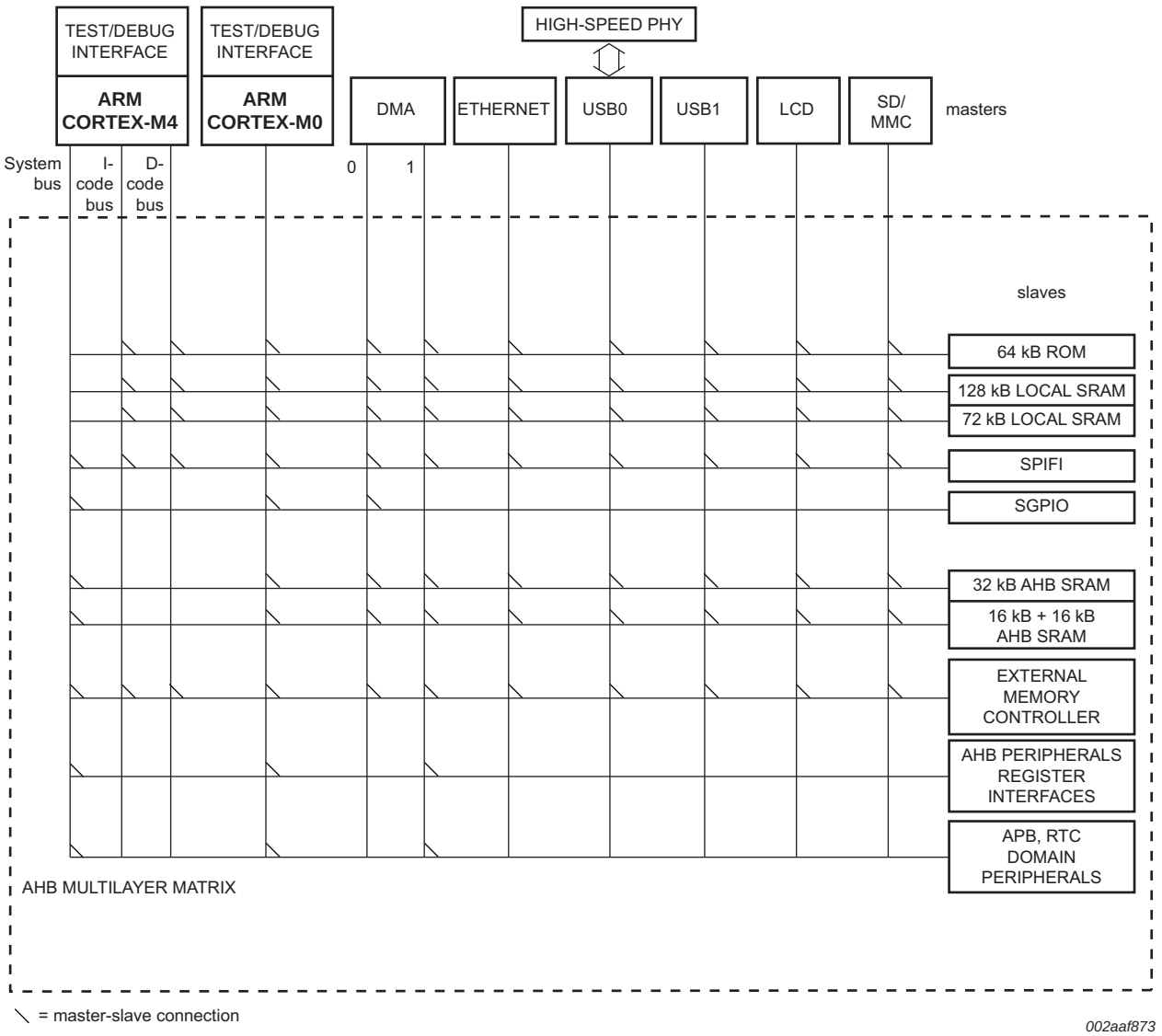


**Fig 6. AHB multilayer matrix master and slave connections**

## 7.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The ARM Cortex-M0 co-processor has its own NVIC with 32 vectored interrupts. Most peripheral interrupts are shared between the Cortex-M0 and Cortex-M4 NVICs.


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### 7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- The Cortex-M4 NVIC supports up to 53 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

### 7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags can represent more than one interrupt source.

## 7.7 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

**Remark:** The SysTick is not included in the ARM Cortex-M0 core.

## 7.8 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts
- C_CAN0/1 and QEI interrupts
- Ethernet, USB0, USB1 signals
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3)

**Remark:** Any interrupt can wake up the ARM Cortex-M4 from sleep mode if enabled in the NVIC.

## 7.9 Global Input Multiplexer Array (GIMA)

The GIMA routes signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.


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### 7.9.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

## 7.10 On-chip static RAM

The LPC4350/30/20/10 support up to 200 kB local SRAM and an additional 64 kB AHB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

## 7.11 In-System Programming (ISP)

In-System Programming (ISP) means programming or reprogramming the on-chip SRAM memory, using the boot loader software and the USART0 serial port. ISP can be performed when the part resides in the end-user board. ISP loads data into on-chip SRAM and execute code from on-chip SRAM.

## 7.12 Boot ROM

The internal ROM memory is used to store the boot code of the LPC4350/30/20/10. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.
- Supports booting from UART interfaces and external static memory such as NOR flash, quad SPI flash, and USB0 and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

Several boot modes are available depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins P2_9, P2_8, P1_2, and P1_1.

**Table 4. Boot mode when OTP BOOT_SRC bits are programmed**

| Boot mode | BOOT_SRC bit 3 | BOOT_SRC bit 2 | BOOT_SRC bit 1 | BOOT_SRC bit 0 | Description |
|---|---|---|---|---|---|
| Pin state | 0 | 0 | 0 | 0 | Boot source is defined by the reset state of P1_1, P1_2, P2_8, and P2_9 pins. See Table 5. |
| USART0 | 0 | 0 | 0 | 1 | Boot from device connected to USART0 using pins P2_0 and P2_1. |
| SPIFI | 0 | 0 | 1 | 0 | Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8. |
| EMC 8-bit | 0 | 0 | 1 | 1 | Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus. |


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**Table 4. Boot mode when OTP BOOT_SRC bits are programmed** *…continued*

| Boot mode | BOOT_SRC bit 3 | BOOT_SRC bit 2 | BOOT_SRC bit 1 | BOOT_SRC bit 0 | Description |
|---|---|---|---|---|---|
| EMC 16-bit | 0 | 1 | 0 | 0 | Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus. |
| EMC 32-bit | 0 | 1 | 0 | 1 | Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus. |
| USB0 | 0 | 1 | 1 | 0 | Boot from USB0. |
| USB1 | 0 | 1 | 1 | 1 | Boot from USB1. |
| SPI (SSP) | 1 | 0 | 0 | 0 | Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1]. |
| USART3 | 1 | 0 | 0 | 1 | Boot from device connected to USART3 using pins P2_3 and P2_4. |

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
**Remark:** Pin functions for SPIFI and SSP0 boot are different.

**Table 5. Boot mode when OPT BOOT_SRC bits are zero**

| Boot mode | Pins | | | | Description |
|---|---|---|---|---|---|
| | P2_9 | P2_8 | P1_2 | P1_1 | |
| USART0 | LOW | LOW | LOW | LOW | Boot from device connected to USART0 using pins P2_0 and P2_1. |
| SPIFI | LOW | LOW | LOW | HIGH | Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1]. |
| EMC 8-bit | LOW | LOW | HIGH | LOW | Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus. |
| EMC 16-bit | LOW | LOW | HIGH | HIGH | Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus. |
| EMC 32-bit | LOW | HIGH | LOW | LOW | Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus. |
| USB0 | LOW | HIGH | LOW | HIGH | Boot from USB0 |
| USB1 | LOW | HIGH | HIGH | LOW | Boot from USB1. |
| SPI (SSP) | LOW | HIGH | HIGH | HIGH | Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1]. |
| USART3 | HIGH | LOW | LOW | LOW | Boot from device connected to USART3 using pins P2_3 and P2_4. |

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
**Remark:** Pin functions for SPIFI and SSP0 boot are different.

## 7.13 Memory mapping

The memory map shown in Figure 7 and Figure 8 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.


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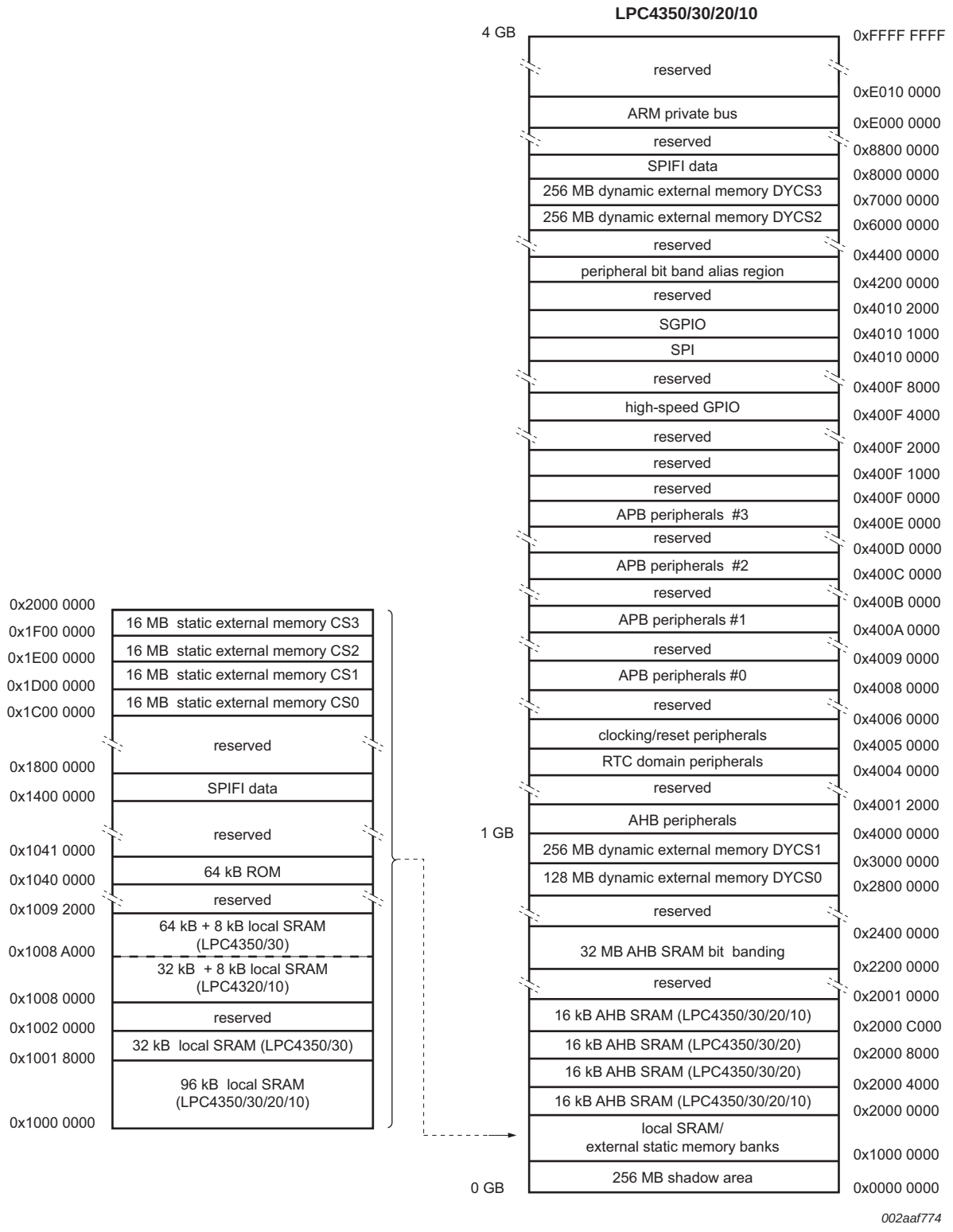


**Fig 7. LPC4350/30/20/10 Memory mapping (overview)**


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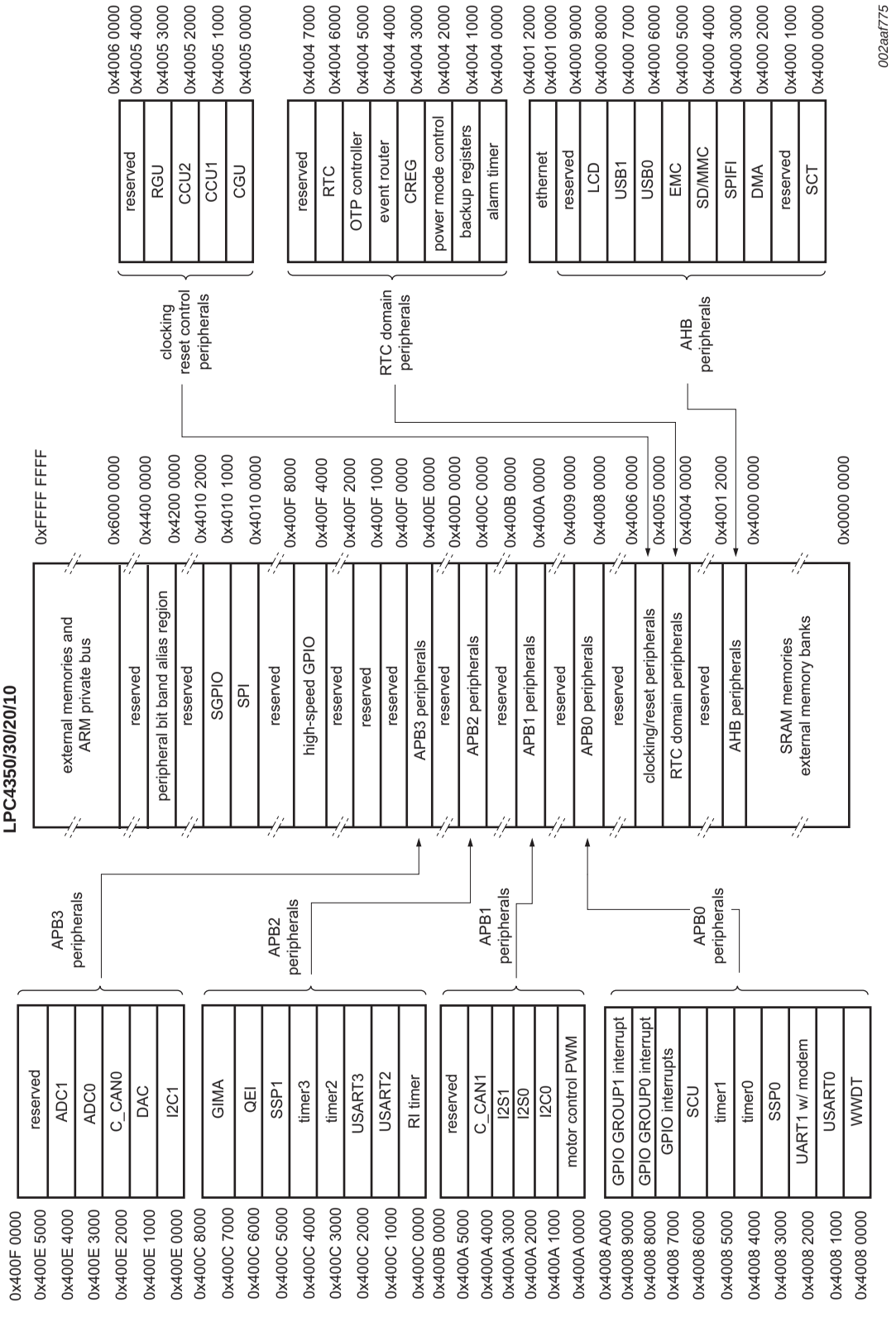


**Fig 8. LPC4350/30/20/10 Memory mapping (peripherals)**


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## 7.14 One-Time Programmable (OTP) memory

The OTP provides 64 bit + 256 bit One-Time Programmable (OTP) memory for general-purpose use.

## 7.15 General-Purpose I/O (GPIO)

The LPC4350/30/20/10 provide eight GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

### 7.15.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request (GPIO interrupts).
- Two GPIO group interrupts can be triggered by any pin or pins in each port (GPIO group0 and group1 interrupts).

## 7.16 Configurable digital peripherals

### 7.16.1 State Configurable Timer (SCTimer/PWM) subsystem

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values


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In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

#### 7.16.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Counters can be configured as up-counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs and interrupts.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - up to 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states

### 7.16.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

#### 7.16.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.
- Each slice has a 32-bit pattern match filter.


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## 7.17 AHB peripherals

### 7.17.1 General-Purpose DMA (GPDMA)

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

#### 7.17.1.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

### 7.17.2 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.


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After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

#### 7.17.2.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
- Supports DMA access.

### 7.17.3 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

- Secure Digital memory (SD version 3.0).
- Secure Digital I/O (SDIO version 2.0).
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1).
- MultiMedia Cards (MMC version 4.4).

### 7.17.4 External Memory Controller (EMC)

The LPC4350/30/20/10 EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

#### 7.17.4.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines-wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay


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- Output enable and write enable delays
- Extended wait

- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

**Note:** Synchronous static memory devices (synchronous burst mode) are not supported.

### 7.17.5 High-speed USB Host/Device/OTG interface (USB0)

**Remark:** The USB0 controller is available on parts LPC4350/30/20. See Table 2.

The USB OTG module allows the LPC4350/30/20/10 to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

#### 7.17.5.1 Features

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

### 7.17.6 High-speed USB Host/Device interface with ULPI (USB1)

**Remark:** The USB1 controller is available on parts LPC4350/30. See Table 2.

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

#### 7.17.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.


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- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

### 7.17.7 LCD controller

**Remark:** The LCD controller is available on LPC4350 only. See Table 2.

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

#### 7.17.7.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.


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- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

### 7.17.8 Ethernet

**Remark:** The Ethernet peripheral is available on parts LPC4350/30. See Table 2.

#### 7.17.8.1 Features

- 10/100 Mbit/s.
- DMA support.
- Power management remote wake-up frame and magic packet detection.
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

## 7.18 Digital serial peripherals

### 7.18.1 UART1

The LPC4350/30/20/10 contain one UART with standard transmit and receive data lines. UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

#### 7.18.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control.
- Support for RS-485/9-bit/EIA-485 mode (UART1).


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- DMA support.

### 7.18.2 USART0/2/3

The LPC4350/30/20/10 contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

#### 7.18.2.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode.
- USART3 includes an IrDA mode to support infrared communication.
- All USARTs have DMA support.
- Support for synchronous mode at a data bit rate of up to 8 Mbit/s.
- Smart card mode conforming to ISO7816 specification

### 7.18.3 SPI serial I/O controller

The LPC4350/30/20/10 contain one SPI controller. SPI is a full-duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

#### 7.18.3.1 Features

- Maximum SPI data bit rate 25 Mbit/s.
- Compliant with SPI specification.
- Synchronous, serial, full-duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.
- 8 bits to 16 bits per transfer.

### 7.18.4 SSP serial I/O controller

**Remark:** The LPC4350/30/20/10 contain two SSP controllers.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full-duplex


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transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

#### 7.18.4.1 Features

- Maximum SSP speed in full-duplex mode of 25 Mbit/s; for transmit only 50 Mbit/s (master) and 17 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.
- DMA transfers supported by GPDMA.

### 7.18.5 $I^2C$-bus interface

**Remark:** The LPC4350/30/20/10 contain two $I^2C$-bus interfaces.

The $I^2C$-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The $I^2C$ is a multi-master bus and can be controlled by more than one bus master connected to it.

#### 7.18.5.1 Features

- $I^2C0$ is a standard $I^2C$-compliant bus interface with open-drain pins. $I^2C0$ also supports Fast mode plus with bit rates up to 1 Mbit/s.
- $I^2C1$ uses standard I/O pins with bit rates of up to 400 kbit/s (Fast $I^2C$-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The $I^2C$-bus can be used for test and diagnostic purposes.
- All $I^2C$-bus controllers support multiple address recognition and a bus monitor mode.

### 7.18.6 $I^2S$ interface

**Remark:** The LPC4350/30/20/10 contain two $I^2S$-bus interfaces.


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The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

#### 7.18.6.1 Features

- The I²S interface has separate input/output channels, each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96, 192) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I²S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests controlled by programmable buffer levels. The DMA requests are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S-bus input and I²S-bus output.

### 7.18.7 C_CAN

**Remark:** The LPC4350/30/20/10 contain two C_CAN controllers.

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can create powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

#### 7.18.7.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.


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## 7.19 Counter/timers and motor control

### 7.19.1 General purpose 32-bit timers/external event counters

The LPC4350/30/20/10 include four 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

#### 7.19.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

### 7.19.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

### 7.19.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

#### 7.19.3.1 Features

- Tracks encoder position.


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- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

### 7.19.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

#### 7.19.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

### 7.19.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

#### 7.19.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.


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- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

## 7.20 Analog peripherals

### 7.20.1 Analog-to-Digital Converter (ADC0/1)

#### 7.20.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

### 7.20.2 Digital-to-Analog Converter (DAC)

#### 7.20.2.1 Features

- 10-bit resolution.
- Monotonic by design (resistor string architecture).
- Controllable conversion speed.
- Low-power consumption.

## 7.21 Peripherals in the RTC power domain

### 7.21.1 RTC

The Real-Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

#### 7.21.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.


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- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

### 7.21.2 Alarm timer

The alarm timer is a 16-bit timer and counts down at 1 kHz from a preset value generating alarms in intervals of up to 1 min. The counter triggers a status bit when it reaches 0x00 and asserts an interrupt if enabled.

The alarm timer is part of the RTC power domain and can be battery powered.

## 7.22 System control

### 7.22.1 Configuration registers (CREG)

The following settings are controlled in the configuration register block:

- BOD trip settings
- Oscillator output
- DMA-to-peripheral muxing
- Ethernet mode
- Memory mapping
- Timer/USART inputs
- Enabling the USB controllers

In addition, the CREG block contains the part identification and part configuration information.

### 7.22.2 System Control Unit (SCU)

The system control unit determines the function and electrical mode of the digital pins. By default function 0 is selected for all pins with pull-up enabled. For pins that support a digital and analog function, the ADC function select registers in the SCU enable the analog function.

A separate set of analog I/Os for the ADCs and the DAC as well as most USB pins are located on separate pads and are not controlled through the SCU.

In addition, the clock delay register for the SDRAM EMC_CLK pins and the registers that select the pin interrupts are located in the SCU.

### 7.22.3 Clock Generation Unit (CGU)

The Clock Generator Unit (CGU) generates several base clocks. The base clocks can be unrelated in frequency and phase and can have different clock sources within the CGU. One CGU base clock is routed to the CLKOUT pins. The base clock that generates the CPU clock is referred to as CCLK.

Multiple branch clocks are derived from each base clock. The branch clocks offer flexible control for power-management purposes. All branch clocks are outputs of one of two Clock Control Units (CCUs) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase.


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### 7.22.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC4350/30/20/10 use the IRC as the clock source. The boot loader then configures the PLL1 to provide a 96 MHz clock for the core and the PLL0USB or PLL0AUDIO as needed if an external boot source is selected.

### 7.22.5 PLL0USB (for USB0)

PLL0 is a dedicated PLL for the USB0 High-speed controller.

PLL0 accepts an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

### 7.22.6 PLL0AUDIO (for audio)

The audio PLL PLL0AUDIO is a general-purpose PLL with a small step size. This PLL accepts an input clock frequency derived from an external oscillator or internal IRC. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). A sigma-delta converter modulates the PLL divider ratios to obtain the desired output frequency. The output frequency can be set as a multiple of the sampling frequency $f_s$ to $32 \times f_s$, $64 \times f_s$, $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, $512 \times f_s$ and the sampling frequency $f_s$ can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96,192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

### 7.22.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

### 7.22.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC4350/30/20/10.

### 7.22.9 Power control

The LPC4350/30/20/10 feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.


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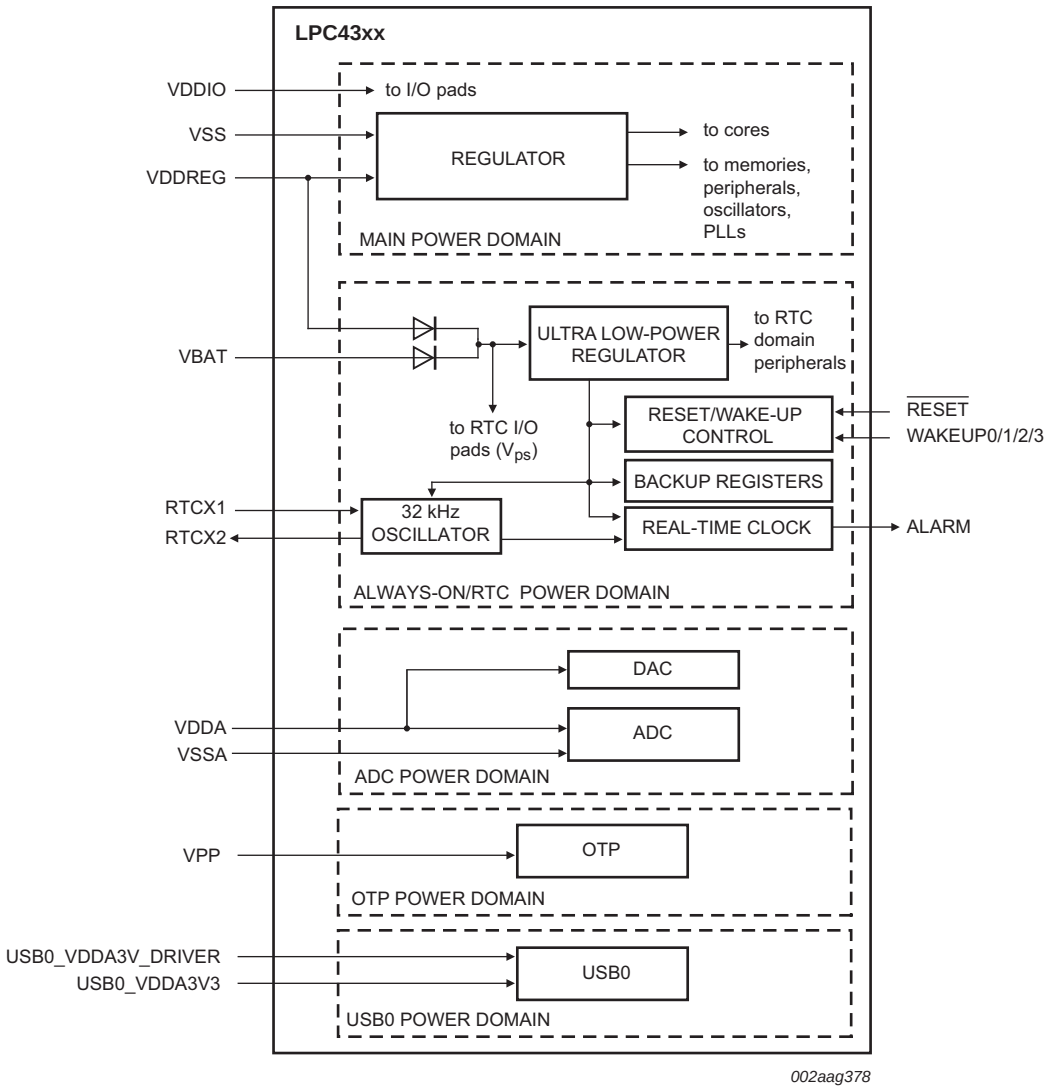


**Fig 9. Power domains**

### 7.22.10 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC4350/30/20/10 support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
   a. Deep-sleep mode
   b. Power-down mode
   c. Deep power-down mode


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Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

Wake-up from sleep mode is caused by an interrupt or event in the core's NVIC. The interrupt is captured in the NVIC and an event is captured in the Event router. Both cores can wake up from sleep mode independently of each other.

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot.

## 7.23 Serial Wire Debug/JTAG

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

**Remark:** Serial Wire Debug is supported for the ARM Cortex-M4 only,

The ARM Cortex-M0 coprocessor supports JTAG debug. A standard ARM Cortex-compliant debugger can debug the ARM Cortex-M4 and the ARM Cortex-M0 cores separately or both cores simultaneously.

**Remark:** In order to debug the ARM Cortex-M0, release the M0 reset by software in the RGU block.


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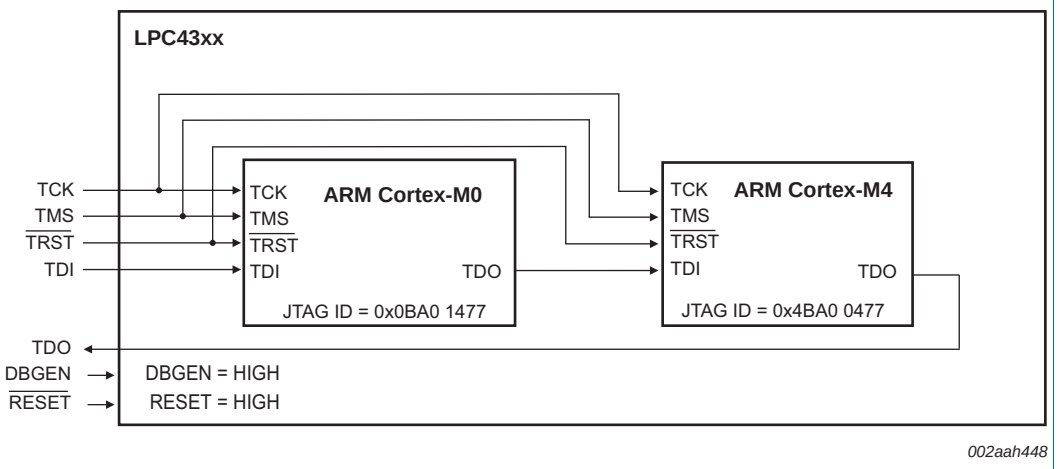


**Fig 10. Dual-core debug configuration**


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# 8. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(REG)(3V3)}$ | regulator supply voltage (3.3 V) | on pin VDDREG | | –0.5 | 3.6 | V |
| $V_{DD(IO)}$ | input/output supply voltage | on pin VDDIO | | –0.5 | 3.6 | V |
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | on pin VDDA | | –0.5 | 3.6 | V |
| $V_{BAT}$ | battery supply voltage | on pin VBAT | | –0.5 | 3.6 | V |
| $V_{prog(pf)}$ | polyfuse programming voltage | on pin VPP | | –0.5 | 3.6 | V |
| $V_I$ | input voltage | only valid when $V_{DD(IO)} \geq 2.2$ V | [2] | | | |
| | | 5 V tolerant I/O pins | | –0.5 | 5.5 | V |
| | | ADC/DAC pins and digital I/O pins configured for an analog function | | –0.5 | $V_{DDA(3V3)}$ | V |
| | | USB0 pins USB0_DP; USB0_DM;USB0_VBUS | | –0.3 | 5.25 | V |
| | | USB0 pins USB0_ID; USB0_RREF | | –0.3 | 3.6 | V |
| | | USB1 pins USB1_DP and USB1_DM | | –0.3 | 5.25 | V |
| $I_{DD}$ | supply current | per supply pin | [3] | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | [3] | - | 100 | mA |
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C | | - | 100 | mA |
| $T_{stg}$ | storage temperature | | [4] | –65 | +150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | | - | 1.5 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins | [5] | –2000 | +2000 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.


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# 9. Thermal characteristics

The average chip junction temperature, $T_j$ (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- $T_{amb}$ = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- $P_D$ = sum of internal and I/O power dissipation

The internal power dissipation is the product of $I_{DD}$ and $V_{DD}$. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

**Table 7. Thermal characteristics**

*$V_{DD}$ = 2.2 V to 3.6 V; $T_{amb}$ = −40 °C to +85 °C unless otherwise specified;*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{j(max)}$ | maximum junction temperature | - | - | 125 | °C |

**Table 8. Thermal resistance (LQFP packages)**

| Symbol | Parameter | Conditions | Thermal resistance in °C/W ±15 % |
|---|---|---|---|
| | | | LQFP144 |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC (4.5 in × 4 in); still air | 38 |
| | | Single-layer (4.5 in × 3 in); still air | 50 |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | 11 |

**Table 9. Thermal resistance value (BGA packages)**

| Symbol | Parameter | Conditions | Thermal resistance in °C/W ±15 % | | |
|---|---|---|---|---|---|
| | | | LBGA256 | TFBGA180 | TFBGA100 |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC (4.5 in × 4 in); still air | 29 | 38 | 46 |
| | | 8-layer (4.5 in × 3 in); still air | 24 | 30 | 37 |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | 14 | 11 | 11 |


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# 10. Static characteristics

**Table 10. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply pins** | | | | | | | |
| $V_{DD(IO)}$ | input/output supply voltage | | | 2.2 | - | 3.6 | V |
| $V_{DD(REG)(3V3)}$ | regulator supply voltage (3.3 V) | | [2] | 2.2 | - | 3.6 | V |
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | on pin VDDA | | 2.2 | - | 3.6 | V |
| | | on pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3 | | 3.0 | 3.3 | 3.6 | V |
| $V_{BAT}$ | battery supply voltage | | [2] | 2.2 | - | 3.6 | V |
| $V_{prog(pf)}$ | polyfuse programming voltage | on pin VPP (for OTP) | [3] | 2.7 | - | 3.6 | V |
| $I_{prog(pf)}$ | polyfuse programming current | on pin VPP; OTP programming time ≤ 1.6 ms | | - | - | 30 | mA |
| $I_{DD(REG)(3V3)}$ | regulator supply current (3.3 V) | Active mode; M0-core in reset; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled | | | | | |
| | | CCLK = 12 MHz | [4] | - | 6.6 | - | mA |
| | | CCLK = 60 MHz | [4] | | 25.3 | - | mA |
| | | CCLK = 120 MHz | [4] | - | 48.4 | - | mA |
| | | CCLK = 180 MHz | [4] | - | 72.0 | - | mA |
| | | CCLK = 204 MHz | [4] | - | 81.5 | - | mA |
| $I_{DD(REG)(3V3)}$ | regulator supply current (3.3 V) | after WFE/WFI instruction executed from RAM; all peripherals disabled; M0 core in reset | | | | | |
| | | sleep mode | [4][5] | - | 5.0 | - | mA |
| | | deep-sleep mode | [4] | - | 30 | - | µA |
| | | power-down mode | [4] | - | 15 | - | µA |
| | | deep power-down mode | [4][6] | - | 0.03 | - | µA |
| | | deep power-down mode; VBAT floating | [4] | - | 2 | - | µA |
| $I_{BAT}$ | battery supply current | active mode; $V_{BAT}$ = 3.2 V; $V_{DD(REG)(3V3)}$ = 3.6 V. | [7] | - | 0 | - | nA |


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**Table 10. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BAT}$ | battery supply current | $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{BAT}$ = 3.6 V | [8] | | | | |
| | | deep-sleep mode | | - | 2 | - | µA |
| | | power-down mode | [8] | - | 2 | - | µA |
| | | deep power-down mode | [8] | - | 2 | - | µA |
| $I_{DD(IO)}$ | I/O supply current | deep sleep mode | - | - | 1 | - | µA |
| | | power-down mode | - | - | 1 | - | µA |
| | | deep power-down mode | [9] | - | 0.05 | - | µA |
| $I_{DDA}$ | Analog supply current | on pin VDDA; | [11] | - | 0.4 | - | |
| | | deep sleep mode | | | | | µA |
| | | power-down mode | [11] | - | 0.4 | - | µA |
| | | deep power-down mode | [11] | - | 0.007 | - | µA |
| **RESET, RTC_ALARM, WAKEUPn pins** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | [10] | 0.8 × ($V_{ps}$ − 0.35) | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | [10] | 0 | - | 0.3 × ($V_{ps}$ − 0.1) | V |
| $V_{hys}$ | hysteresis voltage | | [10] | 0.05 × ($V_{ps}$ − 0.35) | - | - | V |
| $V_o$ | output voltage | | [10] | - | $V_{ps}$ - 0.2 | - | V |
| **Standard I/O pins - normal drive strength** | | | | | | | |
| $C_I$ | input capacitance | | | - | - | 2 | pF |
| $I_{LL}$ | LOW-level leakage current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 3 | - | nA |
| $I_{LH}$ | HIGH-level leakage current | $V_I$ = $V_{DD(IO)}$; on-chip pull-down resistor disabled | | - | 3 | - | nA |
| | | $V_I$ = 5 V | | - | - | 20 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value | | - | 3 | - | nA |
| $V_I$ | input voltage | pin configured to provide a digital function; | | 0 | - | 5.5 | V |
| | | $V_{DD(IO)}$ ≥ 2.2 V | | | | | |
| | | $V_{DD(IO)}$ = 0 V | | 0 | - | 3.6 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD(IO)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7 × $V_{DD(IO)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | 0 | - | 0.3 × $V_{DD(IO)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | 0.1 × $V_{DD(IO)}$ | - | - | V |


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**Table 10. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −6 mA | | $V_{DD(IO)}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 6 mA | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH}$ = $V_{DD(IO)}$ − 0.4 V | | −6 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 6 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | drive HIGH; connected to ground | [12] | - | - | 86.5 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | drive LOW; connected to $V_{DD(IO)}$ | [12] | - | - | 76.5 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | [14][15] [16] | - | 93 | - | µA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V | [14][15] [16] | - | −62 | - | µA |
| | | $V_{DD(IO)}$ < $V_I$ ≤ 5 V | | - | 10 | - | µA |
| $R_S$ | series resistance | on I/O pins with analog function; analog function enabled | | | 200 | | Ω |
| **I/O pins - high drive strength** | | | | | | | |
| $C_I$ | input capacitance | | | - | - | 5.2 | pF |
| $I_{LL}$ | LOW-level leakage current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 3 | - | nA |
| $I_{LH}$ | HIGH-level leakage current | $V_I$ = $V_{DD(IO)}$; on-chip pull-down resistor disabled | | - | 3 | - | nA |
| | | $V_I$ = 5 V | | - | - | 20 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value | | - | 3 | - | nA |
| $V_I$ | input voltage | pin configured to provide a digital function; $V_{DD(IO)}$ ≥ 2.2 V | | 0 | - | 5.5 | V |
| | | $V_{DD(IO)}$ = 0 V | | 0 | - | 3.6 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD(IO)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7 × $V_{DD(IO)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | 0 | - | 0.3 × $V_{DD(IO)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | 0.1 × $V_{DD(IO)}$ | - | - | V |
| $I_{pd}$ | pull-down current | $V_I$ = $V_{DD(IO)}$ | [14][15] [16] | - | 62 | - | µA |


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**Table 10. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{pu}$ | pull-up current | $V_I$ = 0 V | [14][15] [16] | - | −62 | - | µA |
| | | $V_{DD(IO)} < V_I \leq 5$ V | | - | 10 | - | µA |
| I/O pins - high drive strength: standard drive mode | | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(IO)} - 0.4$ V | | −4 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 4 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | drive HIGH; connected to ground | [12] | - | - | 32 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | drive LOW; connected to $V_{DD(IO)}$ | [12] | - | - | 32 | mA |
| I/O pins - high drive strength: medium drive mode | | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(IO)} - 0.4$ V | | −8 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 8 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | drive HIGH; connected to ground | [12] | - | - | 65 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | drive LOW; connected to $V_{DD(IO)}$ | [12] | - | - | 63 | mA |
| I/O pins - high drive strength: high drive mode | | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(IO)} - 0.4$ V | | −14 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 14 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | drive HIGH; connected to ground | [12] | - | - | 113 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | drive LOW; connected to $V_{DD(IO)}$ | [12] | - | - | 110 | mA |
| I/O pins - high drive strength: ultra-high drive mode | | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(IO)} - 0.4$ V | | −20 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 20 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | drive HIGH; connected to ground | [12] | - | - | 165 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | drive LOW; connected to $V_{DD(IO)}$ | [12] | - | - | 156 | mA |
| **I/O pins - high-speed** | | | | | | | |
| $C_I$ | input capacitance | | | - | - | 2 | pF |
| $I_{LL}$ | LOW-level leakage current | $V_I$ = 0 V; on-chip pull-up resistor disabled | | - | 3 | - | nA |


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**Table 10. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LH}$ | HIGH-level leakage current | $V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled | | - | 3 | - | nA |
| | | $V_I$ = 5 V | | - | - | 20 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value | | - | 3 | - | nA |
| $V_I$ | input voltage | pin configured to provide a digital function; | | | | | |
| | | $V_{DD(IO)} \geq$ 2.2 V | | 0 | - | 5.5 | V |
| | | $V_{DD(IO)}$ = 0 V | | 0 | - | 3.6 | V |
| $V_O$ | output voltage | output active | | 0 | - | $V_{DD(IO)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7 × $V_{DD(IO)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | 0 | - | 0.3 × $V_{DD(IO)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | 0.1 × $V_{DD(IO)}$ | - | - | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −8 mA | | $V_{DD(IO)}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 8 mA | | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH} = V_{DD(IO)}$ − 0.4 V | | −8 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 8 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | drive HIGH; connected to ground | [12] | - | - | 86 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | drive LOW; connected to $V_{DD(IO)}$ | [12] | - | - | 76 | mA |
| $I_{pd}$ | pull-down current | $V_I = V_{DD(IO)}$ | [14][15][16] | - | 62 | - | µA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V | [14][15][16] | - | −62 | - | µA |
| | | $V_{DD(IO)} < V_I \leq$ 5 V | | - | 0 | - | µA |
| **Open-drain $I^2C$0-bus pins** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7 × $V_{DD(IO)}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | | 0 | 0.14 | 0.3 × $V_{DD(IO)}$ | V |
| $V_{hys}$ | hysteresis voltage | | | 0.1 × $V_{DD(IO)}$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OLS}$ = 3 mA | | - | - | 0.4 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{DD(IO)}$ | [13] | - | 4.5 | - | µA |
| | | $V_I$ = 5 V | | - | - | 10 | µA |


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**Table 10. Static characteristics** *...continued*

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Oscillator pins** | | | | | | | |
| $V_{i(XTAL1)}$ | input voltage on pin XTAL1 | | | −0.5 | - | 1.2 | V |
| $V_{o(XTAL2)}$ | output voltage on pin XTAL2 | | | −0.5 | - | 1.2 | V |
| $C_{io}$ | input/output capacitance | | [17] | - | - | 0.8 | pF |
| **USB0 pins**[18] | | | | | | | |
| $V_I$ | input voltage | on pins USB0_DP; USB0_DM; USB0_VBUS | | | | | |
| | | $V_{DD(IO)} \geq 2.2$ V | | 0 | - | 5.25 | V |
| | | $V_{DD(IO)} = 0$ V | | 0 | - | 3.6 | V |
| $R_{pd}$ | pull-down resistance | on pin USB0_VBUS | | 48 | 64 | 80 | kΩ |
| $V_{IC}$ | common-mode input voltage | high-speed mode | | −50 | 200 | 500 | mV |
| | | full-speed/low-speed mode | | 800 | - | 2500 | mV |
| | | chirp mode | | −50 | - | 600 | mV |
| $V_{i(dif)}$ | differential input voltage | | | 100 | 400 | 1100 | mV |
| **USB1 pins (USB1_DP/USB1_DM)**[18] | | | | | | | |
| $I_{OZ}$ | OFF-state output current | $0 V < V_I < 3.3$ V | [18] | - | - | ±10 | µA |
| $V_{BUS}$ | bus supply voltage | | [19] | - | - | 5.25 | V |
| $V_{DI}$ | differential input sensitivity voltage | \|(D+) − (D−)\| | | 0.2 | - | - | V |
| $V_{CM}$ | differential common mode voltage range | includes $V_{DI}$ range | | 0.8 | - | 2.5 | V |
| $V_{th(rs)se}$ | single-ended receiver switching threshold voltage | | | 0.8 | - | 2.0 | V |
| $V_{OL}$ | LOW-level output voltage for low-/full-speed | $R_L$ of 1.5 kΩ to 3.6 V | | - | - | 0.18 | V |
| $V_{OH}$ | HIGH-level output voltage (driven) for low-/full-speed | $R_L$ of 15 kΩ to GND | | 2.8 | - | 3.5 | V |
| $C_{trans}$ | transceiver capacitance | pin to GND | | - | - | 20 | pF |
| $Z_{DRV}$ | driver output impedance for driver which is not high-speed capable | with 33 Ω series resistor; steady state drive | [20] | 36 | - | 44.1 | Ω |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V. See Figure 18.

[3] Pin VPP should either be not connected (when OTP does not need to be programmed) or tied to pins VDDIO and VDDREG to ensure the same ramp-up time for both supply voltages.

[4] $V_{DD(REG)(3V3)} = 3.3$ V; $V_{DD(IO)} = 3.3$ V; $T_{amb} = 25$ °C.


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[5] PLL1 disabled; IRC running; CCLK = 12 MHz.

[6] $V_{BAT}$ = 3.6 V.

[7] $V_{DD(IO)} = V_{DDA}$ = 3.6 V; over entire frequency range CCLK = 12 MHz to 180 MHz.

[8] On pin VBAT; $T_{amb}$ = 25 °C.

[9] $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V. Input leakage increases when $V_{DD(IO)}$ is floating or grounded. It is recommended to keep $V_{DD(REG)(3V3)}$ and $V_{DD(IO)}$ powered in deep power-down mode.

[10] $V_{ps}$ corresponds to the output of the power switch (see Figure 9) which is determined by the greater of $V_{BAT}$ and $V_{DD(Reg)(3V3)}$.

[11] $V_{DDA(3V3)}$ = 3.3 V; $T_{amb}$ = 25 °C.

[12] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[13] To $V_{SS}$.

[14] The values specified are simulated and absolute values.

[15] The weak pull-up resistor is connected to the $V_{DD(IO)}$ rail and pulls up the I/O pin to the $V_{DD(IO)}$ level.

[16] The input cell disables the weak pull-up resistor when the applied input voltage exceeds $V_{DD(IO)}$.

[17] The parameter value specified is a simulated value excluding bond capacitance.

[18] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[19] $V_{DD(IO)}$ present.

[20] Includes external resistors of 33 Ω ± 1 % on D+ and D−.


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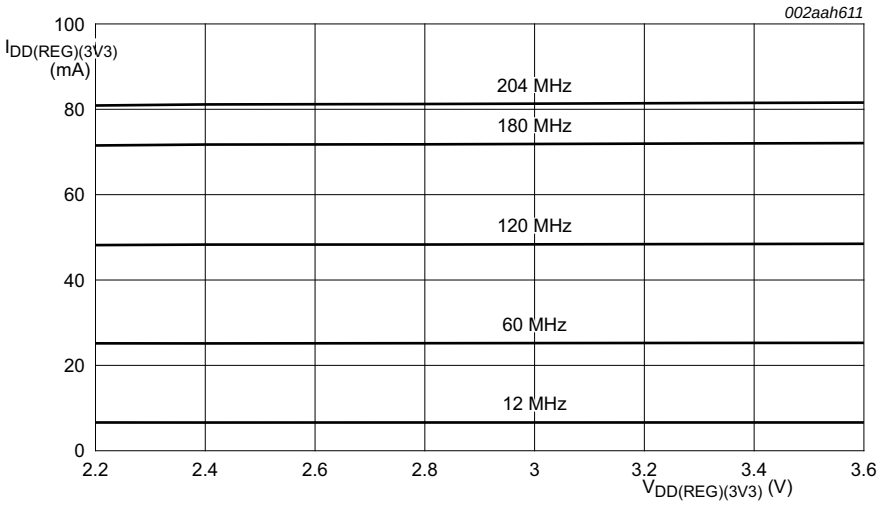
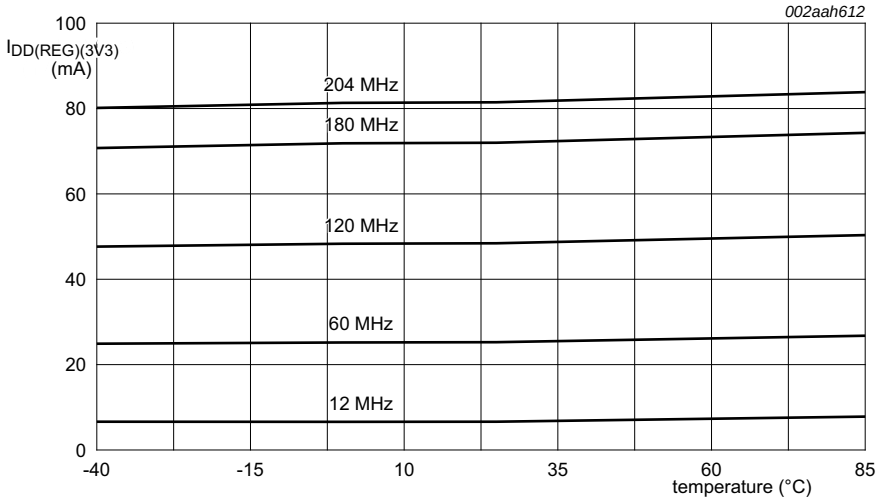
## 10.1 Power consumption




Conditions: $T_{amb}$ = 25 °C; active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

**Fig 11. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode**




Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V, Active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

**Fig 12. Typical supply current versus temperature in Active mode**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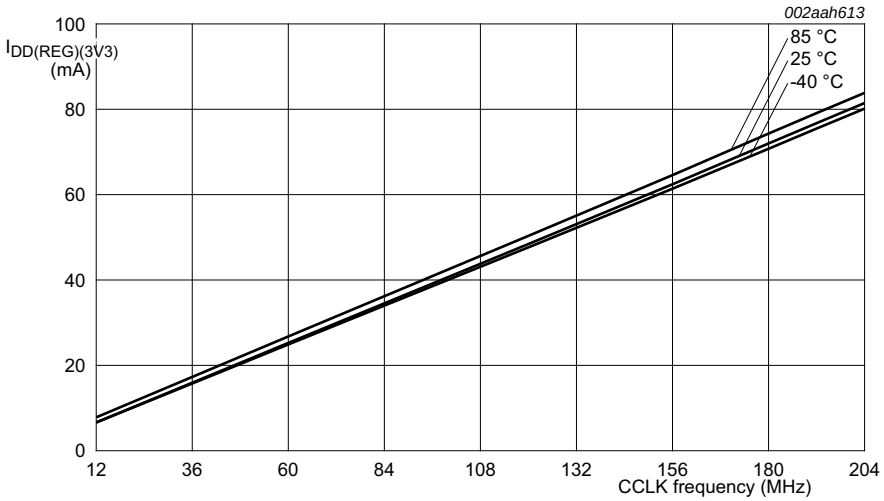
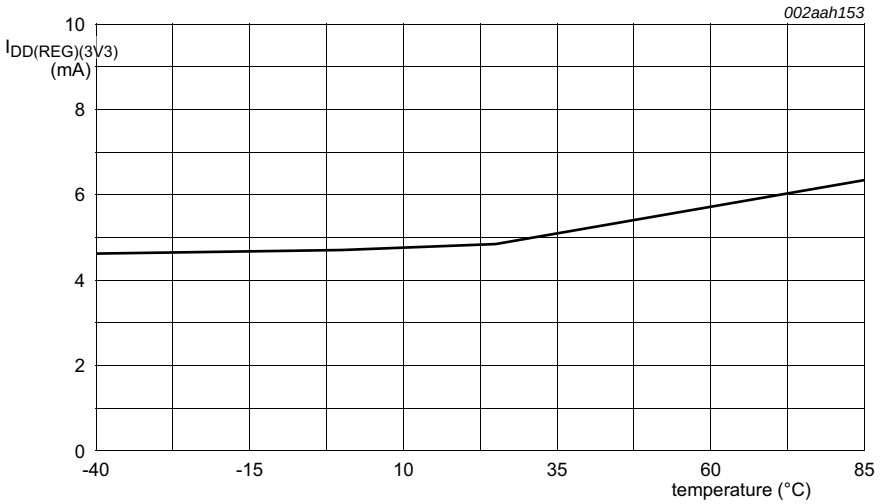



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; Active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

**Fig 13. Typical supply current versus frequency in Active mode**




Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled; core clock CCLK = 12 MHz.

**Fig 14. Typical supply current versus temperature in Sleep mode**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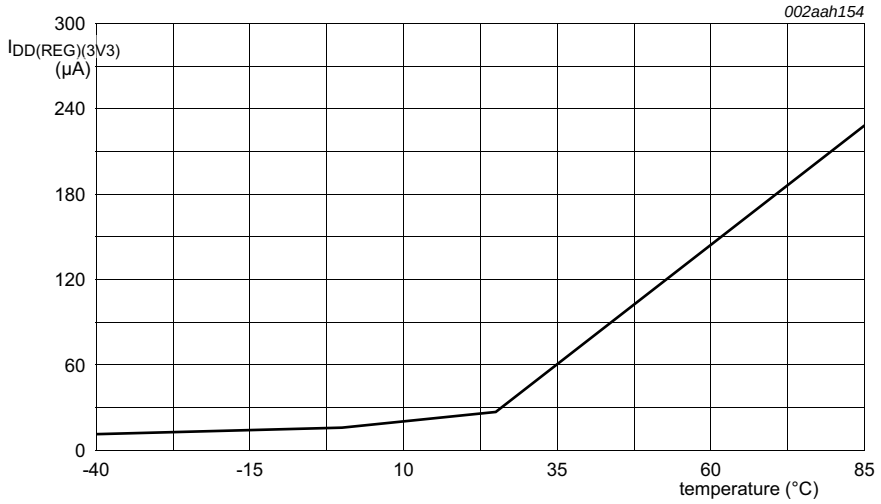
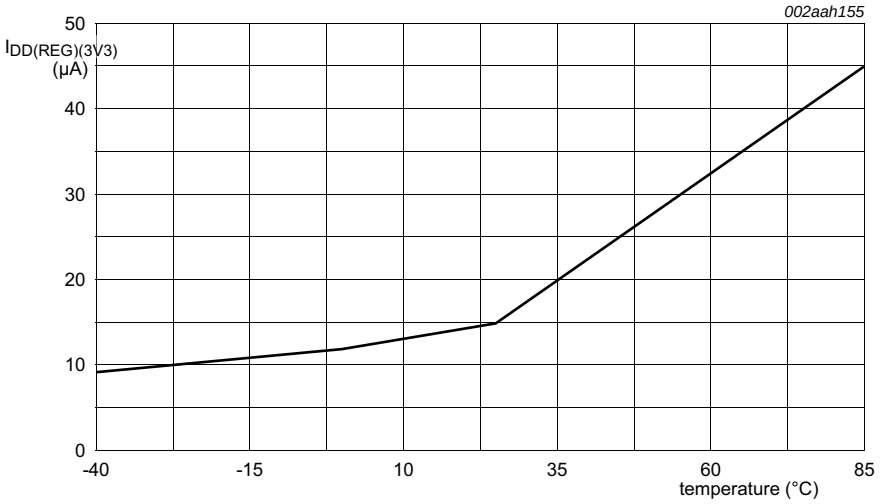



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{BAT}$ floating; $V_{DD(IO)}$ = 3.3 V.

**Fig 15. Typical supply current versus temperature in Deep-sleep mode**




Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{BAT}$ floating; $V_{DD(IO)}$ = 3.3 V.

**Fig 16. Typical supply current versus temperature in Power-down mode**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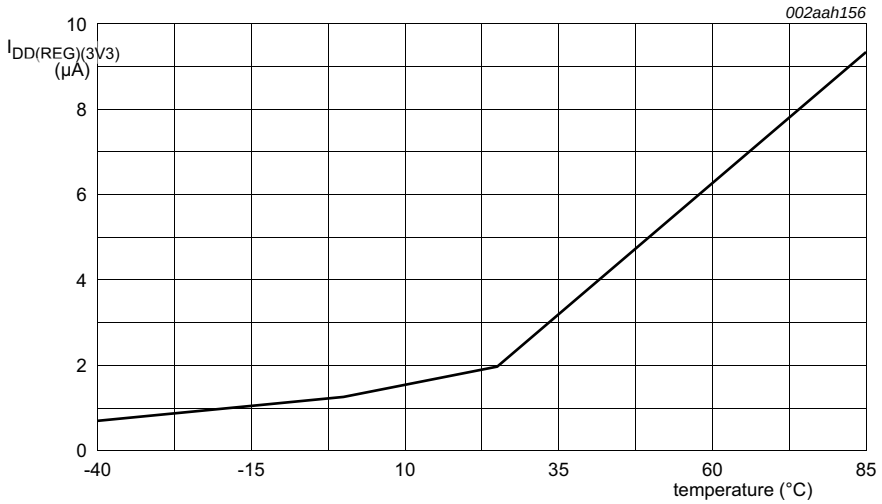
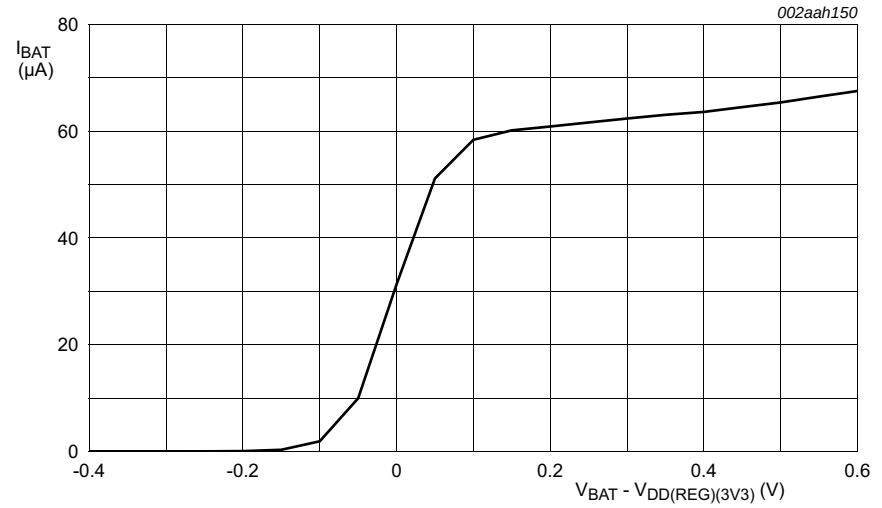



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{BAT}$ floating; $V_{DD(IO)}$ = 3.3 V.

**Fig 17. Typical supply current versus temperature in Deep power-down mode**




Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; CCLK = 12 MHz.

**Fig 18. Typical battery supply current in Active mode**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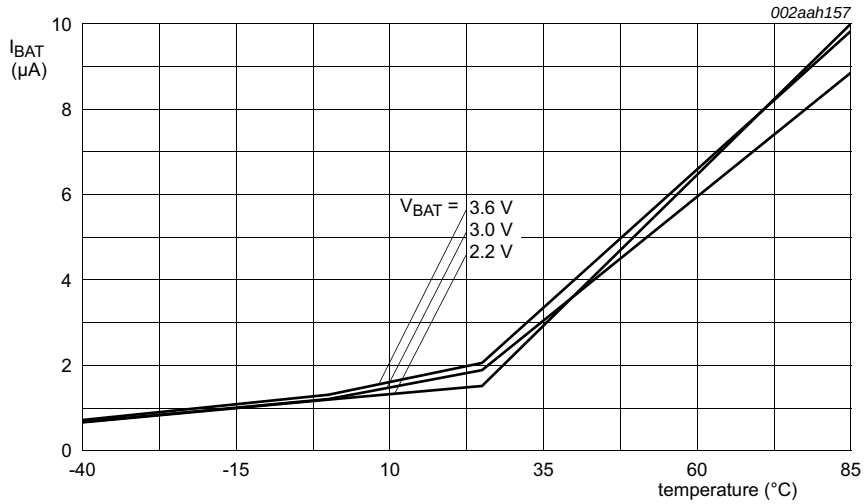


Conditions: $V_{DD(REG)(3V3)}$, $V_{DD(IO)}$ floating.

**Fig 19. Typical battery supply versus temperature in Deep power-down mode**

## 10.2 Peripheral power consumption

The typical power consumption at T = 25 °C for each individual peripheral is measured as follows:

1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

**Table 11. Peripheral power consumption**

| Peripheral | Branch clock | $I_{DD(REG)(3V3)}$ in mA | |
|---|---|---|---|
| | | Branch clock frequency = 48 MHz | Branch clock frequency = 96 MHz |
| M0 core | CLK_M4_M0APP | 3.3 | 6.6 |
| I2C1 | CLK_APB3_I2C1 | 0.01 | 0.02 |
| I2C0 | CLK_APB1_I2C0 | 0.02 | 0.01 |
| DAC | CLK_APB3_DAC | 0.01 | 0.02 |
| ADC0 | CLK_APB3_ADC0 | 0.05 | 0.05 |
| ADC1 | CLK_APB3_ADC1 | 0.04 | 0.04 |
| CAN0 | CLK_APB3_CAN0 | 0.17 | 0.17 |
| CAN1 | CLK_APB1_CAN1 | 0.17 | 0.17 |
| MOTOCON | CLK_APB1_MOTOCON | 0.05 | 0.05 |
| I2S | CLK_APB1_I2S | 0.11 | 0.11 |
| SPIFI | CLK_SPIFI, CLK_M4_SPIFI | 0.95 | 1.85 |
| GPIO | CLK_M4_GPIO | 0.66 | 1.31 |


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**Table 11. Peripheral power consumption**

| Peripheral | Branch clock | $I_{DD(REG)(3V3)}$ in mA | |
|---|---|---|---|
| | | Branch clock frequency = 48 MHz | Branch clock frequency = 96 MHz |
| LCD | CLK_M4_LCD | 0.85 | 1.72 |
| ETHERNET | CLK_M4_ETHERNET | 1.05 | 2.09 |
| UART0 | CLK_M4_UART0, CLK_APB0_UART0 | 0.3 | 0.38 |
| UART1 | CLK_M4_UART1, CLK_APB0_UART1 | 0.27 | 0.48 |
| UART2 | CLK_M4_UART2, CLK_APB2_UART2 | 0.27 | 0.47 |
| UART3 | CLK_M4_USART3, CLK_APB2_UART3 | 0.29 | 0.49 |
| TIMER0 | CLK_M4_TIMER0 | 0.07 | 0.14 |
| TIMER1 | CLK_M4_TIMER1 | 0.07 | 0.14 |
| TIMER2 | CLK_M4_TIMER2 | 0.07 | 0.15 |
| TIMER3 | CLK_M4_TIMER3 | 0.06 | 0.11 |
| SDIO | CLK_M4_SDIO, CLK_SDIO | 0.79 | 1.37 |
| SCTimer/PWM | CLK_M4_SCT | 0.52 | 1.05 |
| SSP0 | CLK_M4_SSP0, CLK_APB0_SSP0 | 0.12 | 0.21 |
| SSP1 | CLK_M4_SSP1, CLK_APB2_SSP1 | 0.15 | 0.28 |
| DMA | CLK_M4_DMA | 1.88 | 3.71 |
| WWDT | CLK_M4_WWDT | 0.05 | 0.08 |
| QEI | CLK_M4_QEI | 0.33 | 0.68 |
| USB0 | CLK_M4_USB0, CLK_USB0 | 1.46 | 3.32 |
| USB1 | CLK_M4_USB1, CLK_USB1 | 2.83 | 5.03 |
| RITIMER | CLK_M4_RITIMER | 0.04 | 0.08 |
| EMC | CLK_M4_EMC, CLK_M4_EMC_DIV | 3.6 | 6.97 |
| SCU | CLK_M4_SCU | 0.09 | 0.23 |
| CREG | CLK_M4_CREG | 0.37 | 0.72 |
| SGPIO | CLK_PERIPH_SGPIO | 0.1 | 0.17 |
| SPI | CLK_SPI | 0.07 | 0.11 |


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## 10.3 BOD and band gap static characteristics

**Table 12. BOD static characteristics[1]**

*$T_{amb}$ = 25 °C; simulated values for nominal processing.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{th}$ | threshold voltage | interrupt level 0 | | | | | |
| | | assertion | | - | 2.75 | - | V |
| | | de-assertion | | - | 2.92 | - | V |
| | | interrupt level 1 | | | | | |
| | | assertion | | - | 2.85 | - | V |
| | | de-assertion | | - | 3.00 | - | V |
| | | interrupt level 2 | | | | | |
| | | assertion | | - | 2.95 | - | V |
| | | de-assertion | | - | 3.12 | - | V |
| | | interrupt level 3 | | | | | |
| | | assertion | | - | 3.05 | - | V |
| | | de-assertion | | - | 3.19 | - | V |
| | | reset level 0 | | | | | |
| | | assertion | | - | 1.70 | - | V |
| | | de-assertion | | - | 1.85 | - | V |
| | | reset level 1 | | | | | |
| | | assertion | | - | 1.80 | - | V |
| | | de-assertion | | - | 1.95 | - | V |
| | | reset level 2 | | | | | |
| | | assertion | | - | 1.90 | - | V |
| | | de-assertion | | - | 2.05 | - | V |
| | | reset level 3 | | | | | |
| | | assertion | | - | 2.00 | - | V |
| | | de-assertion | | - | 2.15 | - | V |

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see *the LPC43xx user manual*.

**Table 13. Band gap characteristics**

*$V_{DDA(3V3)}$ over specified ranges; $T_{amb}$ = −40 °C to +105 °C; unless otherwise specified*

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ref(bg)}$ | band gap reference voltage | [1] | 0.621 | 0.6425 | 0.664 | mV |

[1] Based on characterization, not tested in production.


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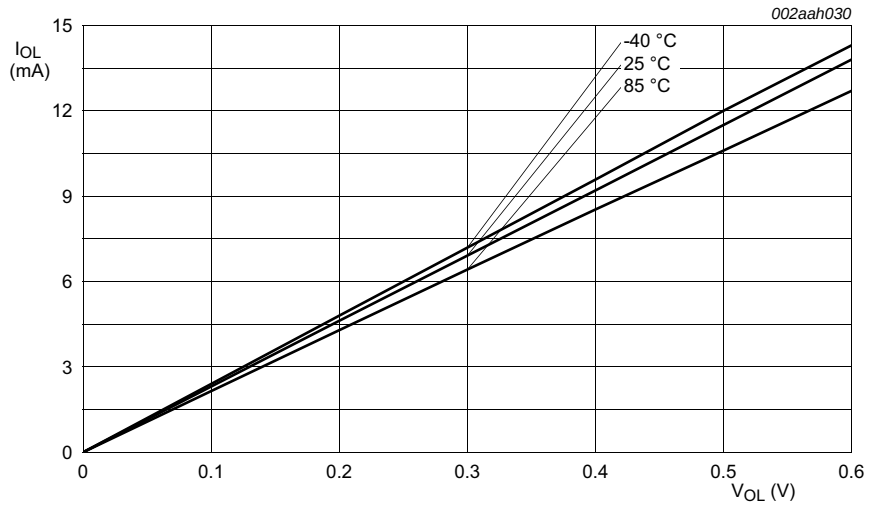
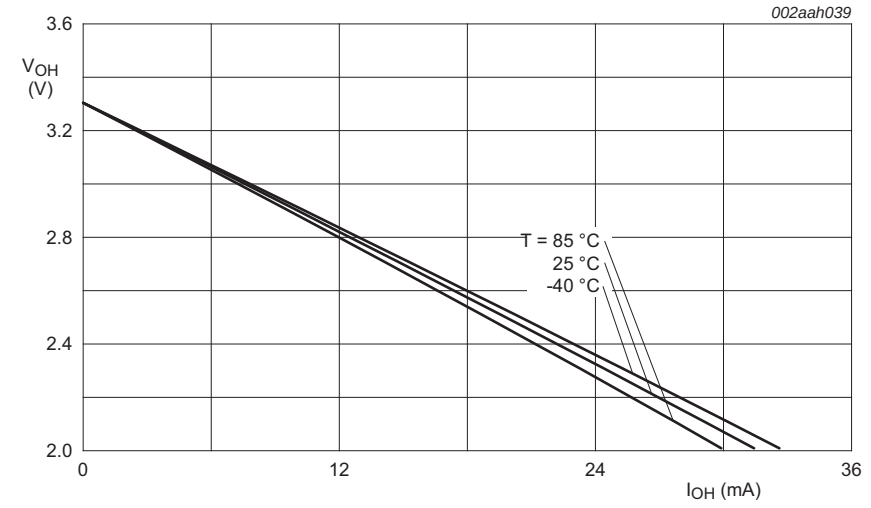
## 10.4 Electrical pin characteristics




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

**Fig 20. Normal-drive pins; typical LOW level output current $I_{OL}$ versus LOW level output voltage $V_{OL}$**




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

**Fig 21. Normal-drive pins; typical HIGH level output voltage $V_{OL}$ versus HGH level output current $I_{OH}$**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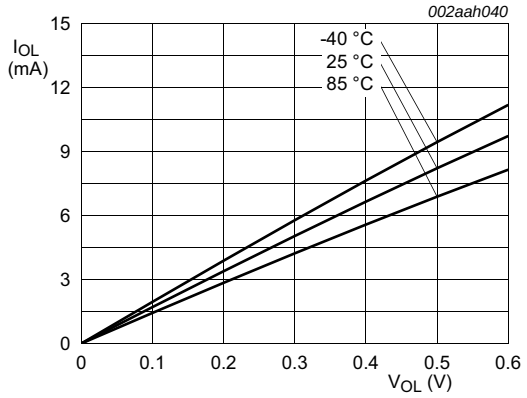
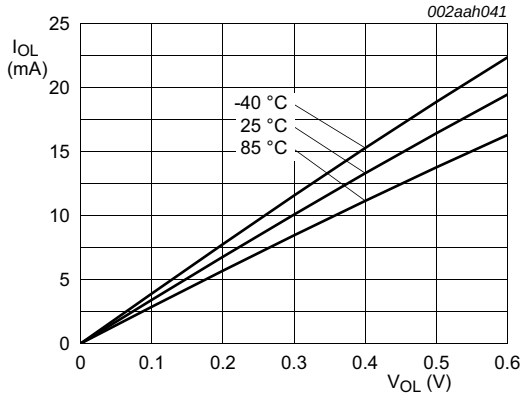
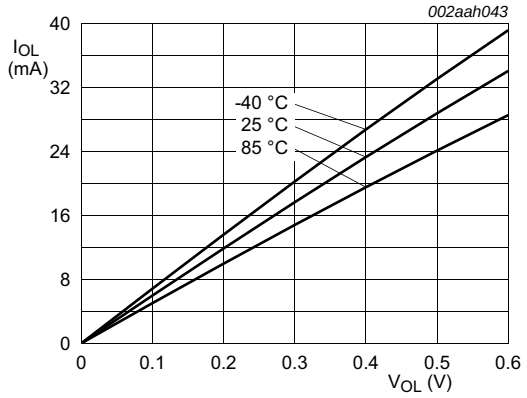


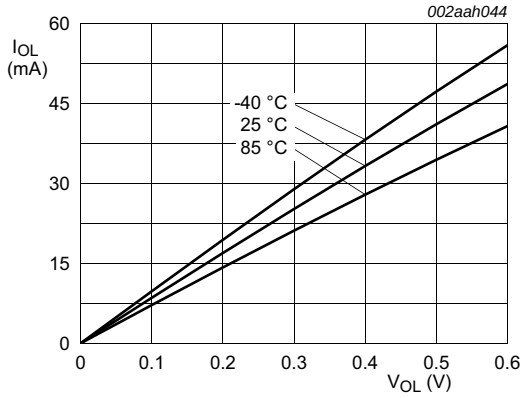

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

**Fig 22. High-drive pins; typical LOW level output current $I_{OL}$ versus LOW level output voltage $V_{OL}$**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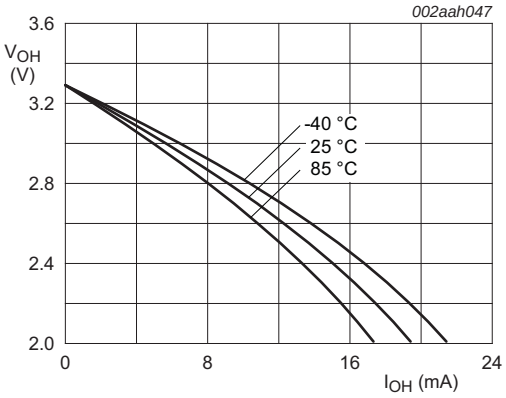
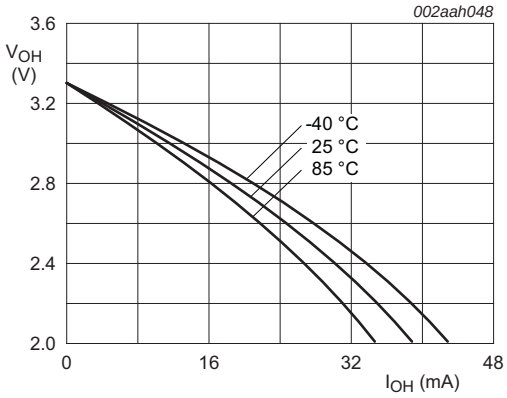
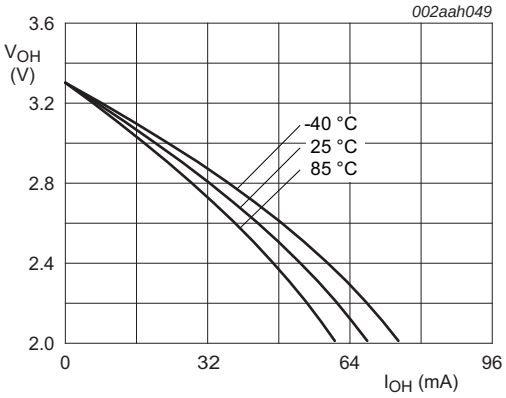


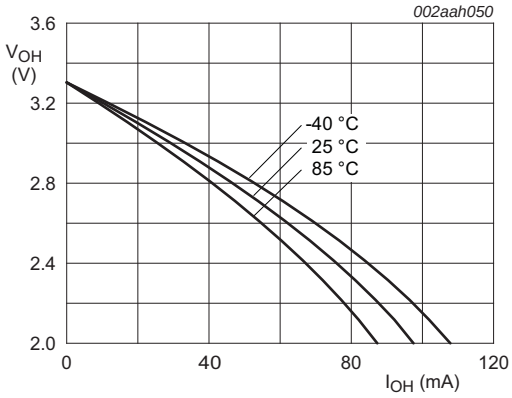

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

**Fig 23. High-drive pins; typical HIGH level output voltage $V_{OH}$ versus HGH level output current $I_{OH}$**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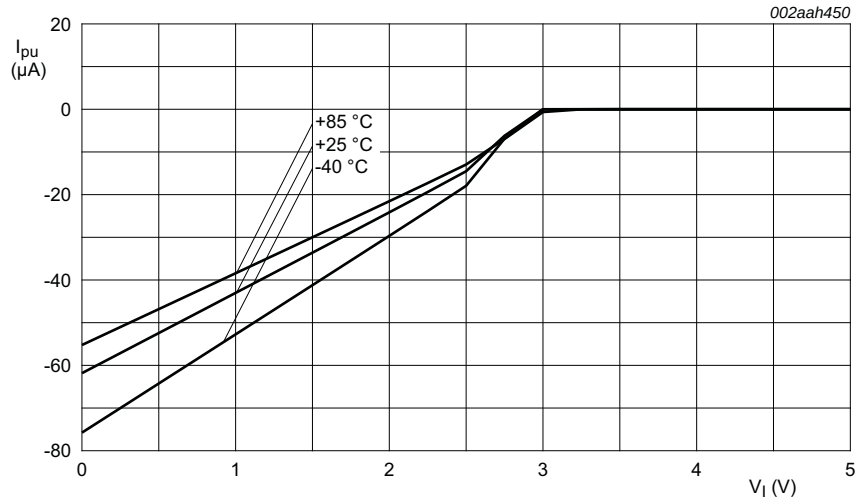
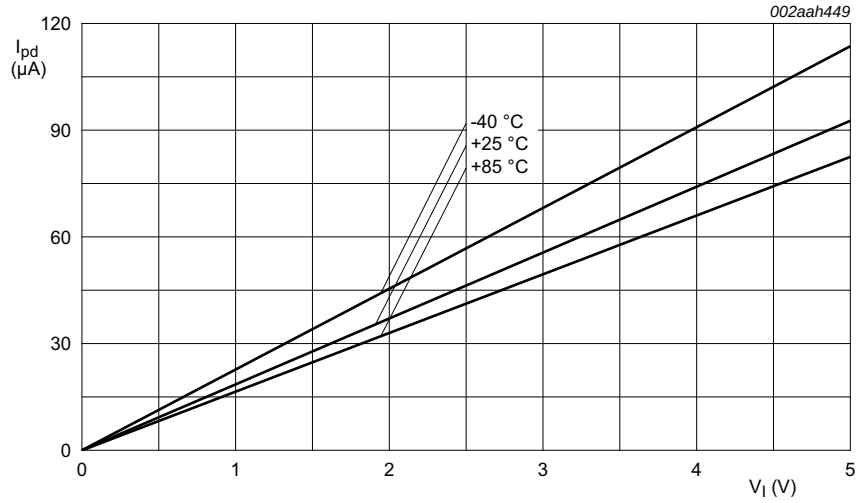



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated values.

**Fig 24. Typical pull-up current $I_{pu}$ versus input voltage $V_I$**




Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated values.

**Fig 25. Typical pull-down current $I_{pd}$ versus input voltage $V_I$**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# 11. Dynamic characteristics

## 11.1 Wake-up times

**Table 14. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes**

$T_{amb}$ = −40 °C to +85 °C

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{wake}$ | wake-up time | from Sleep mode | [2] | 3 × $T_{cy(clk)}$ | 5 × $T_{cy(clk)}$ | - | ns |
| | | from Deep-sleep and Power-down mode | | 12 | 51 | - | µs |
| | | from Deep power-down mode | | - | 250 | - | µs |
| | | after reset | | - | 250 | - | µs |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

## 11.2 External clock for oscillator in slave mode

**Remark:** The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 10). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

**Table 15. Dynamic characteristic: external clock**

$T_{amb}$ = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges.[1]

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | | | 1 | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | | 40 | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | | $T_{cy(clk)}$ × 0.4 | $T_{cy(clk)}$ × 0.6 | ns |
| $t_{CLCX}$ | clock LOW time | | | $T_{cy(clk)}$ × 0.4 | $T_{cy(clk)}$ × 0.6 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

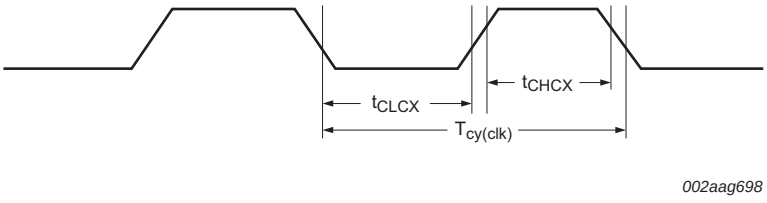


**Fig 26. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**


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## 11.3 Crystal oscillator

**Table 16. Dynamic characteristic: oscillator**

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.*[1]

| Symbol | Parameter | Conditions | | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Low-frequency mode (1 MHz - 20 MHz)**[5] | | | | | | | |
| $t_{jit(per)}$ | period jitter time | 5 MHz crystal | [3][4] | - | 13.2 | - | ps |
| | | 10 MHz crystal | | - | 6.6 | - | ps |
| | | 15 MHz crystal | | - | 4.8 | - | ps |
| **High-frequency mode (20 MHz - 25 MHz)**[6] | | | | | | | |
| $t_{jit(per)}$ | period jitter time | 20 MHz crystal | [3][4] | - | 4.3 | - | ps |
| | | 25 MHz crystal | | - | 3.7 | - | ps |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

## 11.4 IRC oscillator

**Table 17. Dynamic characteristic: IRC oscillator**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.*[1]

| Symbol | Parameter | Conditions | | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | | 11.82 | 12.0 | 12.18 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

## 11.5 RTC oscillator

**Table 18. Dynamic characteristic: RTC oscillator**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.2 V ≤ $V_{BAT}$ ≤ 3.6 V*[1]*; typical $C_{RTCX1/2}$ = 20 pF; also see Section 13.3.*

| Symbol | Parameter | Conditions | | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{i(RTC)}$ | RTC input frequency | - | | - | 32.768 | - | kHz |
| $I_{DD(RTC)}$ | RTC supply current | | | | 280 | 800 | nA |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.


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## 11.6 GPCLKIN

**Table 19. Dynamic characteristic: GPCLKIN**

$T_{amb}$ = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GP_CLKIN | input frequency | - | - | 25 | MHz |

## 11.7 I/O pins

**Table 20. Dynamic characteristic: I/O pins[1]**

$T_{amb}$ = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Standard I/O pins - normal drive strength** | | | | | | | |
| $t_r$ | rise time | pin configured as output; EHS = 1 | [2][3] | 1.0 | - | 2.5 | ns |
| $t_f$ | fall time | pin configured as output; EHS = 1 | [2][3] | 0.9 | - | 2.5 | ns |
| $t_r$ | rise time | pin configured as output; EHS = 0 | [2][3] | 1.9 | - | 4.3 | ns |
| $t_f$ | fall time | pin configured as output; EHS = 0 | [2][3] | 1.9 | - | 4.0 | ns |
| $t_r$ | rise time | pin configured as input | [4] | 0.3 | - | 1.3 | ns |
| $t_f$ | fall time | pin configured as input | [4] | 0.2 | - | 1.2 | ns |
| **I/O pins - high drive strength** | | | | | | | |
| $t_r$ | rise time | pin configured as output; standard drive mode (EHD = 0x0) | [2][5] | 4.3 | - | 7.9 | ns |
| $t_f$ | fall time | pin configured as output; standard drive mode (EHD = 0x0) | [2][5] | 4.7 | - | 8.7 | ns |
| $t_r$ | rise time | pin configured as output; medium drive mode (EHD = 0x1) | [2][5] | 3.2 | - | 5.7 | ns |
| $t_f$ | fall time | pin configured as output; medium drive mode (EHD = 0x1) | [2][5] | 3.2 | - | 5.5 | ns |
| $t_r$ | rise time | pin configured as output; high drive mode (EHD = 0x2) | [2][5] | 2.9 | - | 4.9 | ns |
| $t_f$ | fall time | pin configured as output; high drive mode (EHD = 0x2) | [2][5] | 2.5 | - | 3.9 | ns |
| $t_r$ | rise time | pin configured as output; ultra-high drive mode (EHD = 0x3) | [2][5] | 2.8 | - | 4.7 | ns |
| $t_f$ | fall time | pin configured as output; ultra-high drive mode (EHD = 0x3) | [2][5] | 2.4 | - | 3.4 | ns |
| $t_r$ | rise time | pin configured as input | [4] | 0.3 | - | 1.3 | ns |
| $t_f$ | fall time | pin configured as input | [4] | 0.2 | - | 1.2 | ns |
| **I/O pins - high-speed** | | | | | | | |
| $t_r$ | rise time | pin configured as output; EHS = 1 | [2][3] | 350 | - | 670 | ps |
| $t_f$ | fall time | pin configured as output; EHS = 1 | [2][3] | 450 | - | 730 | ps |
| $t_r$ | rise time | pin configured as output; EHS = 0 | [2][3] | 1.0 | - | 1.9 | ns |
| $t_f$ | fall time | pin configured as output; EHS = 0 | [2][3] | 1.0 | - | 2.0 | ns |
| $t_r$ | rise time | pin configured as input | [4] | 0.3 | - | 1.3 | ns |
| $t_f$ | fall time | pin configured as input | [4] | 0.2 | - | 1.2 | ns |

[1] Simulated data.


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[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the system control block in the SFSP registers using the EHS bit. See the LPC43xx user manual.

[4] $C_L$ = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

[5] The drive modes are configured in the system control block in the SFSP registers using the EHD bit. See the LPC43xx user manual.

## 11.8 I²C-bus

**Table 21. Dynamic characteristic: I²C-bus pins**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.*[1]

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time | [3][4][5][6] | of both SDA and SCL signals<br>Standard-mode | - | 300 | ns |
| | | | Fast-mode | 20 + 0.1 × $C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [2][3][7] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [8][9] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[2] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] $C_b$ = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.


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[9] A Fast-mode $I^2C$-bus device can be used in a Standard-mode $I^2C$-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode $I^2C$-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

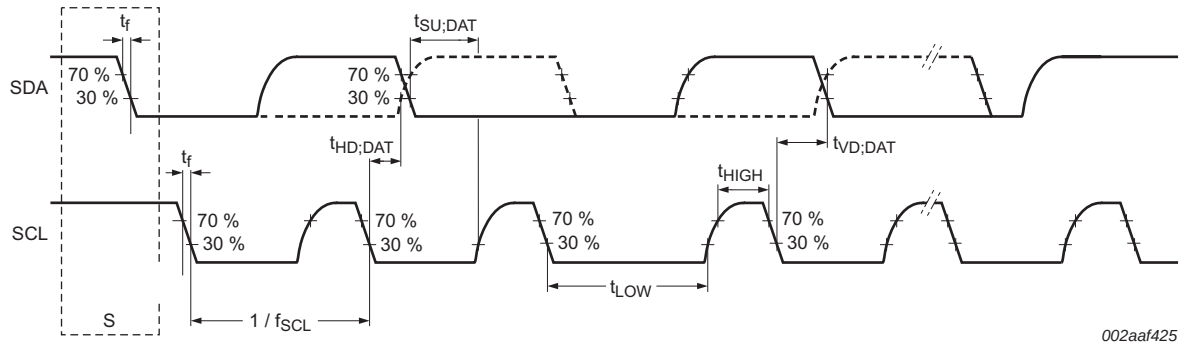


**Fig 27. $I^2C$-bus pins clock timing**

## 11.9 $I^2S$-bus interface

**Table 22. Dynamic characteristics: $I^2S$-bus interface pins**

*$T_{amb}$ = −40 °C to +85 °C ; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **common to input and output** | | | | | | | |
| $t_r$ | rise time | | | - | 4 | - | ns |
| $t_f$ | fall time | | | - | 4 | - | ns |
| $t_{WH}$ | pulse width HIGH | on pins I2Sx_TX_SCK and I2Sx_RX_SCK | | 36 | - | - | ns |
| $t_{WL}$ | pulse width LOW | on pins I2Sx_TX_SCK and I2Sx_RX_SCK | | 36 | - | - | ns |
| **output** | | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin I2Sx_TX_SDA | [1] | - | 4.4 | - | ns |
| | | on pin I2Sx_TX_WS | | - | 4.3 | - | ns |
| **input** | | | | | | | |
| $t_{su(D)}$ | data input set-up time | on pin I2Sx_RX_SDA | [1] | - | 0 | - | ns |
| | | on pin I2Sx_RX_WS | | | 0.20 | | ns |
| $t_{h(D)}$ | data input hold time | on pin I2Sx_RX_SDA | [1] | - | 3.7 | - | ns |
| | | on pin I2Sx_RX_WS | | - | 3.9 | - | ns |

[1] Clock to the $I^2S$-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the $I^2S$-bus interface PCLK = BASE_APB1_CLK / 12. $I^2S$ clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *$I^2S$-bus specification*.


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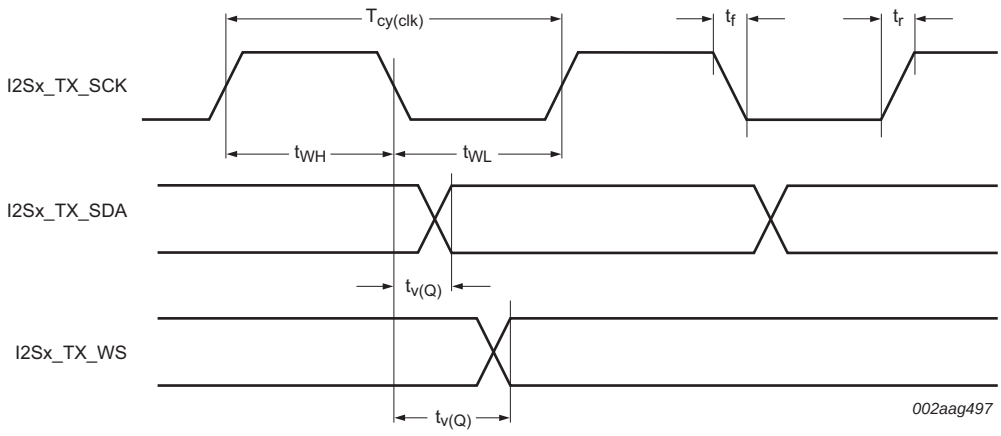


**Fig 28. I²S-bus (transmit)**

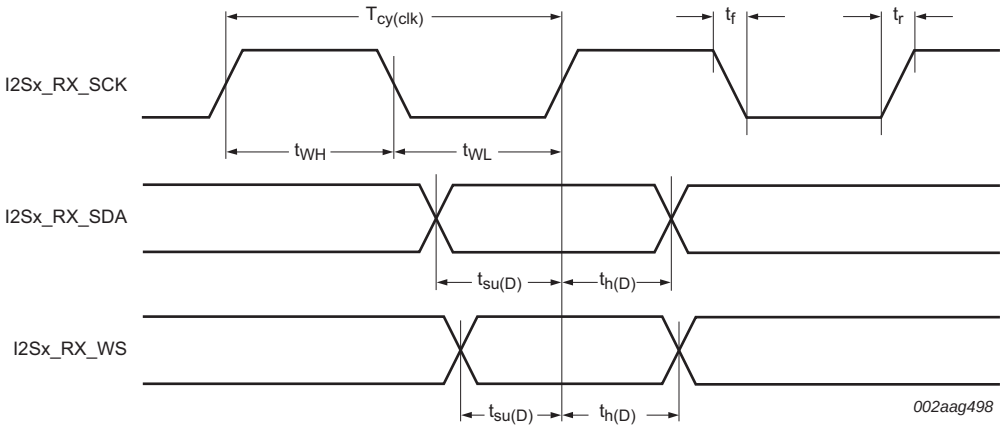


**Fig 29. I²S-bus timing (receive)**

## 11.10 USART interface

**Table 23. USART dynamic characteristics**

*$T_{amb}$ = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. EHS = 1 for all pins. Simulated values.*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| **USART master (in synchronous mode)** | | | | |
| $t_{su(D)}$ | data input set-up time | 26.6 | - | ns |
| $t_{h(D)}$ | data input hold time | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | 0 | 8.8 | ns |
| **USART slave (in synchronous mode)** | | | | |
| $t_{su(D)}$ | data input set-up time | 1.2 | - | ns |
| $t_{h(D)}$ | data input hold time | 0.4 | - | ns |
| $t_{v(Q)}$ | data output valid time | 5.5 | 24 | ns |


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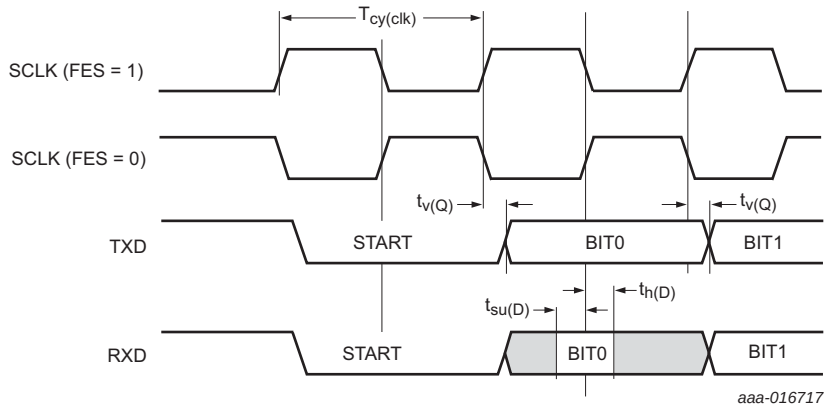


**Fig 30. USART timing**


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## 11.11 SSP interface

**Table 24. Dynamic characteristics: SSP pins in SPI mode**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SSP master** | | | | | | | |
| $T_{cy(clk)}$ | clock cycle time | full-duplex mode | [1] | $1/(25.5 \times 10^6)$ | - | - | s |
| | | when only transmitting | | $1/(51 \times 10^6)$ | - | - | s |
| $t_{DS}$ | data set-up time | in SPI mode | | 13.6 | - | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | | −3.8 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | | - | - | 6.0 | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | | −1.1 | - | - | ns |
| $t_{lead}$ | lead time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | $T_{cy(clk)} + 3.2$ | - | $T_{cy(clk)} + 6.1$ | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | $0.5 \times T_{cy(clk)} + 3.2$ | - | $0.5 \times T_{cy(clk)} + 6.1$ | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | $T_{cy(clk)} + 3.2$ | - | $T_{cy(clk)} + 6.1$ | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | $0.5 \times T_{cy(clk)} + 3.2$ | - | $0.5 \times T_{cy(clk)} + 6.1$ | ns |
| | | synchronous serial frame mode | | $0.5 \times T_{cy(clk)} + 3.2$ | - | $0.5 \times T_{cy(clk)} + 6.1$ | ns |
| | | microwire frame format | | $T_{cy(clk)} + 3.2$ | - | $T_{cy(clk)} + 6.1$ | ns |
| $t_{lag}$ | lag time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | $0.5 \times T_{cy(clk)}$ | - | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | $T_{cy(clk)}$ | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | $0.5 \times T_{cy(clk)}$ | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | $T_{cy(clk)}$ | - | - | ns |
| | | synchronous serial frame mode | | $T_{cy(clk)}$ | - | - | ns |
| | | microwire frame format | | $0.5 \times T_{cy(clk)}$ | - | - | ns |


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**Table 24. Dynamic characteristics: SSP pins in SPI mode**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_d$ | delay time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | - | 0.5 × $T_{cy(clk)}$ | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | - | n/a | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | - | 0.5 × $T_{cy(clk)}$ | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | - | n/a | - | ns |
| | | synchronous serial frame mode | | - | $T_{cy(clk)}$ | - | ns |
| | | microwire frame format | | - | n/a | - | ns |
| **SSP slave** | | | | | | | |
| PCLK | Peripheral clock frequency | | | - | - | 204 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | [2] | 1/(11 × $10^6$) | - | - | s |
| $t_{DS}$ | data set-up time | in SPI mode | | 1.15 | - | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | | 0.5 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | | - | - | [4 × (1/PCLK)] + 3 | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | | 5.1 | - | - | ns |
| $t_{lead}$ | lead time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | $T_{cy(clk)}$ + 2.2 | - | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | 0.5 × $T_{cy(clk)}$ + 2.2 | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | $T_{cy(clk)}$ + 2.2 | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | 0.5 × $T_{cy(clk)}$ + 2.2 | - | - | ns |
| | | synchronous serial frame mode | | 0.5 × $T_{cy(clk)}$ + 2.2 | - | - | ns |
| | | microwire frame format | | $T_{cy(clk)}$ + 2.2 | - | - | ns |


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**Table 24. Dynamic characteristics: SSP pins in SPI mode**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{lag}$ | lag time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | $0.5T_{cy(clk)}$ + 0.2 | - | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | $T_{cy(clk)}$ + 0.2 | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | 0.5 × $T_{cy(clk)}$ + 0.2 | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | $T_{cy(clk)}$ + 0.2 | - | - | ns |
| | | synchronous serial frame mode | | $T_{cy(clk)}$ + 0.2 | - | - | ns |
| | | microwire frame format | | 0.5 × $T_{cy(clk)}$ | - | - | ns |
| $t_d$ | delay time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | - | 0.5 × $T_{cy(clk)}$ | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | - | n/a | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | - | 0.5 × $T_{cy(clk)}$ | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | - | n/a | - | ns |
| | | synchronous serial frame mode | | - | $T_{cy(clk)}$ | - | ns |
| | | microwire frame format | | - | n/a | - | ns |

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / $f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency $f_{main}$, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.


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## 11.12 SPI interface

**Table 25. Dynamic characteristics: SPI**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $T_{cy(PCLK)}$ | PCLK cycle time | | | 5 | | | ns |
| $T_{cy(clk)}$ | clock cycle time | | [1] | 40 | - | - | ns |
| **Master** | | | | | | | |
| $t_{DS}$ | data set-up time | | | 7.2 | - | - | ns |
| $t_{DH}$ | data hold time | | | 0 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | | | - | - | 3.7 | ns |
| $t_{h(Q)}$ | data output hold time | | | - | - | 1.2 | ns |
| **Slave** | | | | | | | |
| $t_{DS}$ | data set-up time | | | 1.2 | - | - | ns |
| $t_{DH}$ | data hold time | | | $3 \times T_{cy(PCLK)} + 0.54$ | - | - | ns |
| $t_{v(Q)}$ | data output valid time | | | - | - | $3 \times T_{cy(PCLK)} + 9.7$ | ns |
| $t_{h(Q)}$ | data output hold time | | | - | - | $2 \times T_{cy(PCLK)} + 7.1$ | ns |

[1] $T_{cy(clk)}$ = 8/BASE_SPI_CLK. $T_{cy(PCLK)}$ = 1/BASE_SPI_CLK.


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## 11.13 SSP/SPI timing diagrams

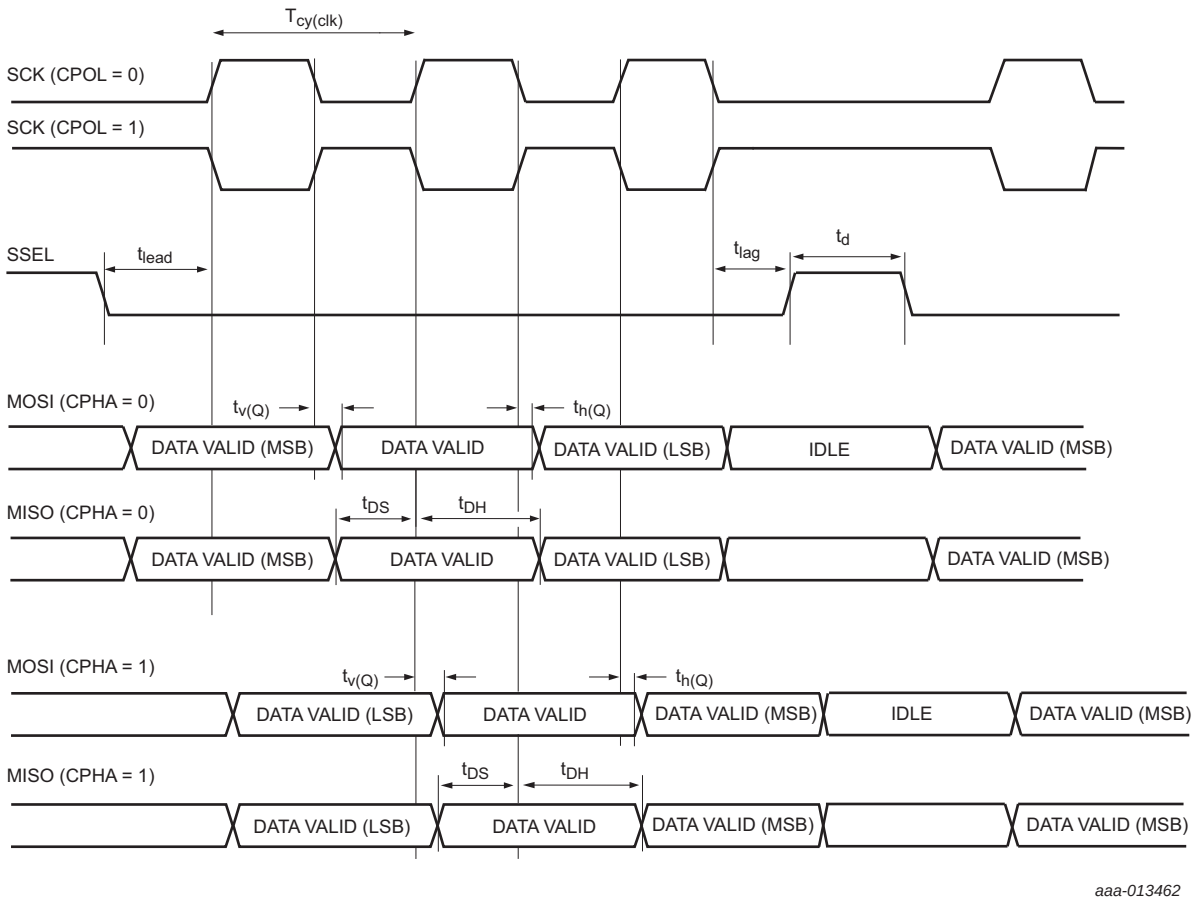


**Fig 31. SSP master mode timing (SPI mode)**


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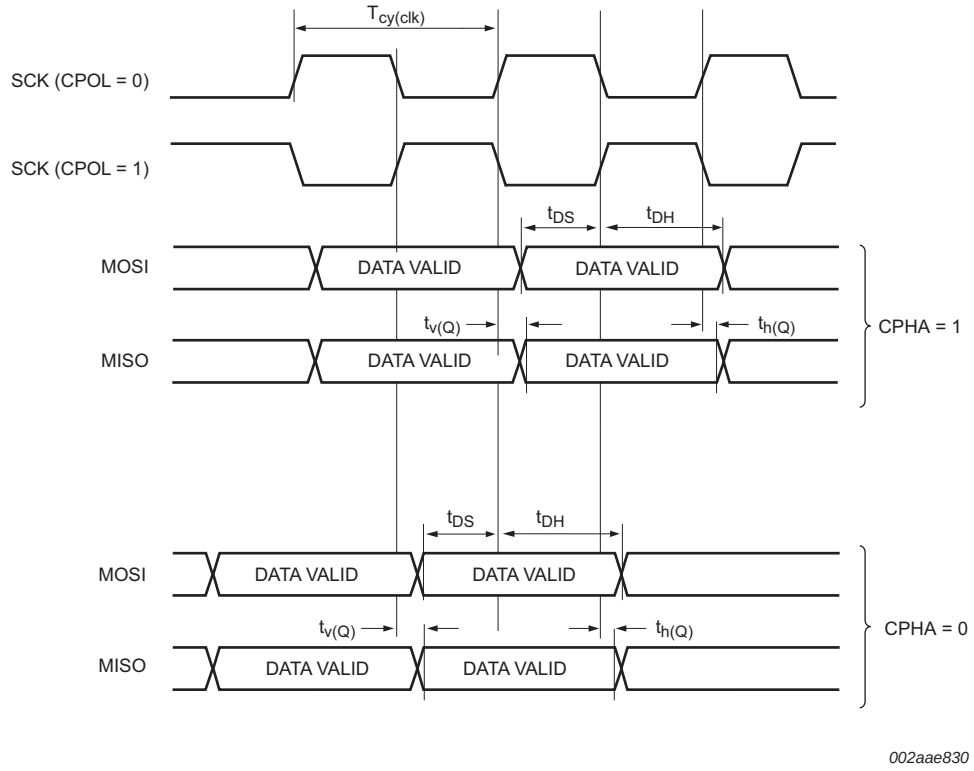


**Fig 32. SSP slave mode timing (SPI mode)**

## 11.14 SGPIO timing

The following considerations apply to SGPIO timing:

- SGPIO input signals are synchronized by the internal clock SGPIO_CLOCK. To guarantee that no samples are missed, all input signals should have a duration of at least one SGPIO_CLOCK cycle plus the set-up and hold times.
- When an external clock input is used to generate output data, synchronization causes a latency of at least one SGPIO_CLOCK cycle. The maximum output data rate is one output every two SGPIO_CLOCK cycles.
- Synchronization also causes a latency of one SGPIO_CLOCK cycle when sampling several inputs. This may cause inputs with very similar timings to be sampled with a difference of one SGPIO_CLOCK cycle.


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**Table 26. Dynamic characteristics: SGPIO**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{su(D)}$ | data input set-up time | | | 2 | - | - | ns |
| $t_{h(D)}$ | data input hold time | | [1] | $T_{SGPIO}$ + 2 | - | - | ns |
| $t_{su(D)}$ | data input set-up time | sampled by SGPIO_CLOCK | [1] | $T_{SGPIO}$ + 2 | - | - | ns |
| $t_{h(D)}$ | data input hold time | sampled by SGPIO_CLOCK | [1] | $T_{SGPIO}$ + 2 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | | [1] | - | - | 2 × $T_{SGPIO}$ | ns |
| $t_{h(Q)}$ | data output hold time | | [1] | $T_{SGPIO}$ | - | | ns |
| $t_{v(Q)}$ | data output valid time | sampled by SGPIO_CLOCK | [1] | −3 | - | 3 | ns |
| $t_{h(Q)}$ | data output hold time | sampled by SGPIO_CLOCK | [1] | −3 | - | 3 | ns |

[1] SGPIO_CLOCK is the internally generated SGPIO clock. $T_{SGPIO} = 1/f_{SGPIO_CLOCK}$.

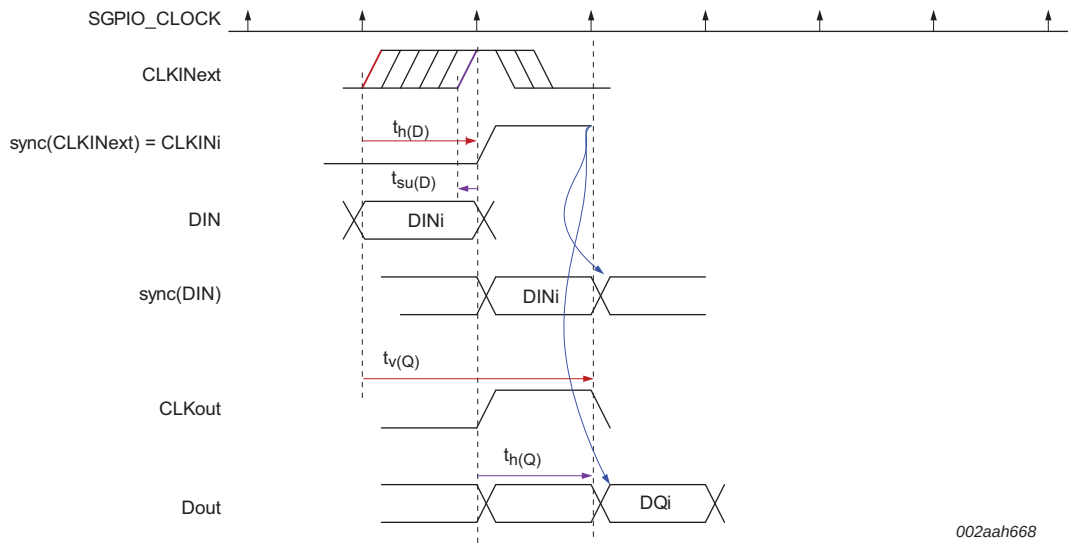


**Fig 33. SGPIO timing**


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## 11.15 External memory interface

**Table 27. Dynamic characteristics: Static asynchronous external memory interface**

*$C_L$ = 22 pF for EMC_Dn $C_L$ = 20 pF for all others; $T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.*

| Symbol | Parameter[1] | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Read cycle parameters** | | | | | | | |
| $t_{CSLAV}$ | $\overline{CS}$ LOW to address valid time | | | −3.1 | - | 1.6 | ns |
| $t_{CSLOEL}$ | $\overline{CS}$ LOW to $\overline{OE}$ LOW time | | [2] | −0.6 + $T_{cy(clk)}$ × WAITOEN | - | 1.3 + $T_{cy(clk)}$ × WAITOEN | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW time | PB = 1 | | −0.7 | - | 1.8 | ns |
| $t_{OELOEH}$ | $\overline{OE}$ LOW to $\overline{OE}$ HIGH time | | [2] | −0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ | - | −0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{am}$ | memory access time | | | - | - | −16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$ | ns |
| $t_{h(D)}$ | data input hold time | | | −16 | - | - | ns |
| $t_{CSHBLSH}$ | $\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time | PB = 1 | | −0.4 | - | 1.9 | ns |
| $t_{CSHOEH}$ | CS HIGH to $\overline{OE}$ HIGH time | | | −0.4 | - | 1.4 | ns |
| $t_{OEHANV}$ | $\overline{OE}$ HIGH to address invalid | PB = 1 | | −2.0 | - | 2.6 | ns |
| $t_{CSHEOR}$ | $\overline{CS}$ HIGH to end of read time | | [3] | −2.0 | - | 0 | ns |
| $t_{CSLSOR}$ | $\overline{CS}$ LOW to start of read time | | [4] | 0 | - | 1.8 | ns |
| **Write cycle parameters** | | | | | | | |
| $t_{CSLAV}$ | $\overline{CS}$ LOW to address valid time | | | −3.1 | - | 1.6 | ns |
| $t_{CSLDV}$ | $\overline{CS}$ LOW to data valid time | | | −3.1 | - | 1.5 | ns |
| $t_{CSLWEL}$ | $\overline{CS}$ LOW to $\overline{WE}$ LOW time | PB = 1 | | −1.5 + (WAITWEN + 1) × $T_{cy(clk)}$ | - | 0.2 + (WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW time | PB = 1 | | −0.7 | - | 1.8 | ns |
| $t_{WELWEH}$ | $\overline{WE}$ LOW to $\overline{WE}$ HIGH time | PB = 1 | [2] | −0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ | - | −0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{WEHDNV}$ | $\overline{WE}$ HIGH to data invalid time | PB = 1 | [2] | −0.9 + $T_{cy(clk)}$ | - | 2.3 + $T_{cy(clk)}$ | ns |
| $t_{WEHEOW}$ | $\overline{WE}$ HIGH to end of write time | PB = 1 | [2] [5] | −0.4 + $T_{cy(clk)}$ | - | −0.3 + $T_{cy(clk)}$ | ns |
| $t_{CSLBLSL}$ | $\overline{CS}$ LOW to $\overline{BLS}$ LOW | PB = 0 | | −0.7 + (WAITWEN + 1) × $T_{cy(clk)}$ | - | 1.8 + (WAITWEN + 1) × $T_{cy(clk)}$ | ns |


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**Table 27. Dynamic characteristics: Static asynchronous external memory interface** *…continued*

*$C_L$ = 22 pF for EMC_Dn $C_L$ = 20 pF for all others; $T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.*

| Symbol | Parameter[1] | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{BLSLBLSH}$ | $\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time | PB = 0 | [2] | −0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ | - | −0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{BLSHEOW}$ | $\overline{BLS}$ HIGH to end of write time | PB = 0 | [2] [5] | −1.9 + $T_{cy(clk)}$ | - | −0.5 + $T_{cy(clk)}$ | ns |
| $t_{BLSHDNV}$ | $\overline{BLS}$ HIGH to data invalid time | PB = 0 | [1] [2] | −2.5 + $T_{cy(clk)}$ | - | 1.4 + $T_{cy(clk)}$ | ns |
| $t_{CSHEOW}$ | $\overline{CS}$ HIGH to end of write time | | [5] | −2.0 | - | 0 | ns |
| $t_{BLSHDNV}$ | $\overline{BLS}$ HIGH to data invalid time | PB = 1 | | −2.5 | - | 1.4 | ns |
| $t_{WEHANV}$ | WE HIGH to address invalid time | PB = 1 | | −0.9 + $T_{cy(clk)}$ | - | 2.4 + $T_{cy(clk)}$ | ns |

[1] Parameters specified for 40 % of $V_{DD(IO)}$ for rising edges and 60 % of $V_{DD(IO)}$ for falling edges.

[2] $T_{cy(clk)}$ = 1/CCLK (see LPC43xx User manual).

[3] End Of Read (EOR): longest of $t_{CSHOEH}$, $t_{OEHANV}$, $t_{CSHBLSH}$.

[4] Start Of Read (SOR): longest of $t_{CSLAV}$, $t_{CSLOEL}$, $t_{CSLBLSL}$.

[5] End Of Write (EOW): earliest of address not valid or $\overline{EMC_BLSn}$ HIGH.

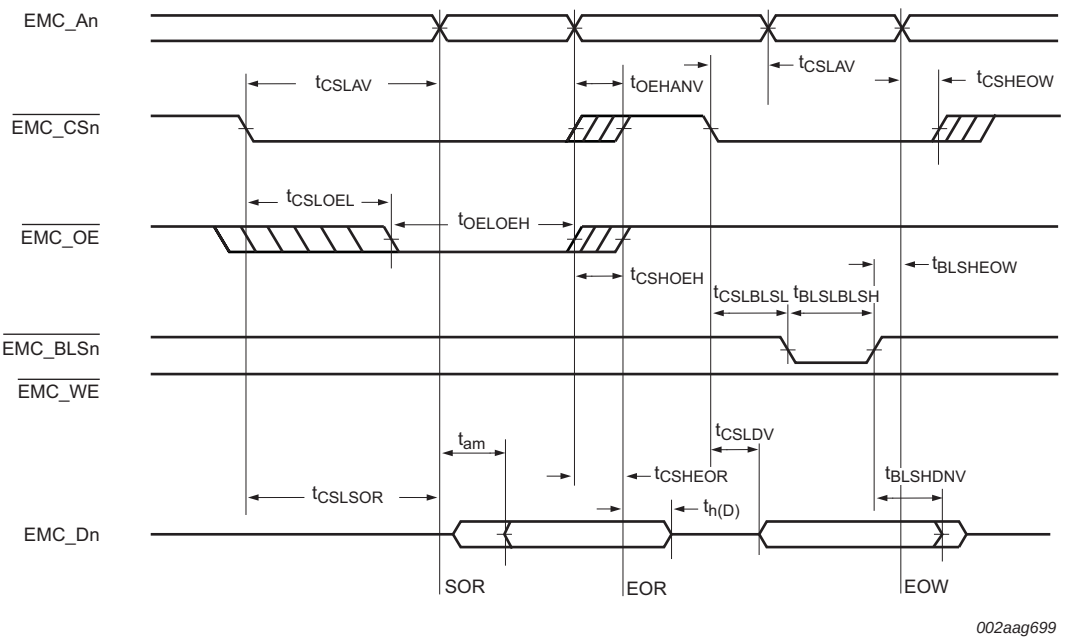


**Fig 34. External static memory read/write access (PB = 0)**


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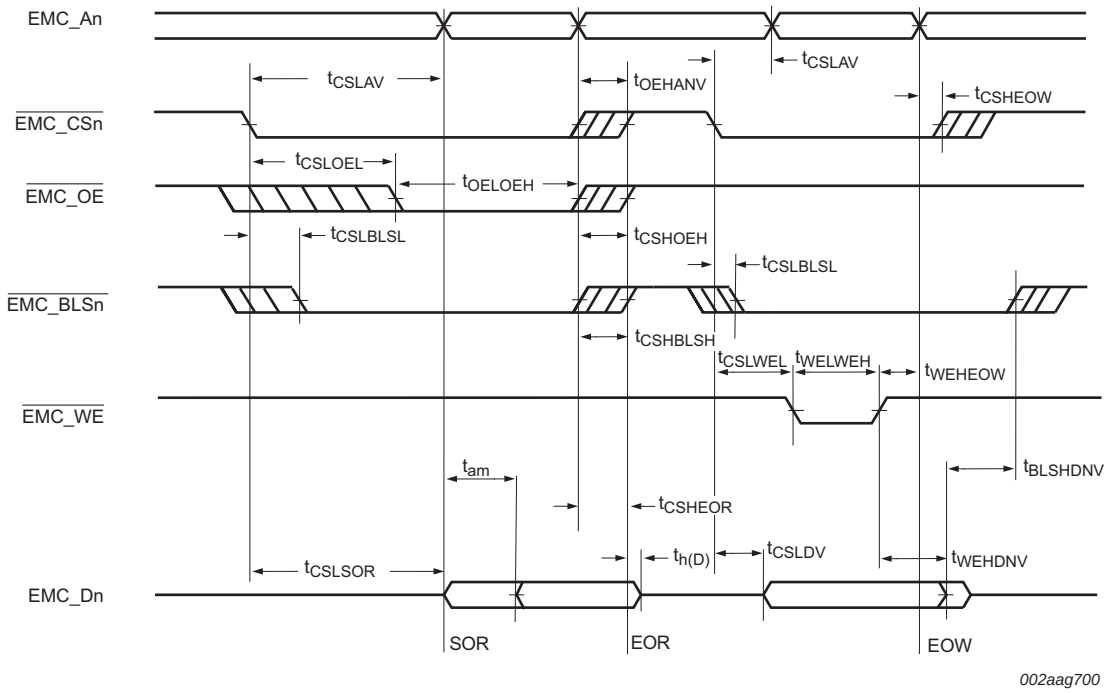


**Fig 35. External static memory read/write access (PB = 1)**


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**Table 28. Dynamic characteristics: Dynamic external memory interface**

*Simulated data over temperature and process range; $C_L$ = 10 pF for $\overline{EMC_DYCSn}$, $\overline{EMC_RAS}$, $\overline{EMC_CAS}$, $\overline{EMC_WE}$, EMC_An; $C_L$ = 9 pF for EMC_Dn; $C_L$ = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; $T_{amb}$ = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ = 3.3 V ± 10 %; RD = 1 (see LPC43xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{cy(clk)}$ | clock cycle time | 8.4 | - | - | ns |
| **Common to read and write cycles** | | | | | |
| $t_{d(DYCSV)}$ | DYCS delay time | - | 3.1 + 0.5 × $T_{cy(clk)}$ | 5.1 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(DYCS)}$ | DYCS hold time | 0.3 + 0.5 × $T_{cy(clk)}$ | 0.9 + 0.5 × $T_{cy(clk)}$ | - | ns |
| $t_{d(RASV)}$ | row address strobe valid delay time | - | 3.1 + 0.5 × $T_{cy(clk)}$ | 4.9 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(RAS)}$ | row address strobe hold time | 0.5 + 0.5 × $T_{cy(clk)}$ | 1.1 + 0.5 × $T_{cy(clk)}$ | - | ns |
| $t_{d(CASV)}$ | column address strobe valid delay time | - | 2.9 + 0.5 × $T_{cy(clk)}$ | 4.6 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(CAS)}$ | column address strobe hold time | 0.3 + 0.5 × $T_{cy(clk)}$ | 0.9 + 0.5 × $T_{cy(clk)}$ | - | ns |
| $t_{d(WEV)}$ | $\overline{WE}$ valid delay time | - | 3.2 + 0.5 × $T_{cy(clk)}$ | 5.9 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(WE)}$ | $\overline{WE}$ hold time | 1.3 + 0.5 × $T_{cy(clk)}$ | 1.4 + 0.5 × $T_{cy(clk)}$ | - | ns |
| $t_{d(DQMOUTV)}$ | DQMOUT valid delay time | - | 3.1 + 0.5 × $T_{cy(clk)}$ | 5.0 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(DQMOUT)}$ | DQMOUT hold time | 0.2 + 0.5 × $T_{cy(clk)}$ | 0.8 + 0.5 × $T_{cy(clk)}$ | - | ns |
| $t_{d(AV)}$ | address valid delay time | - | 3.8 + 0.5 × $T_{cy(clk)}$ | 6.3 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(A)}$ | address hold time | 0.3 + 0.5 × $T_{cy(clk)}$ | 0.9 + 0.5 × $T_{cy(clk)}$ | - | ns |
| $t_{d(CKEOUTV)}$ | CKEOUT valid delay time | - | 3.1 + 0.5 × $T_{cy(clk)}$ | 5.1 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(CKEOUT)}$ | CKEOUT hold time | 0.5 × $T_{cy(clk)}$ | 0.7 + 0.5 × $T_{cy(clk)}$ | - | ns |
| **Read cycle parameters** | | | | | |
| $t_{su(D)}$ | data input set-up time | −1.5 | −0.5 | - | ns |
| $t_{h(D)}$ | data input hold time | 2.2 | 0.8 | - | ns |
| **Write cycle parameters** | | | | | |
| $t_{d(QV)}$ | data output valid delay time | - | 3.8 + 0.5 × $T_{cy(clk)}$ | 6.2 + 0.5 × $T_{cy(clk)}$ | ns |
| $t_{h(Q)}$ | data output hold time | 0.5 × $T_{cy(clk)}$ | 0.7 + 0.5 × $T_{cy(clk)}$ | - | ns |

**Table 29. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values**

*$T_{amb}$ = −40 °C to 85 °C; $V_{DD(IO)}$ = 3.3 V ± 10 %; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_d$ | delay time | delay value | [1] | | | | |
| | | CLKn_DELAY = 0 | | 0.0 | 0.0 | 0.0 | ns |
| | | CLKn_DELAY = 1 | [1] | 0.4 | 0.5 | 0.8 | ns |
| | | CLKn_DELAY = 2 | [1] | 0.7 | 1.0 | 1.7 | ns |
| | | CLKn_DELAY = 3 | [1] | 1.1 | 1.6 | 2.5 | ns |
| | | CLKn_DELAY = 4 | [1] | 1.4 | 2.0 | 3.3 | ns |
| | | CLKn_DELAY = 5 | [1] | 1.7 | 2.6 | 4.1 | ns |
| | | CLKn_DELAY = 6 | [1] | 2.1 | 3.1 | 4.9 | ns |
| | | CLKn_DELAY = 7 | [1] | 2.5 | 3.6 | 5.8 | ns |

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC43xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.


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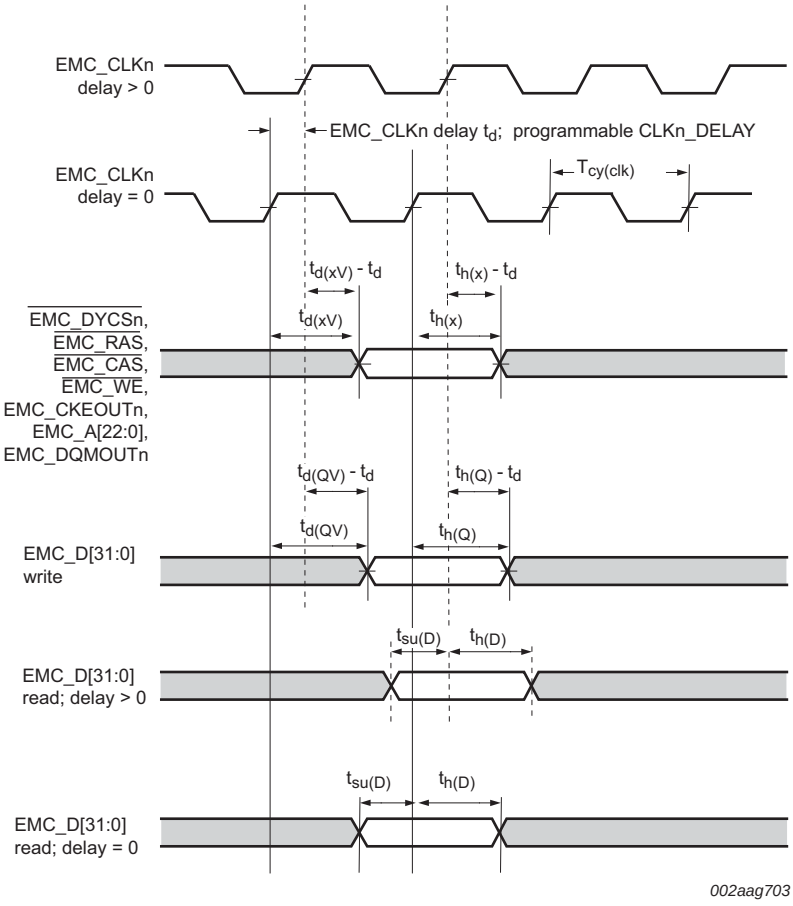


For the programmable EMC_CLK[3:0] clock delays CLKn_DELAY, see Table 29.

**Remark:** For SDRAM operation, set CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY in the EMCDELAYCLK register.

**Fig 36. SDRAM timing**


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## 11.16 USB interface

**Table 30. Dynamic characteristics: USB0 and USB1 pins (full-speed)**
*$C_L$ = 50 pF; $R_{pu}$ = 1.5 kΩ on D+ to $V_{DD(IO)}$; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_r$ | rise time | 10 % to 90 % | | 4 | - | 20 | ns |
| $t_f$ | fall time | 10 % to 90 % | | 4 | - | 20 | ns |
| $t_{FRFM}$ | differential rise and fall time matching | $t_r$ / $t_f$ | | 90 | - | 111.11 | % |
| $V_{CRS}$ | output signal crossover voltage | | | 1.3 | - | 2.0 | V |
| $t_{FEOPT}$ | source SE0 interval of EOP | see Figure 37 | | 160 | - | 175 | ns |
| $t_{FDEOP}$ | source jitter for differential transition to SE0 transition | see Figure 37 | | –2 | - | +5 | ns |
| $t_{JR1}$ | receiver jitter to next transition | | | –18.5 | - | +18.5 | ns |
| $t_{JR2}$ | receiver jitter for paired transitions | 10 % to 90 % | | –9 | - | +9 | ns |
| $t_{EOPR1}$ | EOP width at receiver | must reject as EOP; see Figure 37 | [1] | 40 | - | - | ns |
| $t_{EOPR2}$ | EOP width at receiver | must accept as EOP; see Figure 37 | [1] | 82 | - | - | ns |

[1] Characterized but not implemented as production test. Guaranteed by design.

**Remark:** If only USB0 (HS USB) is used, the pins VDDREG and VDDIO can be at different voltages within the operating range but should have the same ramp up time. If USB1(FS USB) is used, the pins VDDREG and VDDIO should be a minimum of 3.0 V and be tied together.

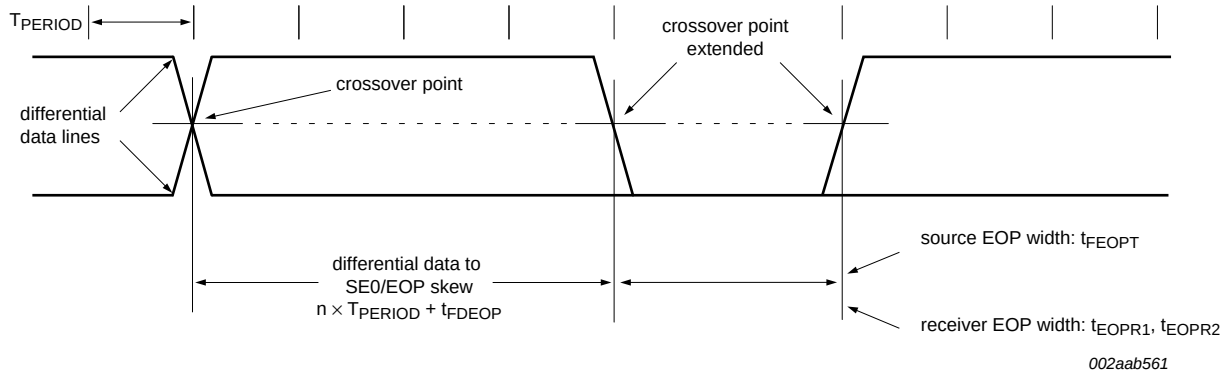


**Fig 37. Differential data-to-EOP transition skew and EOP width**


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**Table 31. Static characteristics: USB0 PHY pins[1]**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **High-speed mode** | | | | | | | |
| $P_{cons}$ | power consumption | | [2] | - | 68 | - | mW |
| $I_{DDA(3V3)}$ | analog supply current (3.3 V) | on pin USB0_VDDA3V3_DRIVER; | [3] | | | | |
| | | total supply current | | - | 18 | - | mA |
| | | during transmit | | - | 31 | - | mA |
| | | during receive | | - | 14 | - | mA |
| | | with driver tri-stated | | - | 14 | - | mA |
| $I_{DDD}$ | digital supply current | | | - | 7 | - | mA |
| **Full-speed/low-speed mode** | | | | | | | |
| $P_{cons}$ | power consumption | | [2] | - | 15 | - | mW |
| $I_{DDA(3V3)}$ | analog supply current (3.3 V) | on pin USB0_VDDA3V3_DRIVER; | | | | | |
| | | total supply current | | - | 3.5 | - | mA |
| | | during transmit | | - | 5 | - | mA |
| | | during receive | | - | 3 | - | mA |
| | | with driver tri-stated | | - | 3 | - | mA |
| $I_{DDD}$ | digital supply current | | | - | 3 | - | mA |
| **Suspend mode** | | | | | | | |
| $I_{DDA(3V3)}$ | analog supply current (3.3 V) | | | - | 24 | - | µA |
| | | with driver tri-stated | | - | 24 | - | µA |
| | | with OTG functionality enabled | | - | 3 | - | mA |
| $I_{DDD}$ | digital supply current | | | - | 30 | - | µA |
| **VBUS detector outputs** | | | | | | | |
| $V_{th}$ | threshold voltage | for VBUS valid | | 4.4 | - | - | V |
| | | for session end | | 0.2 | - | 0.8 | V |
| | | for A valid | | 0.8 | - | 2 | V |
| | | for B valid | | 2 | - | 4 | V |
| $V_{hys}$ | hysteresis voltage | for session end | | - | 150 | 10 | mV |
| | | A valid | | - | 200 | 10 | mV |
| | | B valid | | - | 200 | 10 | mV |

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

## 11.17 Ethernet

**Remark:** The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.


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**Table 32. Dynamic characteristics: Ethernet**

*$T_{amb}$ = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **RMII mode** | | | | | | |
| $f_{clk}$ | clock frequency | for ENET_RX_CLK | [1] | - | 50 | MHz |
| $\delta_{clk}$ | clock duty cycle | | [1] | 50 | 50 | % |
| $t_{su}$ | set-up time | for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV | [1][2] | 4 | - | ns |
| $t_h$ | hold time | for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV | [1][2] | 2 | - | ns |
| **MII mode** | | | | | | |
| $f_{clk}$ | clock frequency | for ENET_TX_CLK | [1] | - | 25 | MHz |
| $\delta_{clk}$ | clock duty cycle | | [1] | 50 | 50 | % |
| $t_{su}$ | set-up time | for ENET_TXDn, ENET_TX_EN, ENET_TX_ER | [1][2] | 4 | - | ns |
| $t_h$ | hold time | for ENET_TXDn, ENET_TX_EN, ENET_TX_ER | [1][2] | 2 | - | ns |
| $f_{clk}$ | clock frequency | for ENET_RX_CLK | [1] | - | 25 | MHz |
| $\delta_{clk}$ | clock duty cycle | | [1] | 50 | 50 | % |
| $t_{su}$ | set-up time | for ENET_RXDn, ENET_RX_ER, ENET_RX_DV | [1][2] | 4 | - | ns |
| $t_h$ | hold time | for ENET_RXDn, ENET_RX_ER, ENET_RX_DV | [1][2] | 2 | - | ns |

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

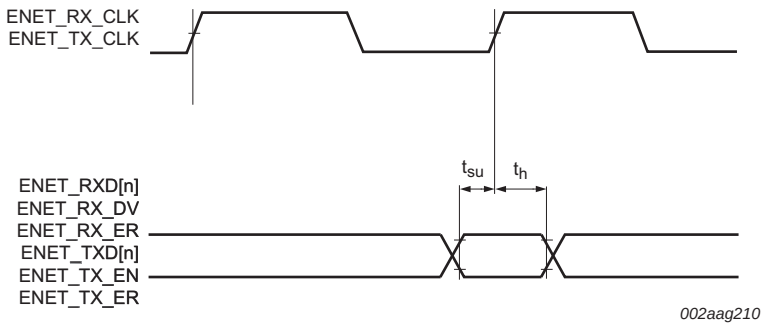


**Fig 38. Ethernet timing**


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## 11.18 SD/MMC

**Table 33. Dynamic characteristics: SD/MMC**

*$T_{amb}$ = −40 °C to 85 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, $C_L$ = 20 pF. SAMPLE_DELAY = 0x9, DRV_DELAY = 0xD in the SDDELAY register sampled at 90 % and 10 % of the signal level, EHS = 1 for SD_CLK pin, EHS = 1 for SD_DATn and SD_CMD pins. Simulated values.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | on pin SD_CLK; data transfer mode | | 52 | MHz |
| $t_{su(D)}$ | data input set-up time | on pins SD_DATn as inputs | 3.9 | - | ns |
| | | on pins SD_CMD as inputs | 5.2 | - | ns |
| $t_{h(D)}$ | data input hold time | on pins SD_DATn as inputs | 0.4 | - | ns |
| | | on pins SD_CMD as inputs | 0 | | ns |
| $t_{d(QV)}$ | data output valid delay time | on pins SD_DATn as outputs | - | 15.3 | ns |
| | | on pins SD_CMD as outputs | - | 16 | ns |
| $t_{h(Q)}$ | data output hold time | on pins SD_DATn as outputs | 4 | - | ns |
| | | on pins SD_CMD as outputs | 4 | - | ns |

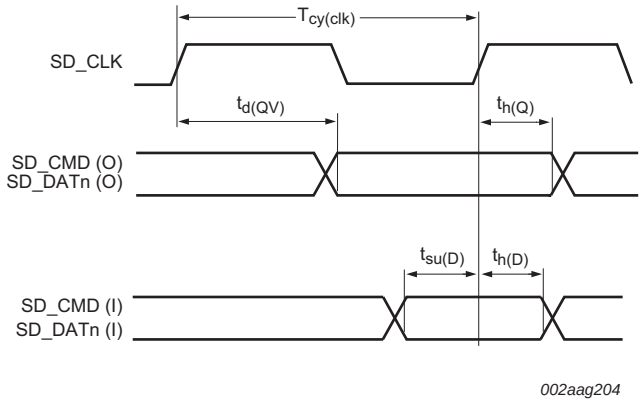


**Fig 39. SD/MMC timing**

## 11.19 LCD

**Table 34. Dynamic characteristics: LCD**

*$T_{amb}$ = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF. Simulated values.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | on pin LCD_DCLK | - | 50 | - | MHz |
| $t_{d(QV)}$ | data output valid delay time | | | - | 17 | ns |
| $t_{h(Q)}$ | data output hold time | | 8.5 | - | | ns |


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## 11.20 SPIFI

**Table 35. Dynamic characteristics: SPIFI**

*$T_{amb}$ = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. $C_L$ = 20 pF. Sampled at 90 % and 10 % of the signal level. EHS = 1 for all pins. Simulated values.*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cy(clk)}$ | clock cycle time | 9.6 | - | ns |
| $t_{DS}$ | data set-up time | 2.8 | - | ns |
| $t_{DH}$ | data hold time | 0 | - | ns |
| $t_{v(Q)}$ | data output valid time | - | 2.6 | ns |
| $t_{h(Q)}$ | data output hold time | 0.8 | - | ns |

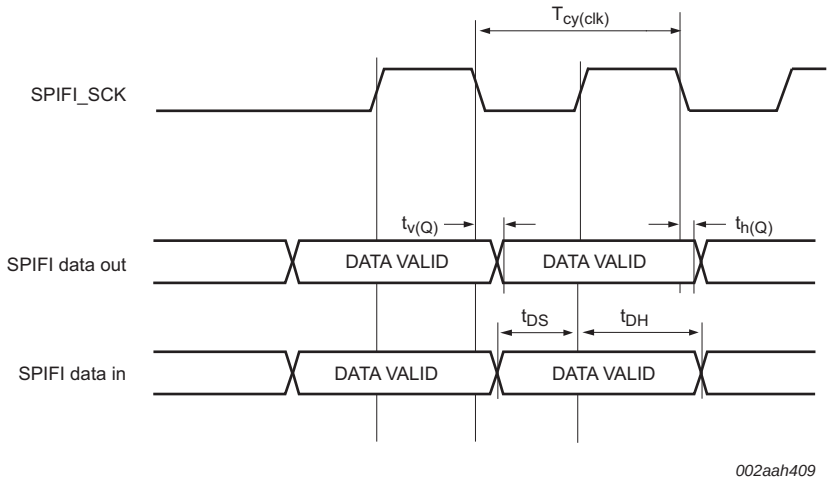


**Fig 40. SPIFI timing (Mode 0)**


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# 12. ADC/DAC electrical characteristics

**Table 36. ADC characteristics**

*$V_{DDA(3V3)}$ over specified ranges; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IA}$ | analog input voltage | | | 0 | - | $V_{DDA(3V3)}$ | V |
| $C_{ia}$ | analog input capacitance | | | - | - | 2 | pF |
| $E_D$ | differential linearity error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [1][2] | - | ±0.8 | - | LSB |
| | | 2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±1.0 | - | LSB |
| $E_{L(adj)}$ | integral non-linearity | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [3] | - | ±0.8 | - | LSB |
| | | 2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±1.5 | - | LSB |
| $E_O$ | offset error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [4] | - | ±0.15 | - | LSB |
| | | 2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±0.15 | - | LSB |
| $E_G$ | gain error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [5] | - | ±0.3 | - | % |
| | | 2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±0.35 | - | % |
| $E_T$ | absolute error | 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V | [6] | - | ±3 | - | LSB |
| | | 2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V | | - | ±4 | - | LSB |
| $R_{vsi}$ | voltage source interface resistance | see Figure 42 | | - | - | $1/(7 \times f_{clk(ADC)} \times C_{ia})$ | kΩ |
| $R_i$ | input resistance | | [7][8] | - | - | 1.2 | MΩ |
| $f_{clk(ADC)}$ | ADC clock frequency | | | - | - | 4.5 | MHz |
| $f_s$ | sampling frequency | 10-bit resolution; 11 clock cycles | | - | - | 400 | kSamples/s |
| | | 2-bit resolution; 3 clock cycles | | | | 1.5 | MSamples/s |

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 41.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 41.

[4] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 41.

[5] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 41.

[6] The absolute error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 41.

[7] $T_{amb}$ = 25 °C.

[8] Input resistance $R_i$ depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.


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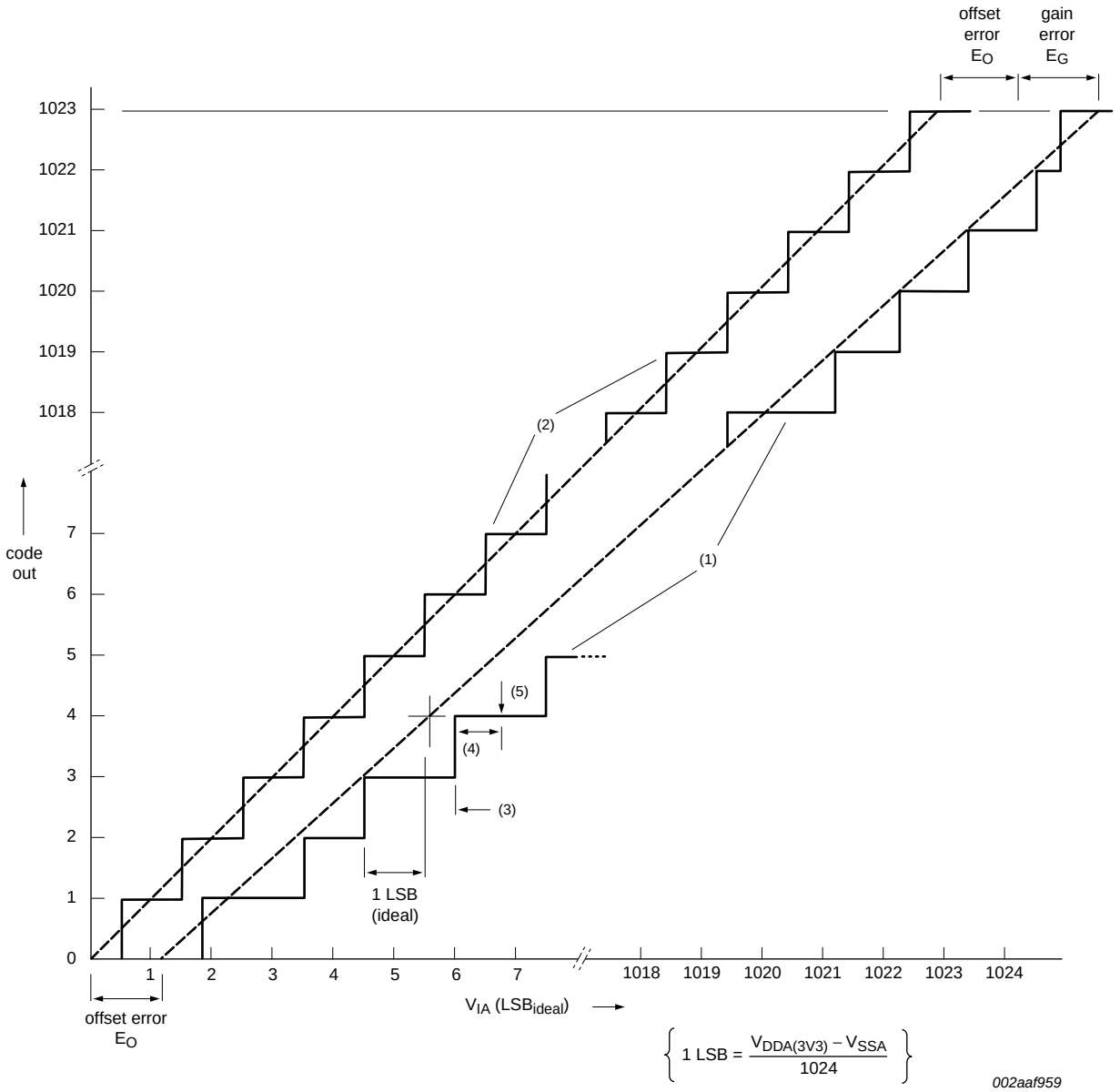


(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 41. 10-bit ADC characteristics**


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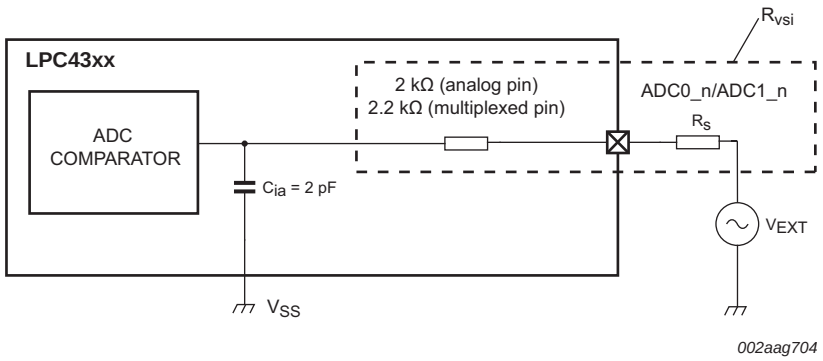


$Rs < 1/((7 \times f_{clk(ADC)}) \times C_{ia}) - 2\ k\Omega$

**Fig 42. ADC interface to pins**

**Table 37. DAC characteristics**

*$V_{DDA(3V3)}$ over specified ranges; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $E_D$ | differential linearity error | $2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$ | [1] | - | ±0.8 | - | LSB |
| | | $2.2\ V \le V_{DDA(3V3)} < 2.7\ V$ | | - | ±1.0 | - | LSB |
| $E_{L(adj)}$ | integral non-linearity | code = 0 to 975<br>$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$ | [1] | - | ±1.0 | - | LSB |
| | | $2.2\ V \le V_{DDA(3V3)} < 2.7\ V$ | | - | ±1.5 | - | LSB |
| $E_O$ | offset error | $2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$ | [1] | - | ±0.8 | - | LSB |
| | | $2.2\ V \le V_{DDA(3V3)} < 2.7\ V$ | | - | ±1.0 | - | LSB |
| $E_G$ | gain error | $2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$ | [1] | - | ±0.3 | - | % |
| | | $2.2\ V \le V_{DDA(3V3)} < 2.7\ V$ | | - | ±1.0 | - | % |
| $C_L$ | load capacitance | | | - | - | 200 | pF |
| $R_L$ | load resistance | | | 1 | - | - | kΩ |
| $t_s$ | settling time | | [2] | | 0.4 | | μσ |

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC43xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.


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# 13. Application information

## 13.1 LCD panel signal usage

**Table 38. LCD panel connections for STN single panel mode**

| External pin | 4-bit mono STN single panel | | 8-bit mono STN single panel | | Color STN single panel | |
|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD[23:8] | - | - | - | - | - | - |
| LCD_VD7 | - | - | P8_4 | UD[7] | P8_4 | UD[7] |
| LCD_VD6 | - | - | P8_5 | UD[6] | P8_5 | UD[6] |
| LCD_VD5 | - | - | P8_6 | UD[5] | P8_6 | UD[5] |
| LCD_VD4 | - | - | P8_7 | UD[4] | P8_7 | UD[4] |
| LCD_VD3 | P4_2 | UD[3] | P4_2 | UD[3] | P4_2 | UD[3] |
| LCD_VD2 | P4_3 | UD[2] | P4_3 | UD[2] | P4_3 | UD[2] |
| LCD_VD1 | P4_4 | UD[1] | P4_4 | UD[1] | P4_4 | UD[1] |
| LCD_VD0 | P4_1 | UD[0] | P4_1 | UD[0] | P4_1 | UD[0] |
| LCD_LP | P7_6 | LCDLP | P7_6 | LCDLP | P7_6 | LCDLP |
| LCD_ENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM |
| LCD_FP | P4_5 | LCDFP | P4_5 | LCDFP | P4_5 | LCDFP |
| LCD_DCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK |
| LCD_LE | P7_0 | LCDLE | P7_0 | LCDLE | P7_0 | LCDLE |
| LCD_PWR | P7_7 | CDPWR | P7_7 | LCDPWR | P7_7 | LCDPWR |
| GP_CLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN |

**Table 39. LCD panel connections for STN dual panel mode**

| External pin | 4-bit mono STN dual panel | | 8-bit mono STN dual panel | | Color STN dual panel | |
|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD[23:16] | - | - | - | - | - | - |
| LCD_VD15 | - | - | PB_4 | LD[7] | PB_4 | LD[7] |
| LCD_VD14 | - | - | PB_5 | LD[6] | PB_5 | LD[6] |
| LCD_VD13 | - | - | PB_6 | LD[5] | PB_6 | LD[5] |
| LCD_VD12 | - | - | P8_3 | LD[4] | P8_3 | LD[4] |
| LCD_VD11 | P4_9 | LD[3] | P4_9 | LD[3] | P4_9 | LD[3] |
| LCD_VD10 | P4_10 | LD[2] | P4_10 | LD[2] | P4_10 | LD[2] |
| LCD_VD9 | P4_8 | LD[1] | P4_8 | LD[1] | P4_8 | LD[1] |
| LCD_VD8 | P7_5 | LD[0] | P7_5 | LD[0] | P7_5 | LD[0] |
| LCD_VD7 | - | - | | UD[7] | P8_4 | UD[7] |
| LCD_VD6 | - | - | P8_5 | UD[6] | P8_5 | UD[6] |
| LCD_VD5 | - | - | P8_6 | UD[5] | P8_6 | UD[5] |
| LCD_VD4 | - | - | P8_7 | UD[4] | P8_7 | UD[4] |
| LCD_VD3 | P4_2 | UD[3] | P4_2 | UD[3] | P4_2 | UD[3] |


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**Table 39. LCD panel connections for STN dual panel mode** *…continued*

| External pin | 4-bit mono STN dual panel | | 8-bit mono STN dual panel | | Color STN dual panel | |
|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD2 | P4_3 | UD[2] | P4_3 | UD[2] | P4_3 | UD[2] |
| LCD_VD1 | P4_4 | UD[1] | P4_4 | UD[1] | P4_4 | UD[1] |
| LCD_VD0 | P4_1 | UD[0] | P4_1 | UD[0] | P4_1 | UD[0] |
| LCD_LP | P7_6 | LCDLP | P7_6 | LCDLP | P7_6 | LCDLP |
| LCD_ENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM |
| LCD_FP | P4_5 | LCDFP | P4_5 | LCDFP | P4_5 | LCDFP |
| LCD_DCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK |
| LCD_LE | P7_0 | LCDLE | P7_0 | LCDLE | P7_0 | LCDLE |
| LCD_PWR | P7_7 | LCDPWR | P7_7 | LCDPWR | P7_7 | LCDPWR |
| GP_CLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN |

**Table 40. LCD panel connections for TFT panels**

| External pin | TFT 12 bit (4:4:4 mode) | | TFT 16 bit (5:6:5 mode) | | TFT 16 bit (1:5:5:5 mode) | | TFT 24 bit | |
|---|---|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD23 | PB_0 | BLUE3 | PB_0 | BLUE4 | PB_0 | BLUE4 | PB_0 | BLUE7 |
| LCD_VD22 | PB_1 | BLUE2 | PB_1 | BLUE3 | PB_1 | BLUE3 | PB_1 | BLUE6 |
| LCD_VD21 | PB_2 | BLUE1 | PB_2 | BLUE2 | PB_2 | BLUE2 | PB_2 | BLUE5 |
| LCD_VD20 | PB_3 | BLUE0 | PB_3 | BLUE1 | PB_3 | BLUE1 | PB_3 | BLUE4 |
| LCD_VD19 | - | - | P7_1 | BLUE0 | P7_1 | BLUE0 | P7_1 | BLUE3 |
| LCD_VD18 | - | - | - | - | P7_2 | intensity | P7_2 | BLUE2 |
| LCD_VD17 | - | - | - | - | - | - | P7_3 | BLUE1 |
| LCD_VD16 | - | - | - | - | - | - | P7_4 | BLUE0 |
| LCD_VD15 | PB_4 | GREEN3 | PB_4 | GREEN5 | PB_4 | GREEN4 | PB_4 | GREEN7 |
| LCD_VD14 | PB_5 | GREEN2 | PB_5 | GREEN4 | PB_5 | GREEN3 | PB_5 | GREEN6 |
| LCD_VD13 | PB_6 | GREEN1 | PB_6 | GREEN3 | PB_6 | GREEN2 | PB_6 | GREEN5 |
| LCD_VD12 | P8_3 | GREEN0 | P8_3 | GREEN2 | P8_3 | GREEN1 | P8_3 | GREEN4 |
| LCD_VD11 | - | - | P4_9 | GREEN1 | P4_9 | GREEN0 | P4_9 | GREEN3 |
| LCD_VD10 | - | - | P4_10 | GREEN0 | P4_10 | intensity | P4_10 | GREEN2 |
| LCD_VD9 | - | - | - | - | - | - | P4_8 | GREEN1 |
| LCD_VD8 | - | - | - | - | - | - | P7_5 | GREEN0 |
| LCD_VD7 | P8_4 | RED3 | P8_4 | RED4 | P8_4 | RED4 | P8_4 | RED7 |
| LCD_VD6 | P8_5 | RED2 | P8_5 | RED3 | P8_5 | RED3 | P8_5 | RED6 |
| LCD_VD5 | P8_6 | RED1 | P8_6 | RED2 | P8_6 | RED2 | P8_6 | RED5 |
| LCD_VD4 | P8_7 | RED0 | P8_7 | RED1 | P8_7 | RED1 | P8_7 | RED4 |
| LCD_VD3 | - | - | P4_2 | RED0 | P4_2 | RED0 | P4_2 | RED3 |
| LCD_VD2 | - | - | - | - | P4_3 | intensity | P4_3 | RED2 |
| LCD_VD1 | - | - | - | - | - | - | P4_4 | RED1 |


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**Table 40. LCD panel connections for TFT panels** *...continued*

| External pin | TFT 12 bit (4:4:4 mode) | | TFT 16 bit (5:6:5 mode) | | TFT 16 bit (1:5:5:5 mode) | | TFT 24 bit | |
|---|---|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD0 | - | - | - | - | - | - | P4_1 | RED0 |
| LCD_LP | P7_6 | LCDLP | P7_6 | LCDLP | P7_6 | LCDLP | P7_6 | LCDLP |
| LCD_ENAB /LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM |
| LCD_FP | P4_5 | LCDFP | P4_5 | LCDFP | P4_5 | LCDFP | P4_5 | LCDFP |
| LCD_DCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK |
| LCD_LE | P7_0 | LCDLE | P7_0 | LCDLE | P7_0 | LCDLE | P7_0 | LCDLE |
| LCD_PWR | P7_7 | LCDPWR | P7_7 | LCDPWR | P7_7 | LCDPWR | P7_7 | LCDPWR |
| GP_CLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN |

## 13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC43xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode, couple the input clock signal with a capacitor of 100 pF ($C_C$ in Figure 43), with an amplitude of at least 200 mV (RMS). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 44, and in Table 41 and Table 42. Since the feedback resistance is integrated on chip, only a crystal and the capacitances CX1 and CX2 need to be connected externally in case of fundamental mode oscillation L, CL and RS represent the fundamental frequency). The capacitance $C_P$ in Figure 44 represents the parallel package capacitance and must not be larger than 7 pF. Parameters FC, CL, RS and CP are supplied by the crystal manufacturer.

**Table 41. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode**

| Fundamental oscillation frequency | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|
| 2 MHz | < 200 Ω | 33 pF, 33 pF |
| | < 200 Ω | 39 pF, 39 pF |
| | < 200 Ω | 56 pF, 56 pF |
| 4 MHz | < 200 Ω | 18 pF, 18 pF |
| | < 200 Ω | 39 pF, 39 pF |
| | < 200 Ω | 56 pF, 56 pF |
| 8 MHz | < 200 Ω | 18 pF, 18 pF |
| | < 200 Ω | 39 pF, 39 pF |


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**Table 41. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode** *...continued*

| Fundamental oscillation frequency | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{X2}$ |
|---|---|---|
| 12 MHz | < 160 Ω | 18 pF, 18 pF |
| | < 160 Ω | 39 pF, 39 pF |
| 16 MHz | < 120 Ω | 18 pF, 18 pF |
| | < 80 Ω | 33 pF, 33 pF |
| 20 MHz | <100 Ω | 18 pF, 18 pF |
| | < 80 Ω | 33 pF, 33 pF |

**Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode**

| Fundamental oscillation frequency | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}$, $C_{x2}$ |
|---|---|---|
| 15 MHz | < 80 Ω | 18 pF, 18 pF |
| 20 MHz | < 80 Ω | 39 pF, 39 pF |
| | < 100 Ω | 47 pF, 47 pF |

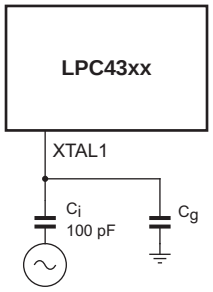


**Fig 43. Slave mode operation of the on-chip oscillator**

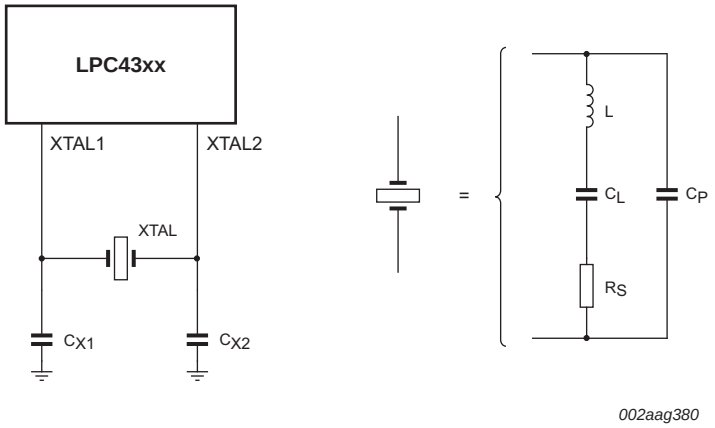


**Fig 44. Oscillator modes with external crystal model used for $C_{X1}$/$C_{X2}$ evaluation**


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## 13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances $C_{RTCX1}$ and $C_{RTCX2}$ need to be connected externally. Typical capacitance values for $C_{RTCX1}$ and $C_{RTCX2}$ are $C_{RTCX1/2}$ = 20 (typical) $\pm$ 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF. $V_{i(RMS)}$ must be lower than 450 mV. See Figure 43 for a similar slave-mode set-up that uses the crystal oscillator.

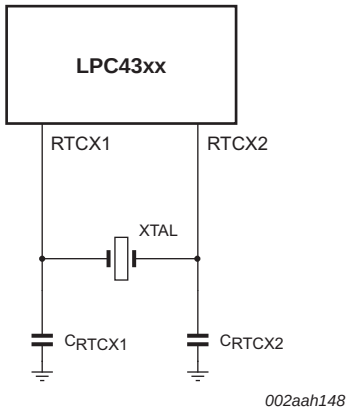


**Fig 45. RTC 32 kHz oscillator circuit**

## 13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors $C_{x1}$, $C_{x2}$, and $C_{x3}$ in case of third overtone crystal usage have a common ground plane. Also connect the external components to the ground plain. To keep the noise coupled in via the PCB as small as possible, make loops and parasitics as small as possible. Choose smaller values of $C_{x1}$ and $C_{x2}$ if parasitics increase in the PCB layout.

Ensure that no high-speed or high-drive signals are near the RTCX1/2 signals.

## 13.5 Standard I/O pin configuration

Figure 46 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input buffer enabled/disabled
- Analog input

The default configuration for standard I/O pins is input buffer disabled and pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.


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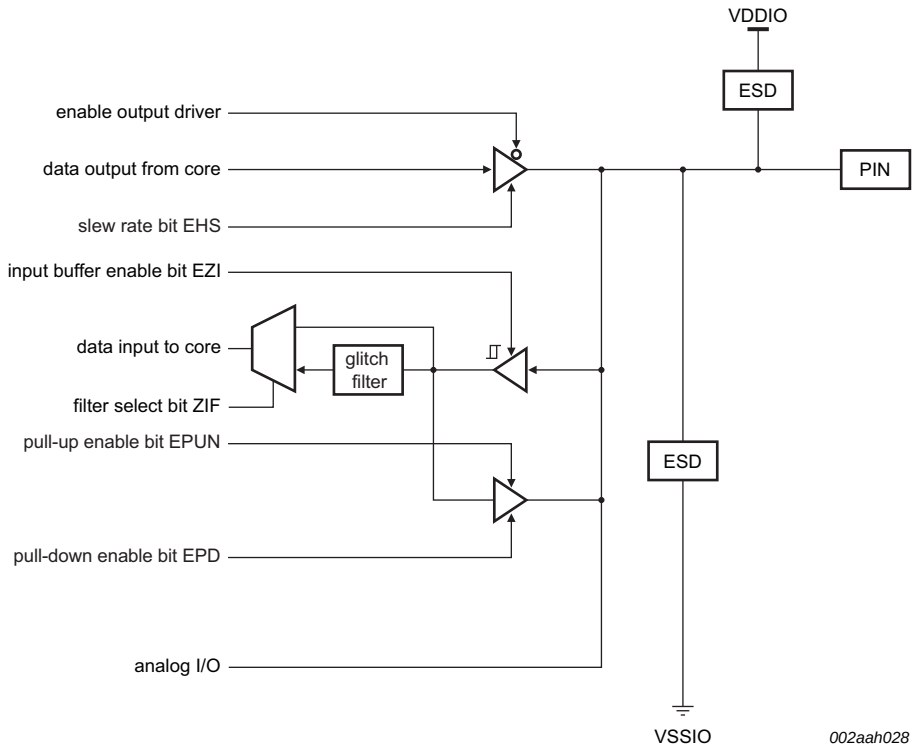


The glitch filter rejects pulses of typical 12 ns width.

**Fig 46. Standard I/O pin configuration with analog input**

## 13.6 Reset pin configuration

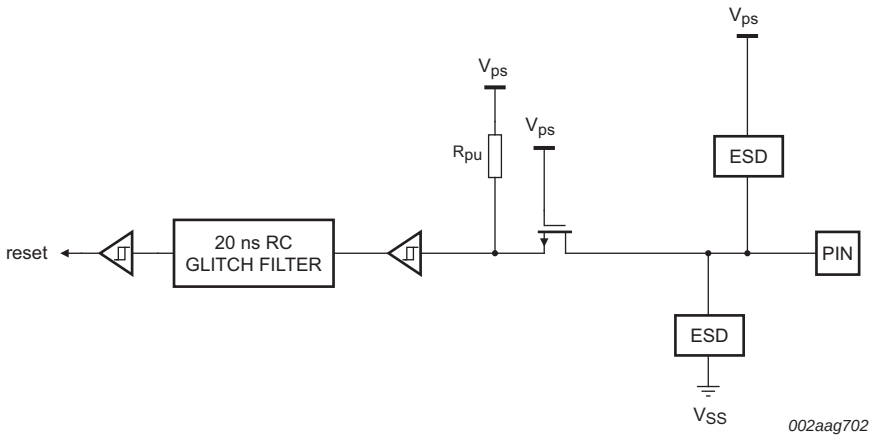


**Fig 47. Reset pin configuration**

## 13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 48) or bus-powered device (see Figure 49).


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On the LPC4350/30/20/10, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 49.

**Remark:** Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

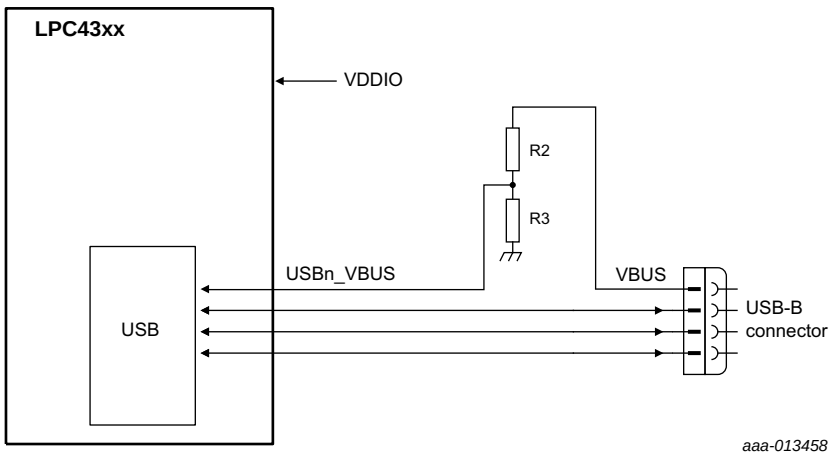


**Fig 48. USB interface on a self-powered device where USBn_VBUS = 5 V**


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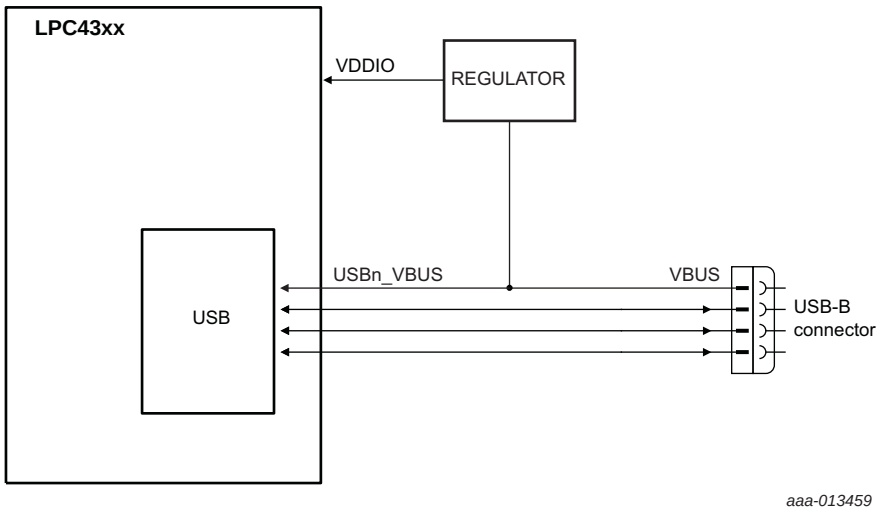


**Fig 49. USB interface on a bus-powered device**

**Remark:** If the VBUS function of the USB1 interface is not connected, configure the pin function for GPIO using the function control bits in the SYSCON block.

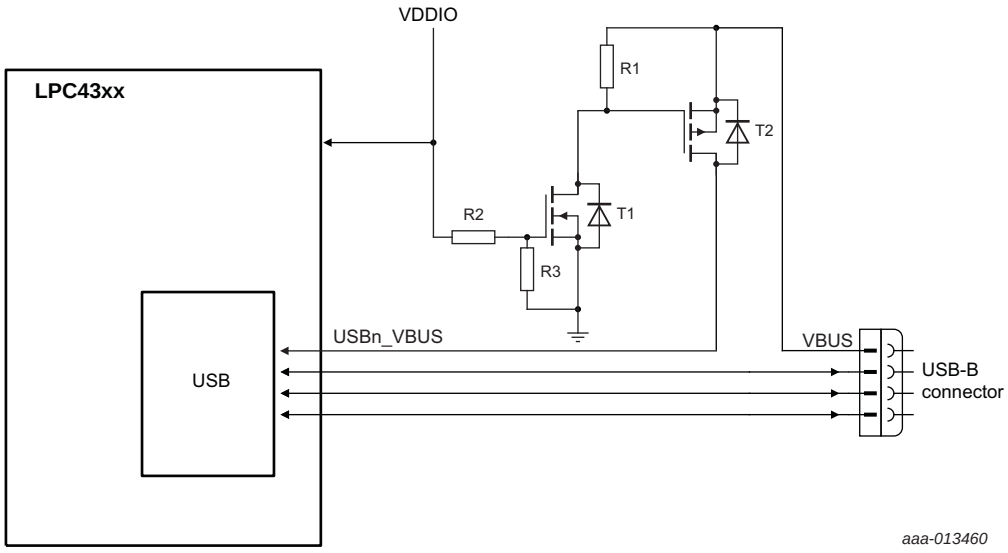


**Fig 50. USB interface for USB operating in OTG mode**

**Remark:** In OTG mode, it is important to be able to detect the VBUS level and to charge and discharge VBUS. This requires adding active devices that disconnect the link when VDDIO is not present.


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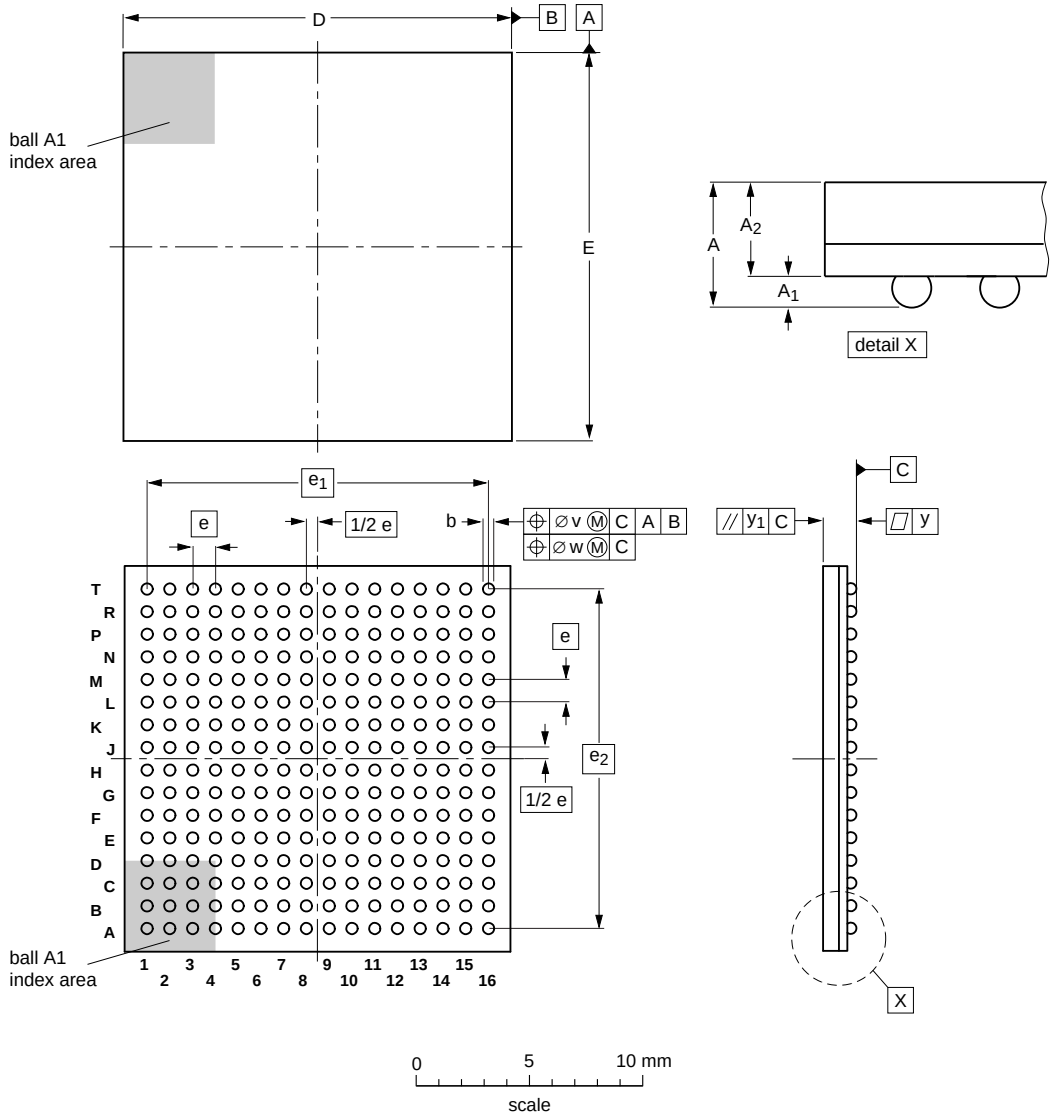
# 14. Package outline

**LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm** **SOT740-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.55 | 0.45<br>0.35 | 1.1<br>0.9 | 0.55<br>0.45 | 17.2<br>16.8 | 17.2<br>16.8 | 1 | 15 | 15 | 0.25 | 0.1 | 0.12 | 0.35 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT740-2 | - - - | MO-192 | - - - | | | ~~05-06-16~~<br>05-08-04 |

**Fig 51. Package outline LBGA256 package**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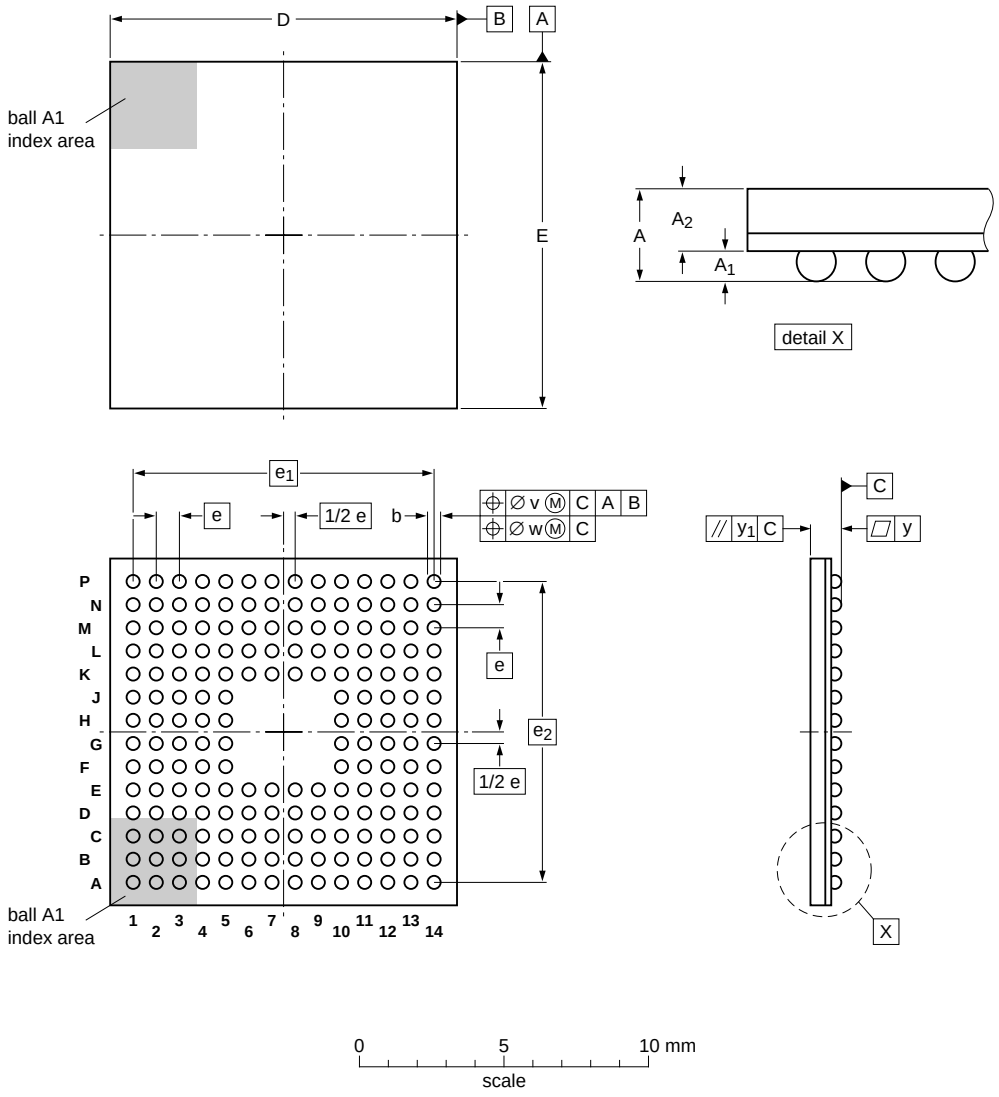
**TFBGA180: thin fine-pitch ball grid array package; 180 balls** **SOT570-3**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | | A | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.20 | 0.40 | 0.80 | 0.50 | 12.1 | 12.1 | 0.8 | 10.4 | 10.4 | 0.15 | 0.05 | 0.12 | 0.1 |
| | nom | 1.06 | 0.35 | 0.71 | 0.45 | 12.0 | 12.0 | | | | | | | |
| | min | 0.95 | 0.30 | 0.65 | 0.40 | 11.9 | 11.9 | | | | | | | |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT570-3 | | | | | | ~~08-07-09~~ 10-04-15 |

**Fig 52. Package outline of the TFBGA180 package**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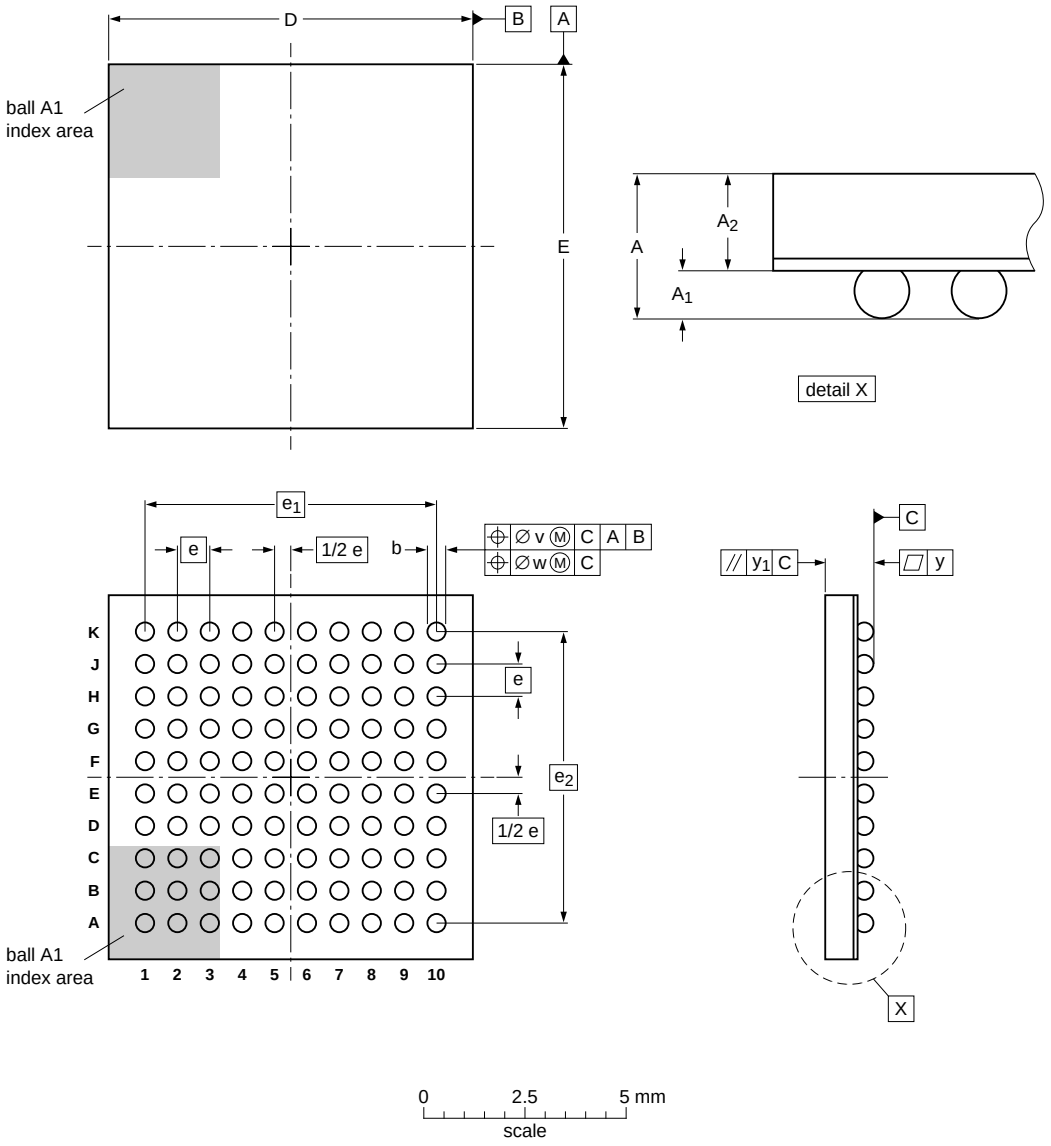
**TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm** **SOT926-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.4<br>0.3 | 0.8<br>0.65 | 0.5<br>0.4 | 9.1<br>8.9 | 9.1<br>8.9 | 0.8 | 7.2 | 7.2 | 0.15 | 0.05 | 0.08 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT926-1 | - - - | - - - | - - - | | | ~~05-12-09~~<br>05-12-22 |

**Fig 53. Package outline of the TFBGA100 package**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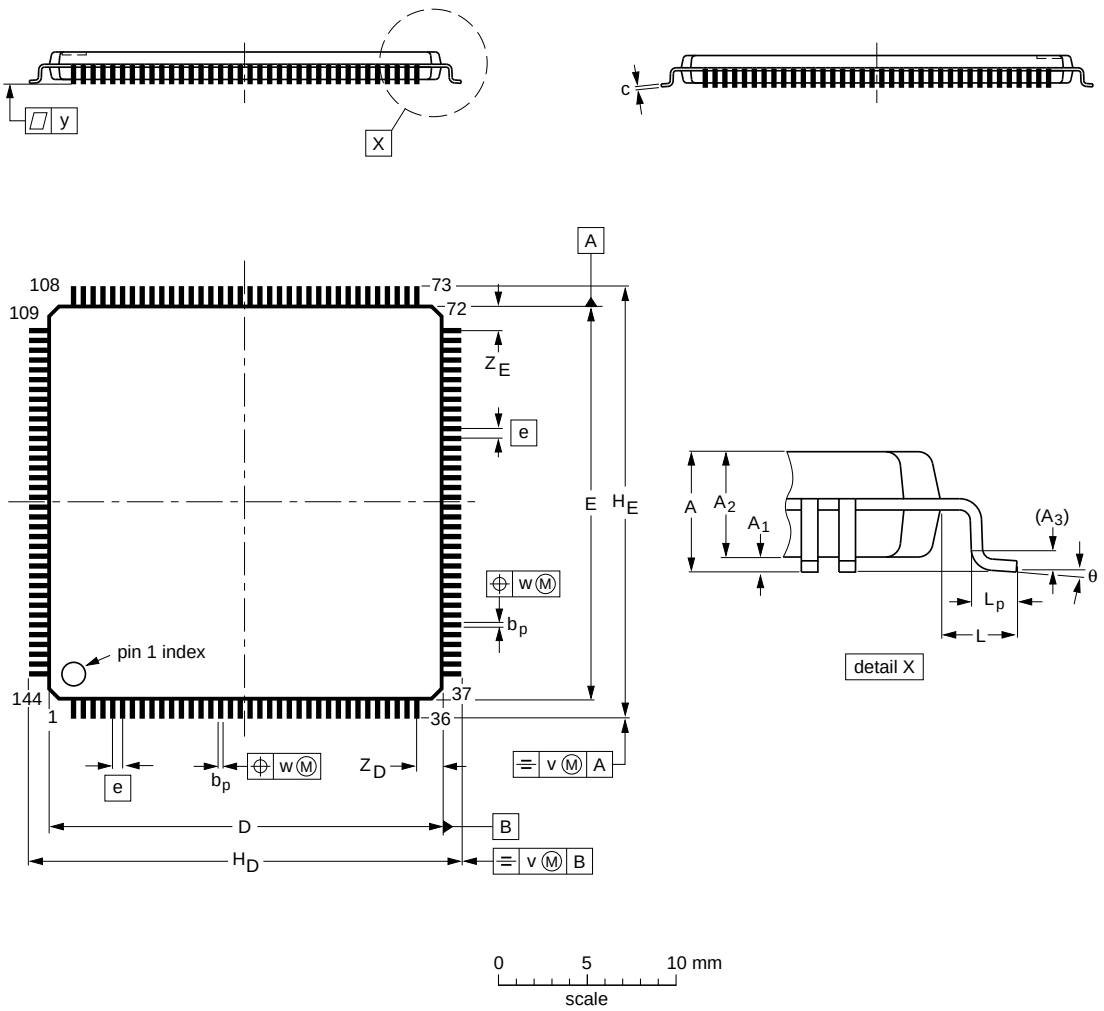
**LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm** **SOT486-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.15<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.20<br>0.09 | 20.1<br>19.9 | 20.1<br>19.9 | 0.5 | 22.15<br>21.85 | 22.15<br>21.85 | 1 | 0.75<br>0.45 | 0.2 | 0.08 | 0.08 | 1.4<br>1.1 | 1.4<br>1.1 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT486-1 | 136E23 | MS-026 | | | | ~~00-03-14~~<br>03-02-20 |

**Fig 54. Package outline for the LQFP144 package**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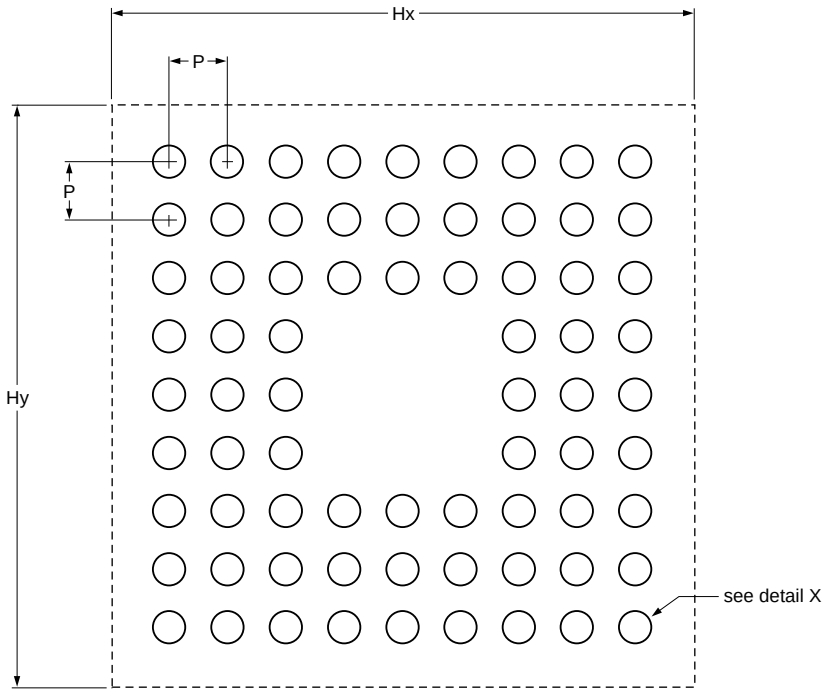
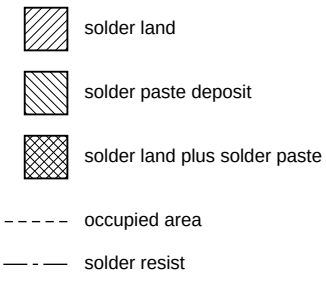
# 15. Soldering

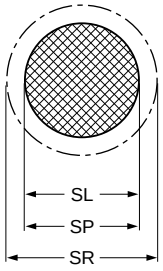
**Footprint information for reflow soldering of LBGA256 package** **SOT740-2**




Generic footprint pattern

Refer to the package outline drawing for actual layout




detail X

DIMENSIONS in mm

| P | SL | SP | SR | Hx | Hy |
|---|---|---|---|---|---|
| 1.00 | 0.450 | 0.450 | 0.600 | 17.500 | 17.500 |

*sot740-2_fr*

**Fig 55. Reflow soldering of the LBGA256 package**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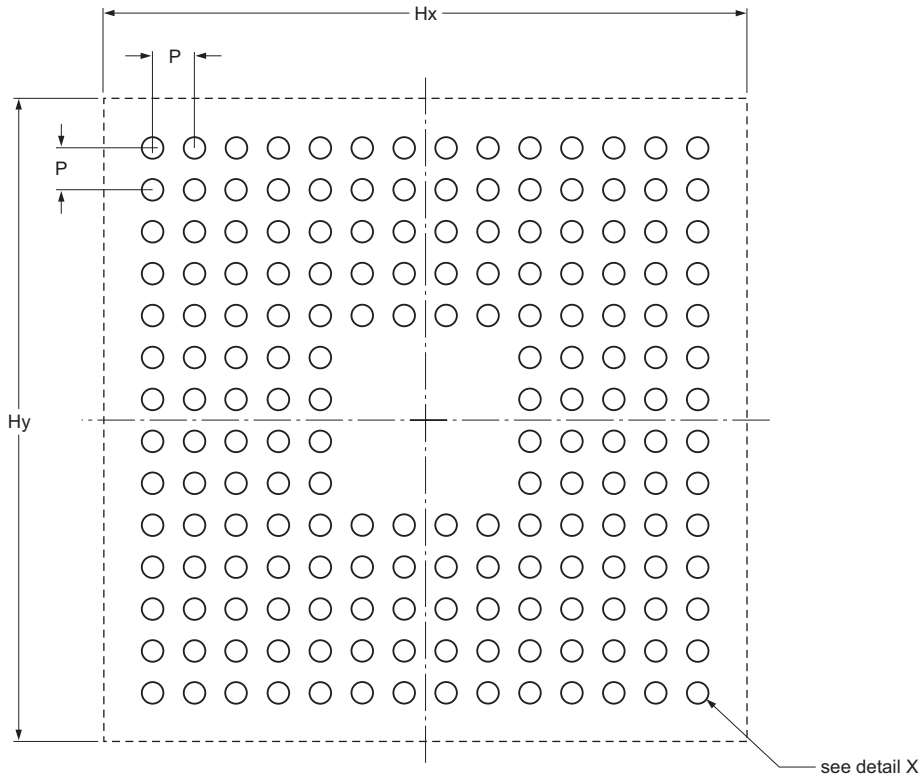
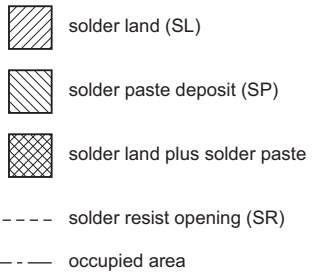
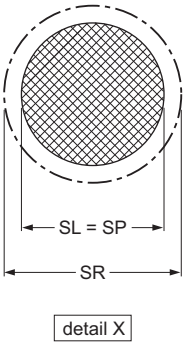
**Footprint information for reflow soldering of TFBGA180 package** **SOT570-3**




detail X

Dimensions in mm

| P | SL | SP | SR | Hx | Hy |
|---|---|---|---|---|---|
| 0.80 | 0.40 | 0.40 | 0.50 | 12.30 | 12.30 |

| Issue date | ~~14-01-30~~ 15-08-27 |
|---|---|

Recommend stencil thickness: 0.1 mm

*sot570-3_fr*

**Fig 56. Reflow soldering of the TFBGA180 package**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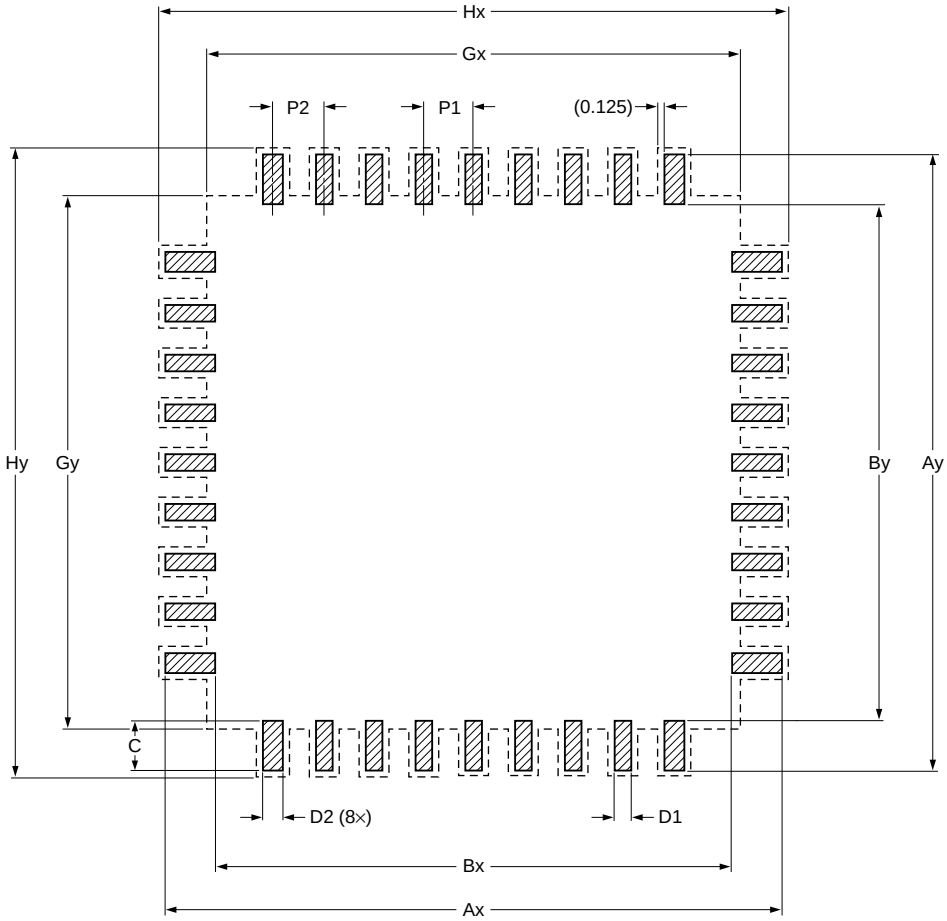
**Footprint information for reflow soldering of LQFP144 package** **SOT486-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 23.300 | 23.300 | 20.300 | 20.300 | 1.500 | 0.280 | 0.400 | 20.500 | 20.500 | 23.550 | 23.550 |

*sot486-1_fr*

**Fig 57. Reflow soldering of the LQFP144 package**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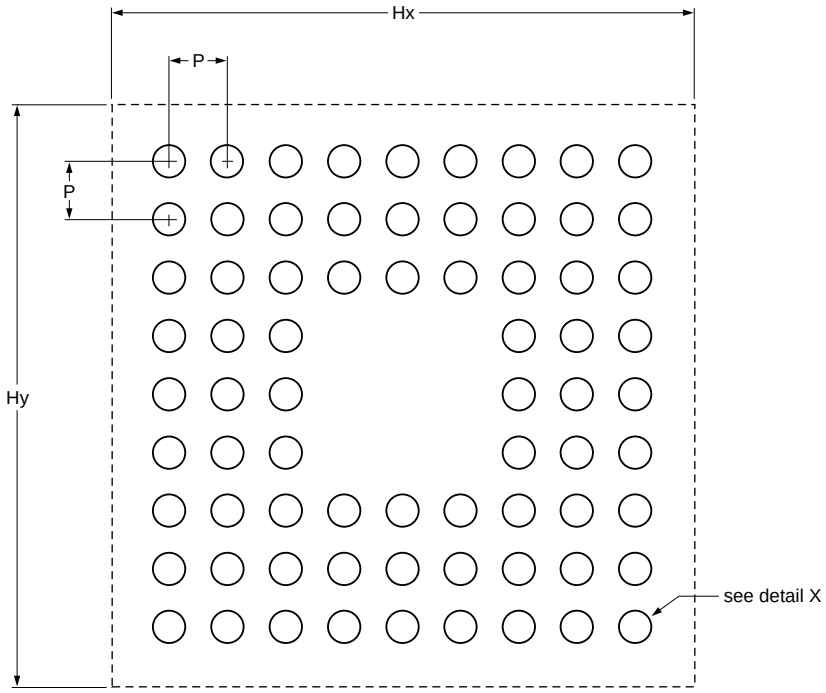
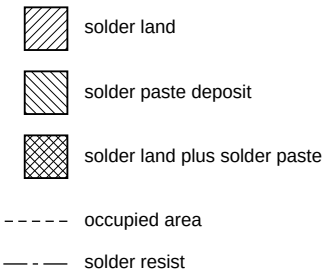
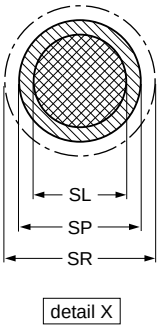
**Footprint information for reflow soldering of TFBGA100 package** **SOT926-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout




detail X

DIMENSIONS in mm

| P | SL | SP | SR | Hx | Hy |
|---|---|---|---|---|---|
| 0.80 | 0.330 | 0.400 | 0.480 | 9.400 | 9.400 |

*sot926-1_fr*

**Fig 58. Reflow soldering of the TFBGA100 package**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# 16. Abbreviations

Table 43. Abbreviations

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| API | Application Programming Interface |
| BOD | BrownOut Detection |
| CAN | Controller Area Network |
| CMAC | Cipher-based Message Authentication Code |
| CSMA/CD | Carrier Sense Multiple Access with Collision Detection |
| DAC | Digital-to-Analog Converter |
| DC-DC | Direct Current-to-Direct Current |
| DMA | Direct Memory Access |
| GPIO | General-Purpose Input/Output |
| IRC | Internal RC |
| IrDA | Infrared Data Association |
| JTAG | Joint Test Action Group |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MAC | Media Access Control |
| MCU | MicroController Unit |
| MIIM | Media Independent Interface Management |
| n.c. | not connected |
| OHCI | Open Host Controller Interface |
| OTG | On-The-Go |
| PHY | Physical Layer |
| PLL | Phase-Locked Loop |
| PMC | Power Mode Control |
| PWM | Pulse Width Modulator |
| RIT | Repetitive Interrupt Timer |
| RMII | Reduced Media Independent Interface |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SIMD | Single Instruction Multiple Data |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| UART | Universal Asynchronous Receiver/Transmitter |
| ULPI | UTMI+ Low Pin Interface |
| USART | Universal Synchronous Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| UTMI | USB2.0 Transceiver Macrocell Interface |


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## 17. References

[1] LPC43xx User manual UM10503:
http://www.nxp.com/documents/user_manual/UM10503.pdf

[2] LPC43X0 Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC43XX.pdf


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# 18. Revision history

**Table 44. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC4350_30_20_10 v.4.6 | 20160314 | Product data sheet | - | LPC4350_30_20_10 v.4.5 |
| Modifications: | • Updated Table 28 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”. | | | |
| LPC4350_30_20_10 v.4.5 | 20151126 | Product data sheet | - | LPC4350_30_20_10 v.4.4 |
| Modifications: | • Fixed the revision number on the first page to v.4.5. In v.4.4 of the document, the revision number of the first page was v.4.3 while the document was at v.4.4.<br>• Added a table note: The values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. See Table 27 “Dynamic characteristics: Static asynchronous external memory interface”.<br>• Changed footnote 12 in Table 3 “Pin description” with the text: VPP is internally connected to VDDIO for all packages with the exception of the LFBGA256 package.<br>• Updated Figure 29 “I2S-bus timing (receive)”: for signal I2Sx_RX_WS changed second half of the signal from tsu(D) to th(D). | | | |
| LPC4350_30_20_10 v.4.4 | 20151117 | Product data sheet | 2015110031 | LPC4350_30_20_10 v.4.3 |
| Modifications: | • Added GPCLKIN section and table. See Section 11.6 “GPCLKIN” and Table 19 “Dynamic characteristic: GPCLKIN”.<br>• Updated SSP slave and SSP master values in Table 24 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.<br>– removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode.<br>– added units to $t_d$, delay time, for SSP slave and master mode. | | | |
| LPC4350_30_20_10 v.4.3 | 20150430 | Product data sheet | | LPC4350_30_20_10 v.4.2 |
| Modifications: | • Updated Section 1 “General description”.<br>• Table note 2 corrected in Table 10.<br>• Updated USART dynamic characteristics table. See Table 23.<br>• Updated SD/MMC dynamic characteristics table. See Table 33.<br>• Updated SPIFI dynamic characteristics table. See Table 35.<br>• Added SSP slave timing data. See Table 24.<br>• Updated USB dynamic characteristics table: USB0 and USB1 pins (full-speed). $t_r$ Min 4 ns, Max 20 ns; $t_f$ Min 4 ns, Max 20 ns; $t_{FRFM}$ Min 90 %, Max 111.11 %. See Table 30:<br>• Added band gap characteristics table. See Table 13.<br>• Added motor control PWM instead of PWM to Table 2.<br>• Added remark to Table 30. | | | |
| LPC4350_30_20_10 v.4.2 | 20140818 | Product data sheet | 201408013F01 | LPC4350_30_20_10 v.4.1 |


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**Table 44. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| Modifications: | • Parameter $C_I$ corrected for high-drive pins (changed from 2 pF to 5.2 pF). See Table 10.<br>• Table 19 “Dynamic characteristic: I/O pins[1]” added.<br>• IRC accuracy changed from 1 % to 1.5 % over the full temperature range. See Table 17 “Dynamic characteristic: IRC oscillator”.<br>• Description of internal pull-up resistor configuration added for $\overline{\text{RESET}}$, WAKEUPn, and ALARM pins.See Table 3.<br>• Description of DEBUG pin updated.<br>• Input range for PLL1 corrected: 1 MHz to 25 MHz. See Section 7.22.7 “System PLL1”.<br>• Section 13.7 “Suggested USB interface solutions” added.<br>• SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 “SSP master mode timing (SPI mode)”.<br>• Parameters $t_{lead}$, $t_{lag}$, and $t_d$ added in Table 23 “Dynamic characteristics: SSP pins in SPI mode”.<br>• Reset state of the RTC alarm pin RTC_ALARM added. See Table 3.<br>• SRAM location for parts LPC4320 corrected in Figure 7.<br>• IEEE standard 802.3 compliance added to Section 11.16. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals.\<br>• Signal polarity of EMC_CKEOUT and EMC_DQMOUT corrected. Both signals are active HIGH.<br>•<br>• Parameter $t_{CSLWEL}$ with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 26 “Dynamic characteristics: Static asynchronous external memory interface”.<br>• Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 26 “Dynamic characteristics: Static asynchronous external memory interface”. | | | |
| LPC4350_30_20_10 v.4.1 | 20131211 | Product data sheet | - | LPC4350_30_20_10 v.4 |
| Modifications: | • Description of $\overline{\text{RESET}}$ pin updated in Table 3.<br>• Layout of local SRAM at address 0x1008 0000 clarified in Figure 7 “LPC4350/30/20/10 Memory mapping (overview)”.<br>• Maximum value for $V_{i(RMS)}$ added in Section 13.3 “RTC oscillator”.<br>• $V_O$ for RTC_ALARM pin added in Table 10.<br>• RTC_ALARM and WAKEUPn pins added to Table 10.<br>• Table note 9 added in Table 10.<br>• Timing parameters in Table 31 “Dynamic characteristics: SD/MMC” corrected.<br>• Band gap characteristics removed.<br>• OTP memory size available for general purpose use corrected.<br>• Part LPC4350FBD208 removed. | | | |
| LPC4350_30_20_10 v.4 | 20130326 | Product data sheet | - | LPC4350_30_20_10 v.3.7 |


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**Table 44. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| | • Parameter $I_{LH}$ (High-level leakage current) for condition $V_I$ = 5 V changed to 20 nA (max). See Table 10.<br>• Parameter $V_{DDA(3V3)}$ added for pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3 in Table 10.<br>• SPI timing data added. See Table 22.<br>• SGPIO timing data added. See Table 23.<br>• SPI and SGPIO peripheral power consumption added in Table 11.<br>• Data sheet status changed to Product data sheet.<br>• Corrected max voltage on pins USB0_DP, USB0_DM, USB0_VBUS, USB1_DP, and USB1_DM in Table 6 and Table 10 to be consistent with USB specifications. | | | |
| LPC4350_30_20_10 v.3.7 | 20130131 | Preliminary data sheet | - | LPC4350_30_20_10 v.3.6 |
| Modifications: | • SGPIO and SPI location corrected in Figure 1.<br>• SGPIO-to-DMA connection corrected in Figure 7.<br>• Power consumption in active mode corrected. See parameter $I_{DD(REG)(3V3)}$ in Table 10 and graphs Figure 12, Figure 13, and Figure 14.<br>• Parameter name $I_{DD(ADC)}$ changed to $I_{DDA}$ in Table 10.<br>• Figure 21 “Band gap voltage for different temperatures and process conditions” and Table 13 “Band gap characteristics” corrected.<br>• Added note to limit data in Table 24 “Dynamic characteristics: Static asynchronous external memory interface” to single memory accesses.<br>• Value of parameter $I_{DD(REG)(3V3)}$ in deep power-down increased to 0.03 µA in Table 10.<br>• Value of parameter $I_{DD(IO)}$ in deep power-down increased to 0.05 µA in Table 10. | | | |
| LPC4350_30_20_10 v.3.6 | 20121119 | Preliminary data sheet | - | LPC4350_30_20_10 v.3.5 |
| Modifications: | • Table 13 “Band gap characteristics” added.<br>• Power consumption for M0 core added in Table 11 “Peripheral power consumption”.<br>• Section 7.22.10 “Power Management Controller (PMC)” added.<br>• Table 10, added Table note 2: “Dynamic characteristics for peripherals are provided for $V_{DD(REG)(3V3)} \geq 2.7$ V.”<br>• Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3.<br>• Use of C_CAN peripheral restricted in Section 2.<br>• ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.<br>• Minimum value for parameter $V_{IL}$ changed to 0 V in Table 10 “Static characteristics”. | | | |
| LPC4350_30_20_10 v.3.5 | 20121011 | Preliminary data sheet | - | LPC4350_30_20_10 v.3.4 |


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**Table 44. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| Modifications: | • Temperature range for simulated timing characteristics corrected to $T_{amb}$ = −40 °C to +85 °C in Section 11 “Dynamic characteristics”.<br>• SPIFI timing added. See Section 11.15.<br>• SPIFI maximum data rate changed to 52 MB per second.<br>• Editorial updates.<br>• Figure 25 and Figure 26 updated for full temperature range.<br>• Section 7.23 “Serial Wire Debug/JTAG” updated.<br>• The following changes were made on the TFBGA180 pinout in Table 3:<br>– P1_13 moved from ball D6 to L8.<br>– P7_5 moved from ball C7 to A7.<br>– PF_4 moved from ball L8 to D6.<br>– $\overline{\text{RESET}}$ moved from ball B7 to C7.<br>– RTCX2 moved from ball A7 to B7.<br>– Ball G10 changed from VSS to VDDIO. | | | |
| LPC4350_30_20_10 v.3.4 | 20120904 | Preliminary data sheet | - | LPC4350_30_20_10 v.3.3 |
| Modifications: | • SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI.<br>• Minimum value for all supply voltages changed to -0.5 V in Table 6. | | | |
| LPC4350_30_20_10 v.3.3 | 20120821 | Preliminary data sheet | - | LPC4350_30_20_10 v.3.2 |
| Modifications: | • Parameter $t_{wake}$ updated in Table 13 for wake-up from deep power-down mode and reset.<br>• Dynamic characteristics of the SD/MMC controller updated in Table 28.<br>• Dynamic characteristics of the LCD controller updated in Table 29.<br>• Dynamic characteristics of the SSP controller updated in Table 21.<br>• Minimum value of $V_I$ for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”,“USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6.<br>• Parameters $I_{IL}$ and $I_{IH}$ renamed to $I_{LL}$ and $I_{LH}$ in Table 10.<br>• AES removed. AES is available on parts LPC43Sxx only.<br>• Pin configuration diagrams corrected for LQFP packages (Figure 5 and Figure 6).<br>• Figure 10 updated.<br>• All power consumption data updated in Table 10 and Section 10.1 “Power consumption”.<br>• BOD levels updated in Table 12.<br>• SWD debug option removed for Cortex-M0 core. | | | |
| LPC4350_30_20_10 v.3.2 | 20120604 | Preliminary data sheet | - | LPC4350_30_20_10 v.3.1 |
| LPC4350_30_20_10 v.3.1 | 20120105 | Objective data sheet | - | LPC4350_30_20_10 v.3 |
| LPC4350_30_20_10 v.3 | 20111205 | Objective data sheet | - | LPC4350_30_20_10 v.2.1 |
| LPC4350_30_20_10 v.2.1 | 20110923 | Objective data sheet | - | LPC4350_30_20_10 v.2 |
| LPC4350_30_20_10 v.2 | 20110714 | Objective data sheet | - | LPC4350_30_20_10 v.1 |
| LPC4350_30_20_10 v.1 | 20101029 | Objective data sheet | - | - |


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|---|---|---|
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