

Product Description

The PE42422 is a HaRP™ technology-enhanced SPDT RF switch designed to cover a broad range of applications from 100-6000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface and requires no external components.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS® process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Features

- Symmetric SPDT reflective switch
- Low insertion loss
 - 0.25 dB typical @ 1000 MHz
 - 0.40 dB typical @ 3000 MHz
 - 0.65 dB typical @ 5000 MHz
 - 0.90 dB typical @ 6000 MHz
- Wide supply range of 2.3V to 5.5V
- Excellent linearity
 - IIP2 of 115 dBm
 - IIP3 of 70 dBm
- High ESD tolerance
 - 4kV HBM on RF pins to GND
 - 1kV on all other pins
- Logic Select (LS) pin provides maximum flexibility of control logic
- 12-lead 2x2 mm QFN package

Figure 1. Functional Diagram

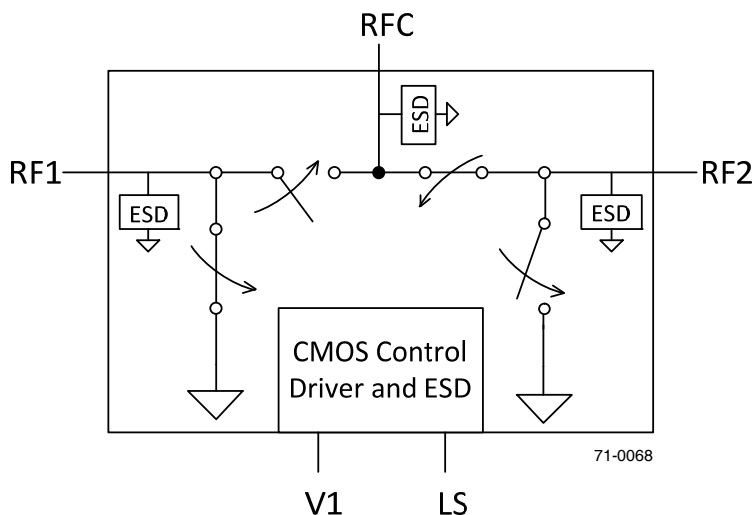


Figure 2. Package Type

12-lead 2x2x0.55 mm QFN

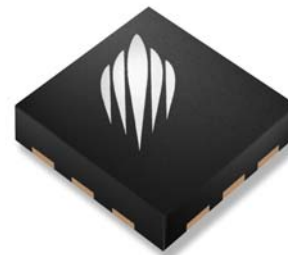


Table 1. Electrical Specifications Temp = 25°C¹, V_{DD} = 2.3V to 5.5V (Z_S = Z_L = 50Ω)

Parameter	Path	Condition	Min	Typ	Max	Units
Operational Frequency			100		6000	MHz
Insertion Loss ²	RFX to RFC	100-1000 MHz		0.25	0.35	dB
		1000-2000 MHz		0.30	0.40	dB
		2000-3000 MHz		0.40	0.50	dB
		3000-4000 MHz		0.50	0.70	dB
		4000-5000 MHz		0.65	0.90 ²	dB
		5000-6000 MHz		0.90	1.25 ²	dB
Isolation	RFX to RFC	100-1000 MHz	42	44		dB
		1000-2000 MHz	33	35		dB
		2000-3000 MHz	27	29		dB
		3000-4000 MHz	22	24		dB
		4000-5000 MHz	18	20		dB
		5000-6000 MHz	15	17		dB
Isolation	RFX to RFX	100-1000 MHz	40	41		dB
		1000-2000 MHz	32	33		dB
		2000-3000 MHz	26	28		dB
		3000-4000 MHz	22	24		dB
		4000-5000 MHz	18	20		dB
		5000-6000 MHz	15	16		dB
Return Loss ²	RFX to RFC	100-1000 MHz		28		dB
		1000-2000 MHz		21		dB
		2000-3000 MHz		20		dB
		3000-4000 MHz		18		dB
		4000-5000 MHz		16 ²		dB
		5000-6000 MHz		13 ²		dB
2nd Harmonic	RFX-RFC	+32 dBm output power, 850 / 900 MHz		-99		dBc
		+32 dBm output power, 1800 / 1900 MHz		-101		dBc
3rd Harmonic	RFX-RFC	+32 dBm output power, 850 / 900 MHz		-93		dBc
		+32 dBm output power, 1800 / 1900 MHz		-87		dBc
IMD3	RF-RFC	Bands I, II, V, VIII +17 dBm CW @ TX freq at RFC, -15 dBm CW @ 2Tx-Rx at RFC, 50Ω		-115		dBm
IIP2	RFX	100-6000 MHz		115		dBm
IIP3	RFX	100-6000 MHz		70		dBm
Input 0.1 dB Compression	RFX or RFC	100-6000 MHz		34		dBm
Switching Time		50% CTRL to (10%-90%) or (90%-10%) RF		2	4	μs

Notes: 1. Typical performance over temperature and V_{DD} shown in *Figure 4* through *Figure 20*

2. High frequency performance can be improved by external matching (see *Figure 21* through *Figure 26* and *Figure 29*)

Figure 3. Pin Configuration (Top View)

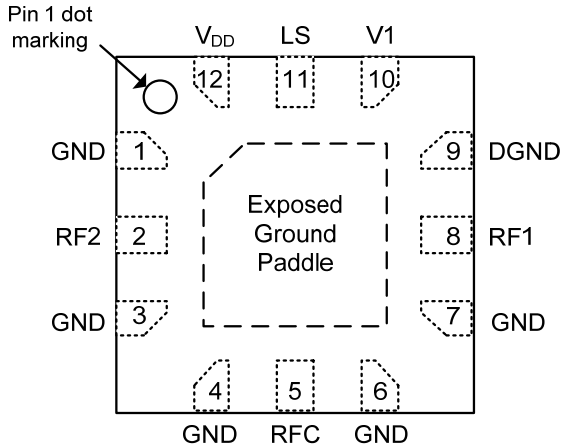


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	RF2 ¹	RF Port 2
3	GND	Ground
4	GND	Ground
5	RFC ¹	RF Common
6	GND	Ground
7	GND	Ground
8	RF1 ¹	RF Port 1
9	DGND	Digital Ground
10	V1	Switch control input, CMOS logic level
11	LS	Logic Select, CMOS logic level
12	V _{DD}	Supply
Paddle	GND	Ground for proper device operation

Note 1: Blocking capacitors needed only when non-zero DC voltage present

Table 3. Truth Table

Path	V1	LS
RFC-RF2	1	1
RFC-RF1	0	1
RFC-RF1	1	0
RFC-RF2	0	0

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Units
V _{DD} Supply Voltage	2.3	3.3	5.5	V
I _{DD} Power Supply Current		120	200	μA
RFX-RFC input power (50Ω)			+32	dBm
Control Voltage High	1.2	1.5	3.3	V
Control Voltage Low	0	0	0.5	V
Operating temperature range	-40	+25	+85	°C

Table 5. Absolute Maximum Ratings

Parameter/Conditions	Min	Max	Units
P _{MAX} Input Power ¹		+32	dBm
ESD Voltage HBM ²			
RF pins to GND		4000	V
All other pins		1000	V
ESD Voltage MM, all pins ³		200	V
T _{ST} Storage Temperature	-65	+150	°C

Notes: 1. V_{DD} within operating range specified in Table 4
2. HBM ESD Voltage (MIL-STD 883 Method 3015.7)
3. MM ESD Voltage (JEDEC JESD22-A115-A)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42422 in the 12-lead 2x2x0.55 mm QFN package is MSL1.

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 4. Insertion Loss RFX¹

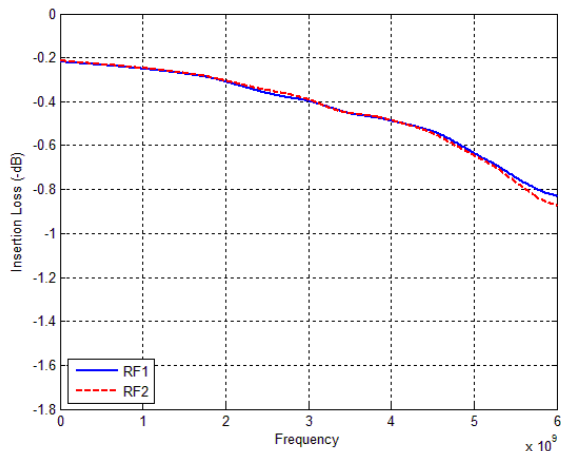


Figure 5. Insertion Loss vs Temp (RF1-RFC)¹

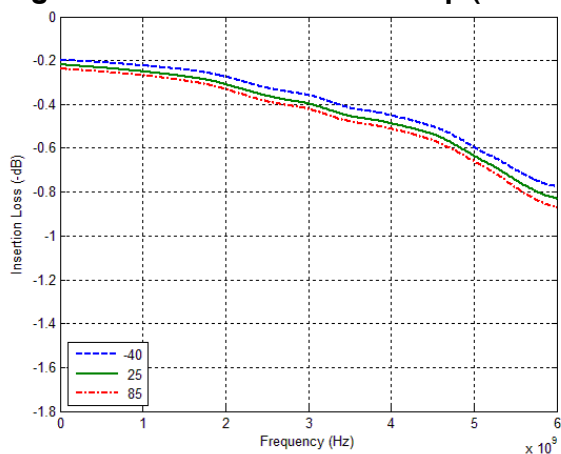


Figure 6. Insertion Loss vs Temp (RF2-RFC)¹

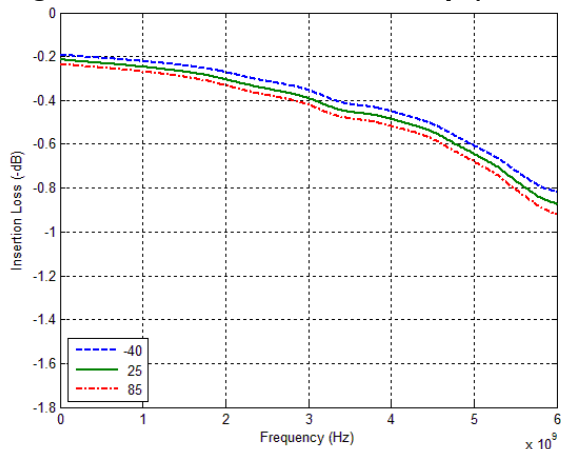


Figure 7. Insertion Loss vs V_{DD} (RF1-RFC)¹

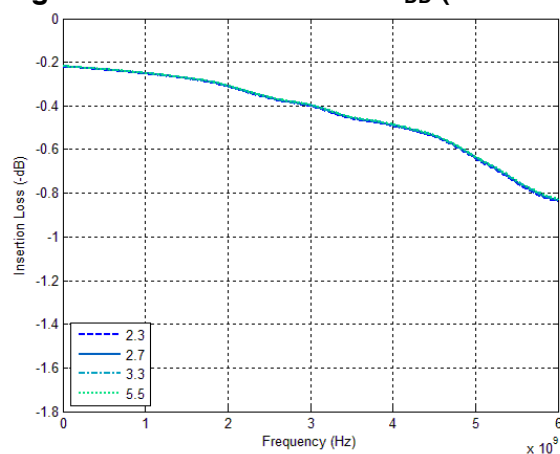
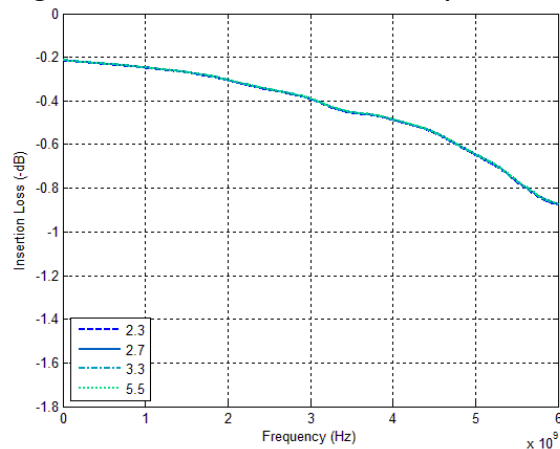


Figure 8. Insertion Loss vs V_{DD} (RF2-RFC)¹



Note 1: High frequency performance can be improved by external matching (see Figure 21 through Figure 26 and Figure 29)

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 9. RFX-RFX Isolation vs Temp

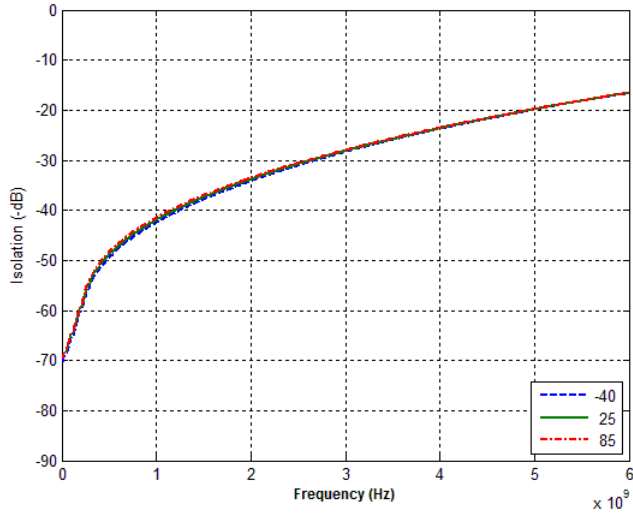


Figure 10. RFX-RFX Isolation vs V_{DD}

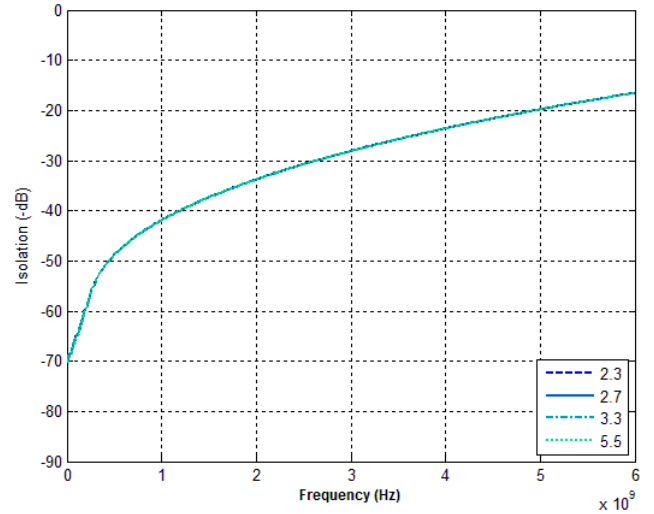


Figure 11. RFC-RFX Isolation vs Temp

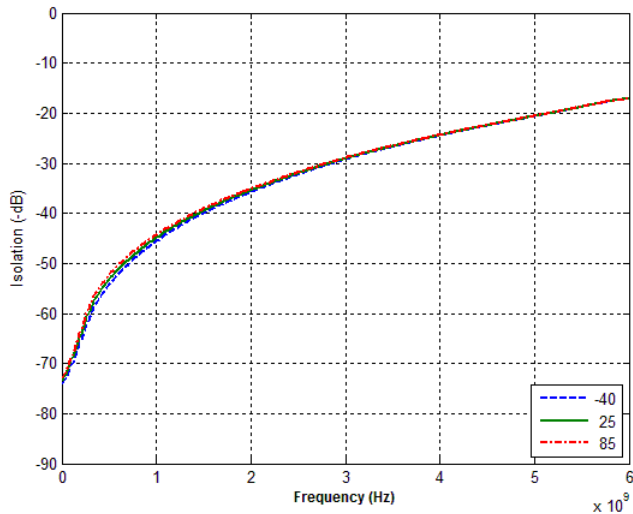
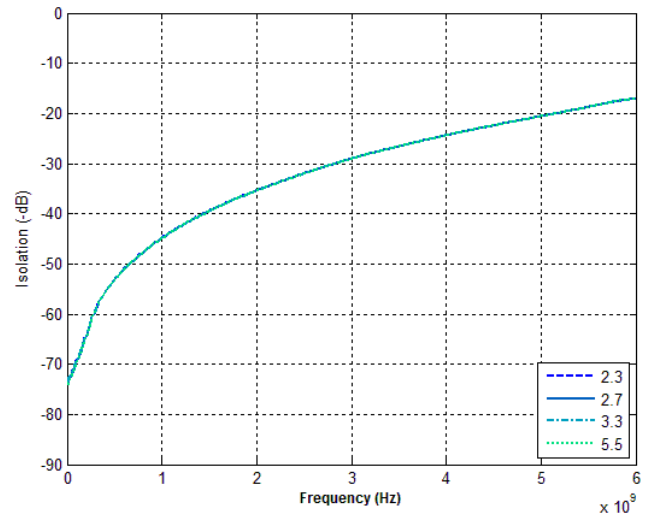


Figure 12. RFC-RFX Isolation vs V_{DD}



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 13. RFC Port Return Loss vs Temp (RF1 Active)¹

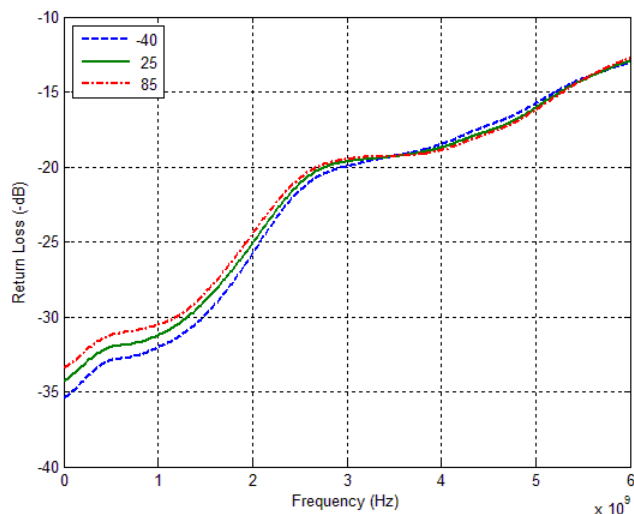


Figure 14. RFC Port Return Loss vs V_{DD} (RF1 Active)¹

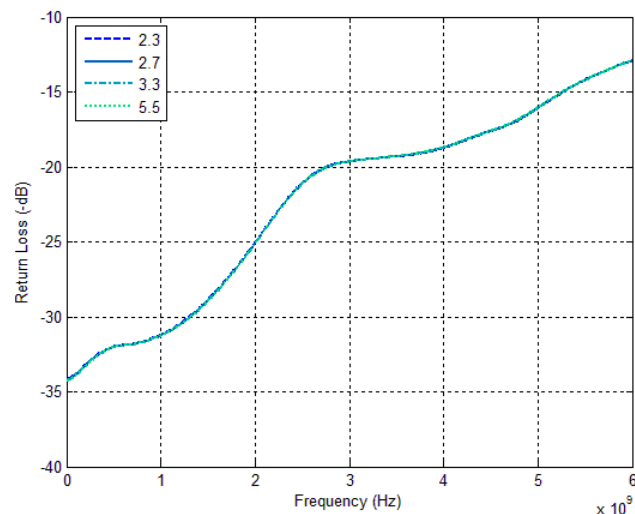


Figure 15. RFC Port Return Loss vs Temp (RF2 Active)¹

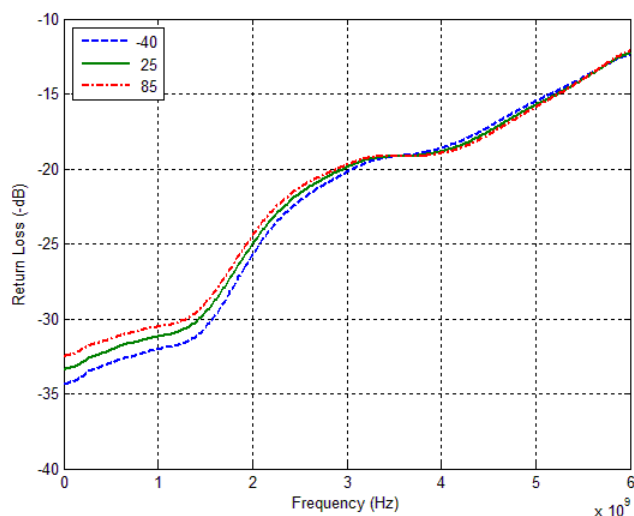
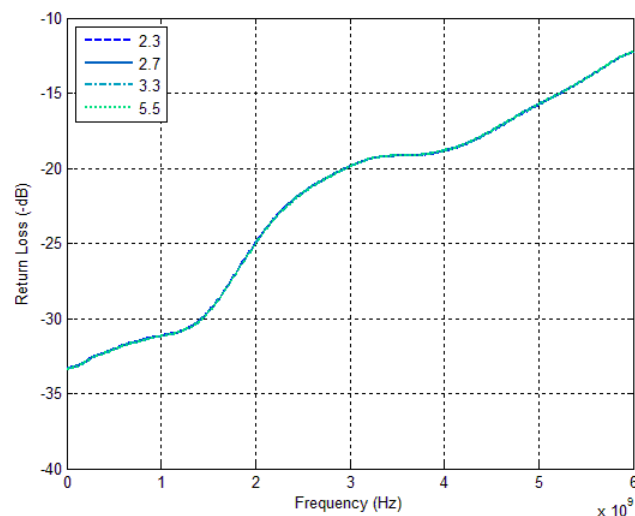


Figure 16. RFC Port Return Loss vs V_{DD} (RF2 Active)¹



Note 1: High frequency performance can be improved by external matching (see Figure 21 through Figure 26 and Figure 29)

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 17. Active Port Return Loss vs Temp (RF1 Active)¹

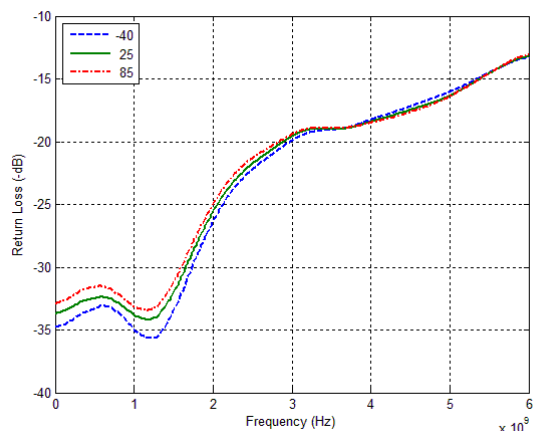


Figure 18. Active Port Return Loss vs V_{DD} (RF1 Active)¹

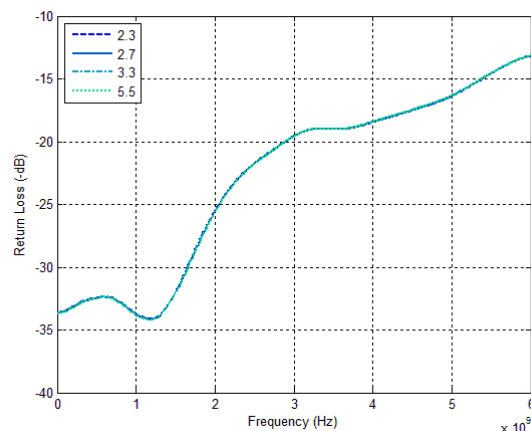


Figure 19. Active Port Return Loss vs Temp (RF2 Active)¹

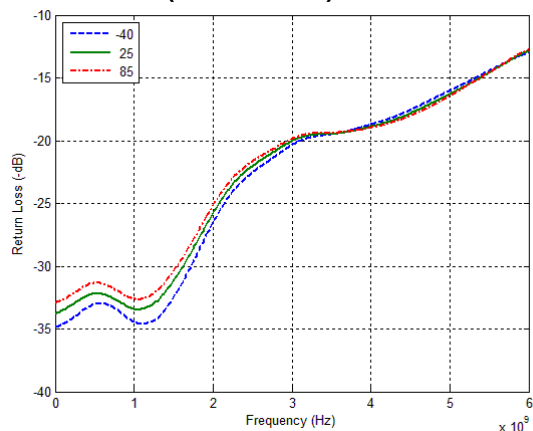
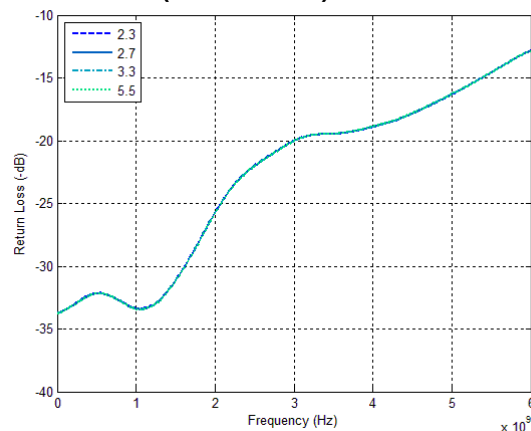


Figure 20. Active Port Return Loss vs V_{DD} (RF2 Active)¹



Note 1: High frequency performance can be improved by external matching (see Figure 21 through Figure 26 and Figure 29)

Performance Comparison @ 25°C and $V_{DD} = 3.3V$ with or without matching

Figure 21. Insertion Loss RF1¹

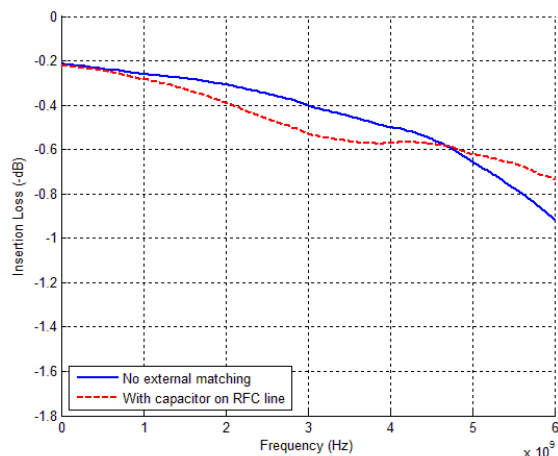


Figure 22. Insertion Loss RF2¹

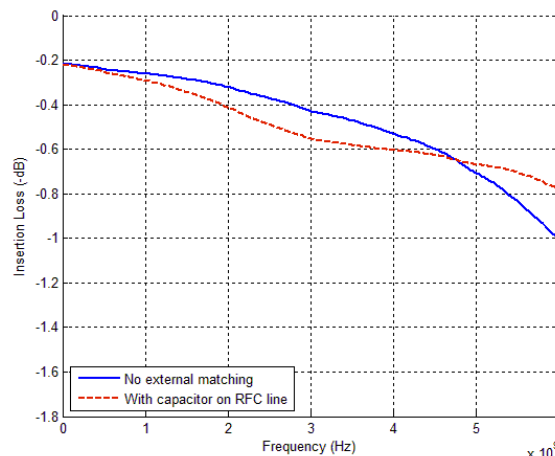


Figure 23. Active Port Return Loss (RF1 Active)¹

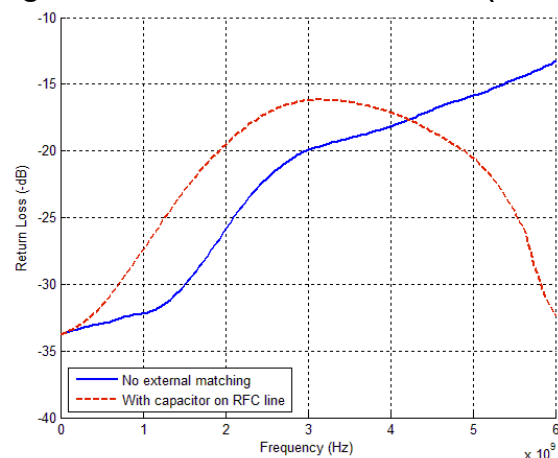


Figure 24. Active Port Return Loss (RF2 Active)¹

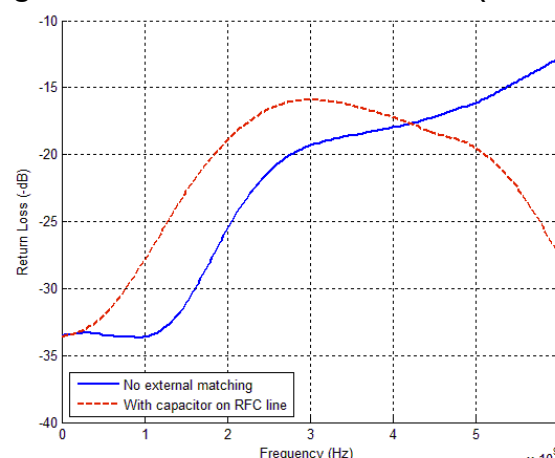


Figure 25. RFC Port Return Loss (RF1 Active)¹

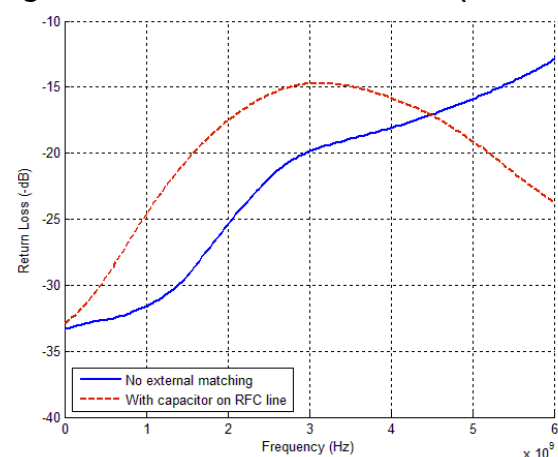
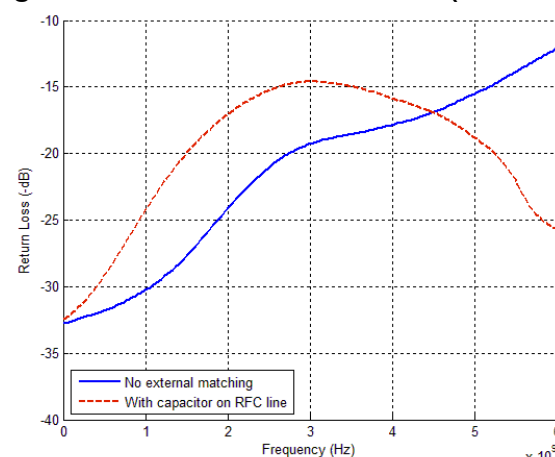


Figure 26. RFC Port Return Loss (RF2 Active)¹



Note 1: High frequency performance can be improved by external matching (see Figure 21 through Figure 26 and Figure 29)

Evaluation Board

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42422. The RF common port is connected through a 50 Ω transmission line via the top SMA connector, J2. RF1 and RF2 ports are connected through 50 Ω transmission lines via SMA connectors J1 and J3, respectively. A through 50 Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. J8 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top and bottom RF layers are Rogers RO4350 material with a 10 mil RF core. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 22 mils, trace gaps of 7 mils, and metal thickness of 2.1 mils.

Figure 27. Evaluation Board Layout

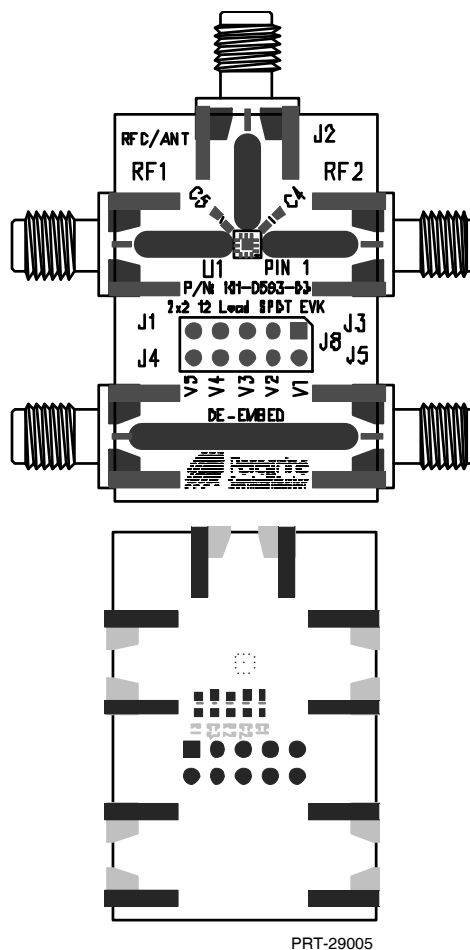


Figure 28. Evaluation Board Schematic

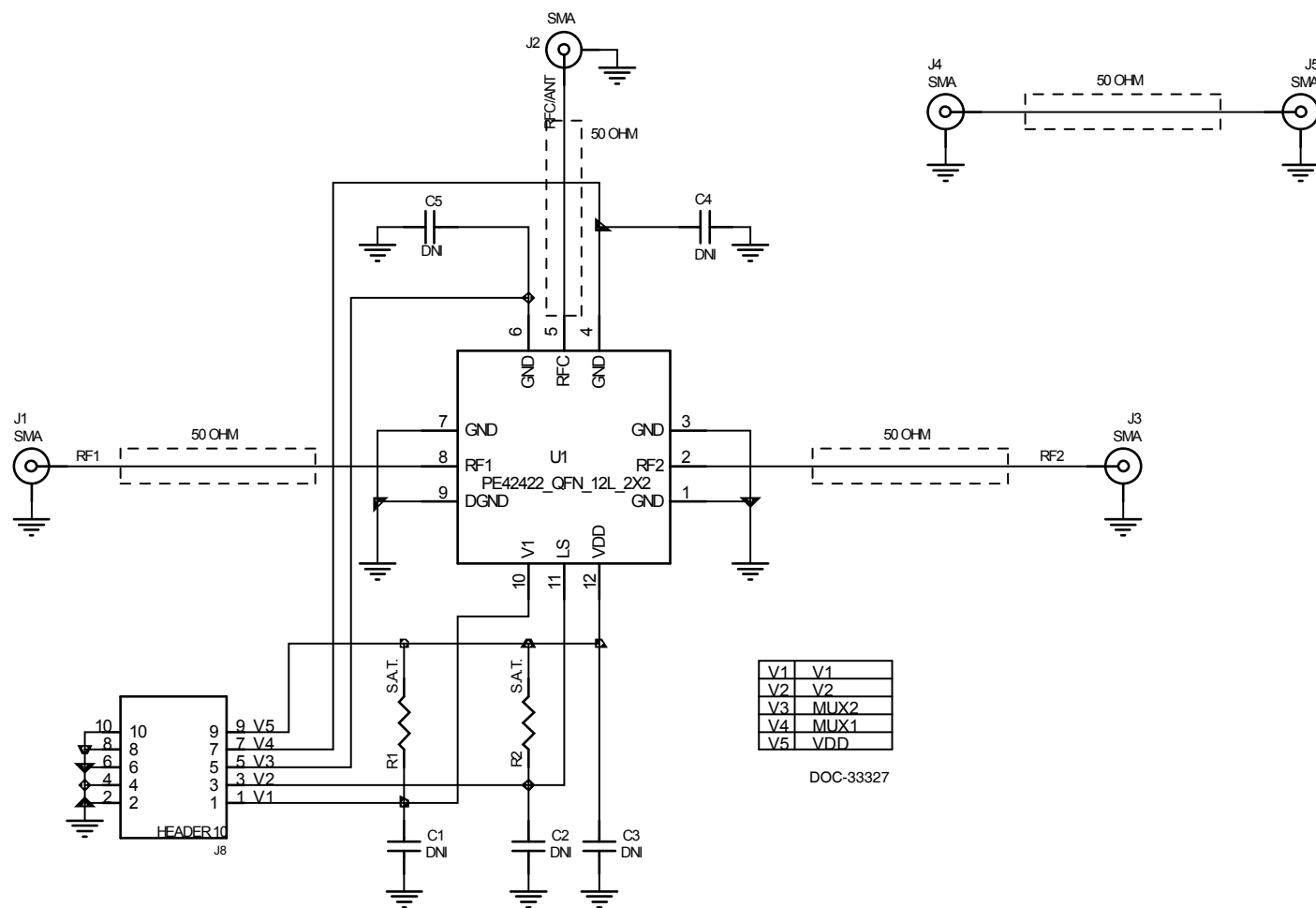


Figure 29. Evaluation Board Schematic with Matching

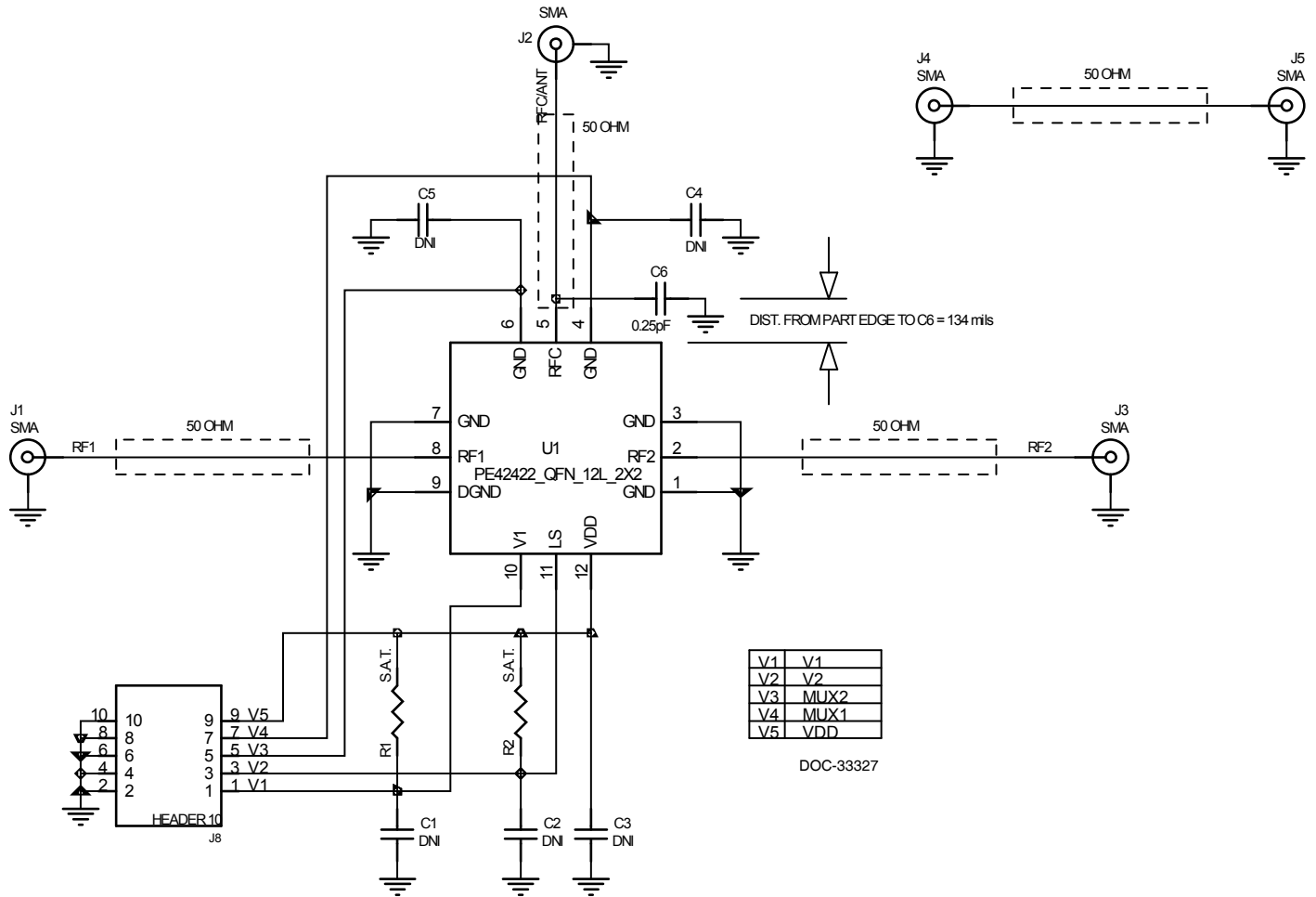


Figure 30. Package Drawing
12-lead 2x2x0.55 mm QFN

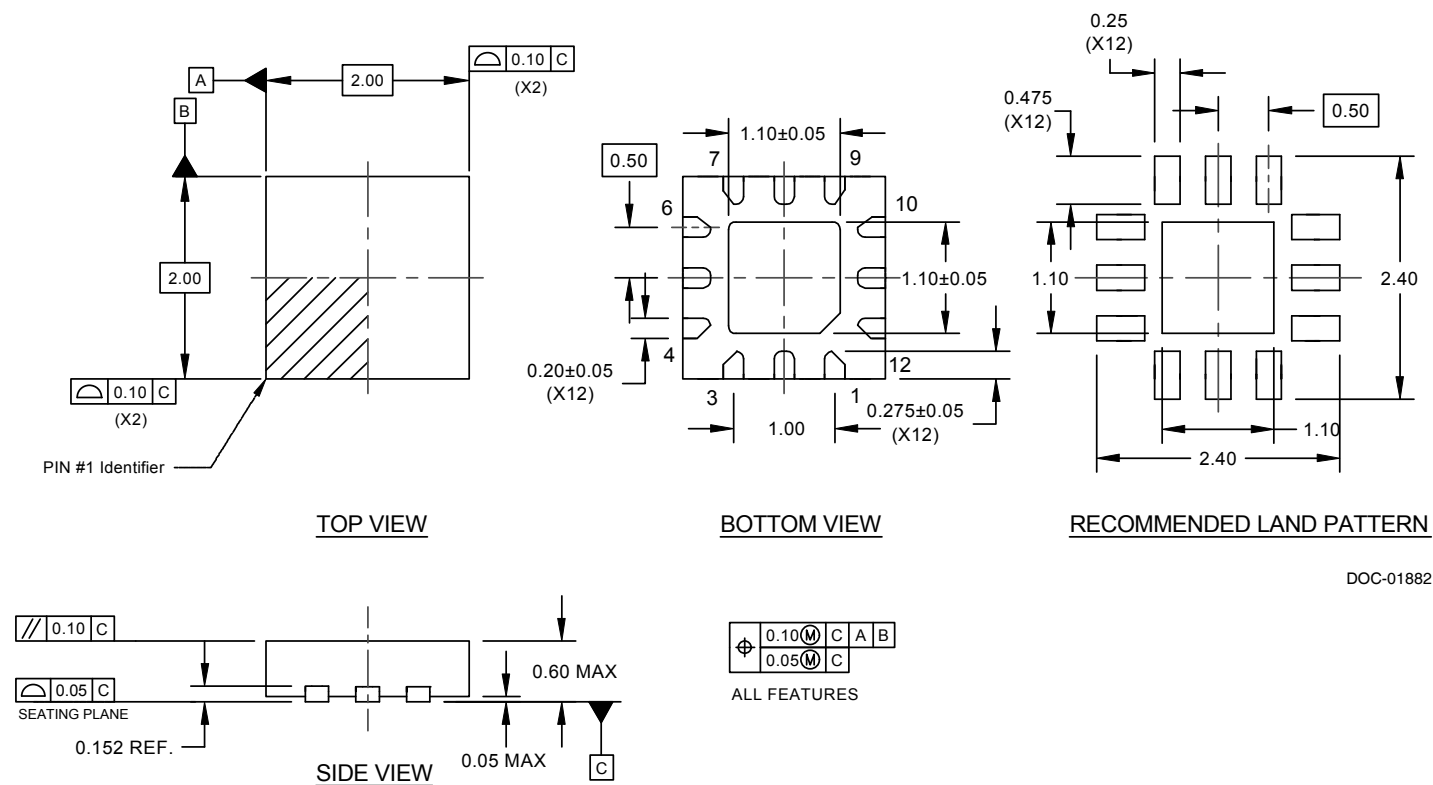
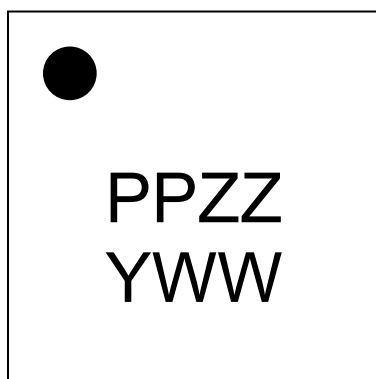


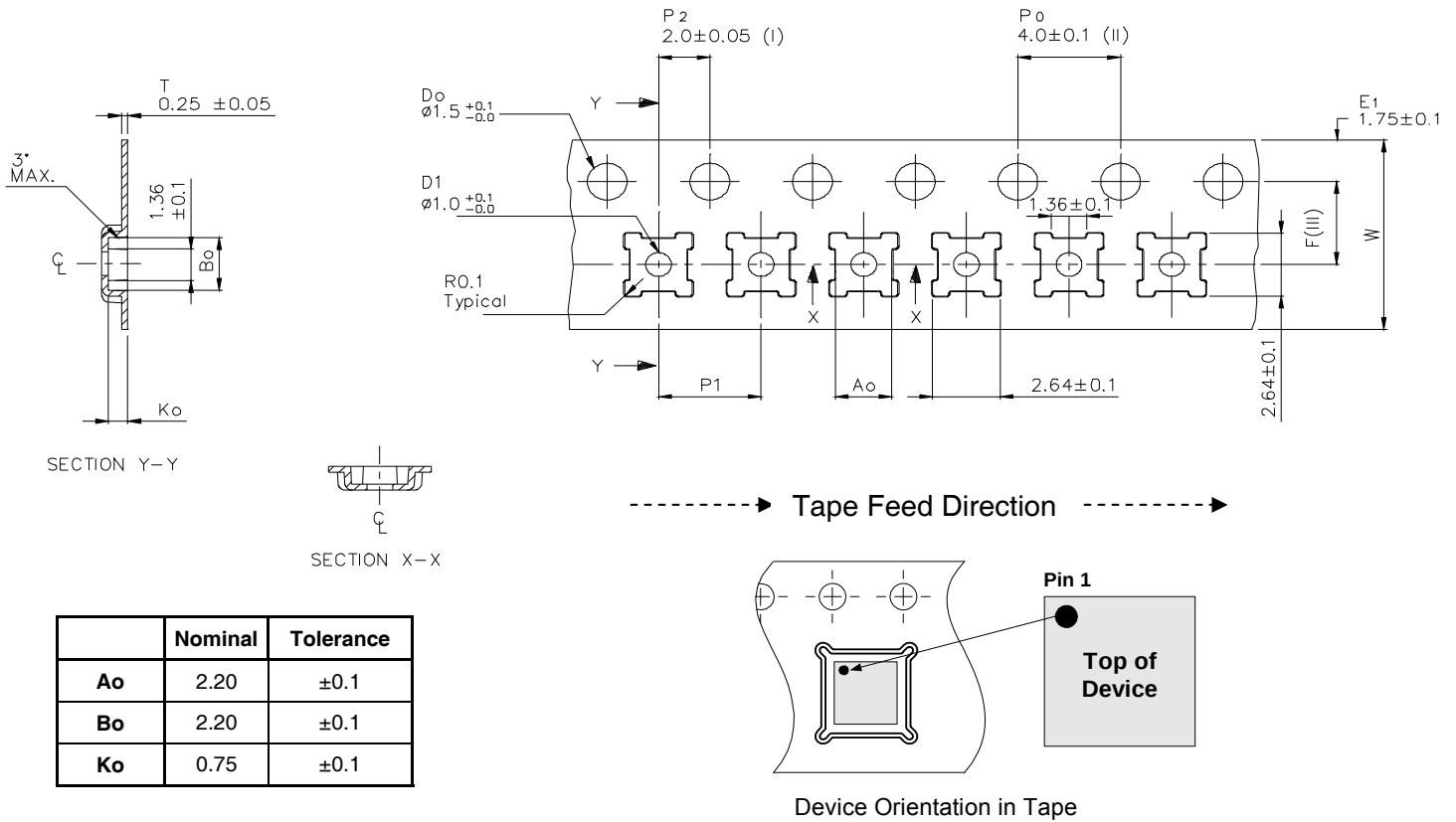
Figure 31. Top Marking Specifications



17-0112

Marking Spec Symbol	Package Marking	Definition
PP	DE	Part number marking for PE42422
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week

Figure 32. Tape and Reel Specifications
12-lead 2x2x0.55 mm QFN



- (I) Measured from centreline of sprocket hole to centreline of pocket.
 (II) Cumulative tolerance of 10 sprocket holes is ± 0.10 .
 (III) Measured from centreline of sprocket hole to centreline of pocket.
 (IV) Other material available.

This part shall not contain any banned substance as Sony standard SS-00259

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
PE42422MLAA-Z	PE42422 SPDT RF Switch	Green 12-lead 2x2mm QFN	3000 units T/R
EK42422-01	PE42422 Evaluation board	Evaluation Kit	1/Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).
 The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: <http://patents.psemi.com>.