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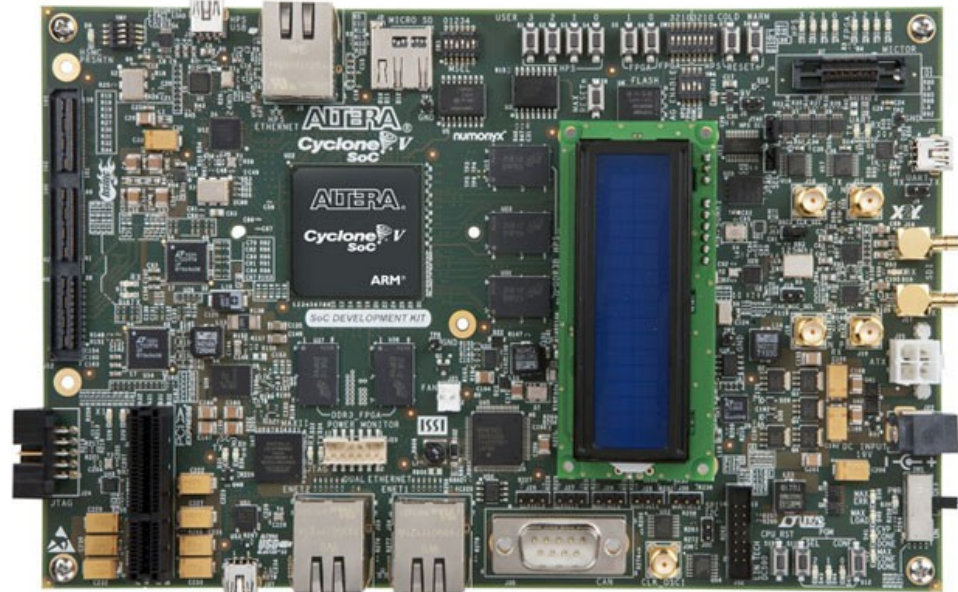
Cyclone V SoC Development Kit and SoC Embedded Design Suite

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from **Altera**

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Figure 1: Photograph of the Cyclone V SX SoC Development Board

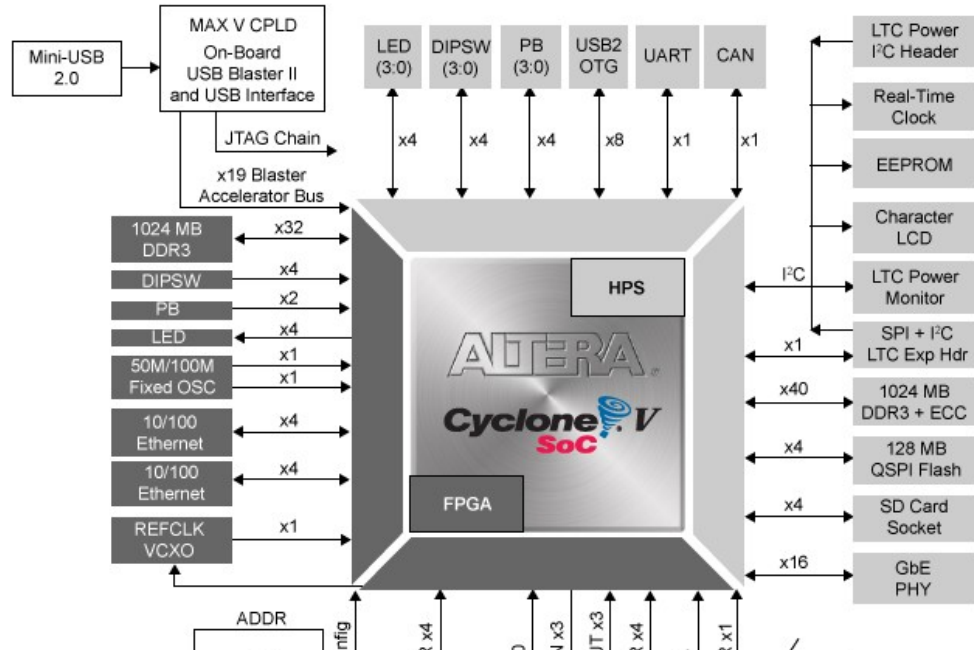


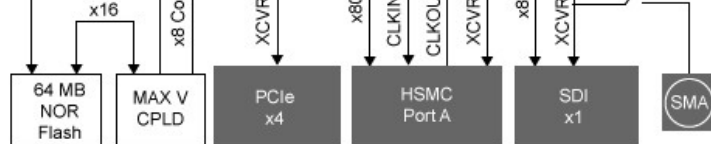
The Altera® Cyclone® V SoC Development Kit offers a quick and simple approach to develop custom ARM® processor-based SOC designs accompanied by Altera's low-power, low-cost Cyclone V FPGA fabric. This kit supports a wide range of functions, such as:

- Processor and FPGA prototyping and power measurement
- Industrial networking protocols
- Motor control applications*
- Acceleration of image- and video-processing applications*
- PCI Express® (PCIe®) x4 lane with ~1,000 MBps transfer rate (endpoint or rootport)

*Application-specific daughtercards, available separately, supporting a wide range of I/O and interface standards.

Figure 2: Schematic of the Cyclone V SX SoC Development Board





Ordering Information

Table 1. Altera's Cyclone V SoC Development Kit Ordering Information

Ordering Code	Price	Ordering Information
DK-DEV-5CSXC6NES	\$1,595 Buy Now ▶	The Cyclone V SoC Development Kit features a 5CSXFC6D6F31C8NES SoC. Buy online via Altera's eStore or contact your local Altera distributors or sales representative to place your order.

Development Kit Contents

The Cyclone V SoC Development Kit features the following:

- Cyclone V SX development board (see Figure 1)
 - Featured devices
 - Cyclone V SX SoC—5CSXFC6D6F31C8NES (SoC)
 - MAX® V CPLD—5M2210ZF256C4N (system controller)
 - MAX II CPLD—EPM570GF100 (embedded USB-Blaster™ II cable)
 - FPGA configuration sources
 - Embedded USB-Blaster II (JTAG) cable
 - EPCQ flash (PFL)
 - Hard processor system (HPS)
 - FPGA memory
 - 1 GB DDR3 SDRAM (32 bit)
 - FPGA I/O interfaces
 - 2X 10/100 Ethernet PHYs (EtherCAT)
 - PCIe Gen 1 x4 female connector
 - Universal high-speed mezzanine card (HSMC)—x4 transceivers, x16 TX LVDS, x16 RX LVDS
 - One serial digital interface (SDI) channel
 - Four SMAs for one transceiver channel
 - x4 push buttons
 - x2 switches
 - x4 LEDs
 - HPS boot sources
 - 128 MB QSPI Flash
 - Removable micro-SDCard flash
 - FPGA
 - HPS memory
 - 1 GB DDR3 SDRAM (32 bit) with error correction code (ECC)
 - 128 MB QSPI flash
 - Micro-SDCard socket with 4 GB micro-SDCard flash device
 - HPS I/O interfaces
 - x1 USB 2.0 On-the-Go (OTG)
 - x1 10/100/1000 Gigabit Ethernet (10GbE/100GbE/1000GbE)
 - x1 CAN
 - x1 UART (UART to USB bridge)
 - x1 real-time clock (with battery backup)
 - x1 two-line text LCD
 - 1-/2-channel, 20 bit delta-sigma analog-to-digital converter (Linear Technology LTC2422)
 - x4 push buttons
 - x4 switches
 - x4 LEDs
 - Clocking
 - Four-output programmable clock generator for FPGA reference clock inputs
 - 125 MHz LVDS oscillator for FPGA reference clock input
 - 148.5 MHz LVDS programmable voltage-controlled crystal oscillator (VCXO) for FPGA reference clock input
 - 50 MHz single-ended oscillator for FPGA and MAX V FPGA clock input
 - 100 MHz single-ended oscillator for MAX V FPGA configuration clock input
 - SMA input for HPS clock
 - Power
 - Laptop DC input 14—20 V adapter
 - System monitoring circuit
 - Power (voltage, current, wattage)
 - HSMC breakout board
 - HSMC loopback board
 - Mechanical
 - Board dimensions—8.19" x 5.22"
- Cyclone V SX FPGA Development Kit software content (downloadable from Table 2)
- Design examples
 - Board test system (BTS)*
 - Golden System Reference Design with Board Update Portal web server
- Complete documentation (see Table 2)
- [SoC Embedded Design Suite Subscription Edition](#)
 - ARM Development Studio 5 (DS-5™) Altera Edition Toolkit
 - Hardware-to-software handoff tools
 - Linux run-time software for application development
 - SoC hardware libraries for firmware development
 - Application examples
- Free software supported by Quartus® II software v13.0, Web Edition

* Watch the [video](#) to learn more.

Available Documentation

Table 2. Altera's Cyclone V SoC Development Kit Ordering Information

Document	Description	Version
Cyclone V SoC Development Kit User Guide (PDF) (COMING SOON)	Information about setting up the Cyclone V SoC Development Board and using the included software.	1.0
Cyclone V SoC Development Board Reference Manual (PDF) (COMING SOON)	Detailed information about board components and interfaces.	1.0
Kit installation (Windows) Kit installation (Linux)	Full installation of all files including reference manual, user guide, quick start guide, BOM, layout, PCB, schematics, BUP example file, BTS example file, and others. BUP has been upgraded to use the Qsys system integration tool.	13.0

Note:

1. This kit installation works with Quartus II Web Edition software v13.0

Related Links

- [Documentation for Cyclone V devices](#)
- [Cyclone V SX transceiver protocols](#)
- [Partner high-speed mezzanine connector cards](#)
- [SoC training](#)

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