

SiGe WIDEBAND DIRECT QUADRATURE MODULATOR, 20 - 2700 MHz

Typical Applications

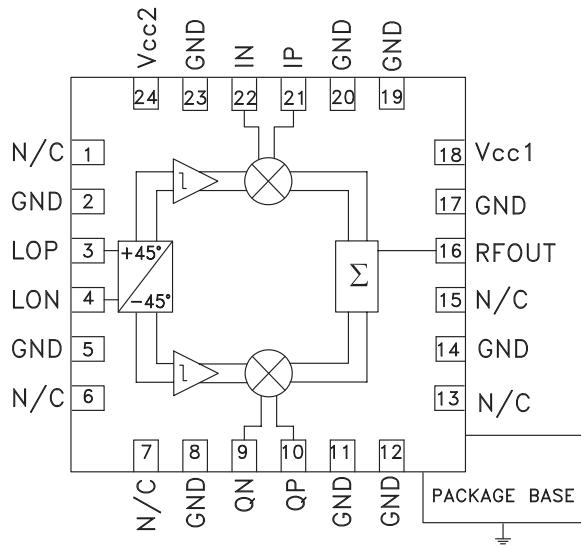
The HMC696LP4E is Ideal for:

- GMSK, QPSK, QAM, SSB Modulators
- Cellular/3G and WiMAX/4G
- Software Defined Radio
- Multi-Band Transmitters
- Test Equipment

Features

- Very Low Noise Floor, -162 dBm/Hz
- Excellent Carrier & Sideband Suppression
- Very High Linearity, +23.7 dBm OIP3
- High Output Power, +8.5 dBm Output P1dB
- High Modulation Accuracy
- 24 Lead 4x4 mm QFN Package: 16 mm²

Functional Diagram



General Description

The HMC696LP4E is a low noise, high linearity Direct Quadrature Modulator RFIC which is ideal for digital modulation applications from 0.02 to 2.7 GHz including software defined radio and multi-band transmitters. Housed in a compact 4x4 mm (LP4) SMT QFN package, the RFIC requires minimal external components & provides a low cost alternative to more complicated double upconversion architectures. The RF output port is single-ended and matched to 50 Ohms with no external components. The LO requires 0 to +10 dBm and can be driven in either differential or single-ended mode. This device is optimized for a +5V supply, and offers improved carrier feedthrough and sideband suppression characteristics. For higher frequency applications, the HMC697LP4E Direct Modulator covers 450 - 4000 MHz.

Electrical Specifications, See Test Conditions on following page herein.

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Frequency Range, RF	20 - 40	40 - 100	100 - 450	450 - 960	960 - 1700	1700 - 2200	2200 - 2700	MHz
Output P1dB	7	8	8	8	7	6	5	dBm
Output Noise Floor		-160	-162	-163	-162	-162	-161	dBm/Hz
Output IP3	21	24	24	23	21	19	17	dBm
Output Power	0	1	1	0	-1	-2	-3	dBm
Carrier Feedthrough (uncalibrated)	-42	-42	-42	-42	-43	-45	-42	dBm
Sideband Suppression (uncalibrated)	-29	-40	-54	-42	-43	-42	-30	dBc
LO Port Return Loss	9	12	15	15	11	7	5	dB
RF Port Return Loss	29	28	29	31	30	24	20	dB



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Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Output					
RF Frequency Range		20		2700	MHz
RF Return Loss			27		dB
LO Input					
LO Frequency Range		20		2700	MHz
LO Input Power			0	10	dBm
LO Port Return Loss			10		dB
Baseband Input Port					
Baseband Input DC Voltage (Vbbdc)			1.5	1.7	V
Baseband Input DC Bias Current (Ibbdc)	Single-ended.		60		μA
Single-ended Baseband Input Capacitance	De-embed to the lead of the device.		4.5		pF
DC Power Requirements See Test Conditions Below					
Supply Voltage (Vcc1, Vcc2)		4.5	5	5.5	V
Supply Current (Icc1 + Icc2)		140	160	180	mA

Test Conditions: Unless Otherwise Specified, the Following Test Conditions Were Used

Parameter	Condition
Temperature	+25 °C
Baseband Input Frequency	200 kHz
Baseband Input DC Voltage (Vbbdc)	+1.5V
Baseband Input AC Voltage (Peak to Peak Differential, I and Q)	700 mV
Baseband Input AC Voltage for OIP3 Measurement (Peak to Peak Differential, I and Q)	700 mV per tone @ 150 & 250 kHz
Frequency Offset for Output Noise Measurements	30 MHz
Supply (Vcc1, Vcc2)	+5V
LO Input Power	0 dBm
LO Input Mode	Single-Ended through LOP
Mounting Configuration	Refer to HMC696LP4E Application Schematic Herein
Sideband & Carrier Feedthrough	Uncalibrated

Calibrated vs. Uncalibrated Test Results

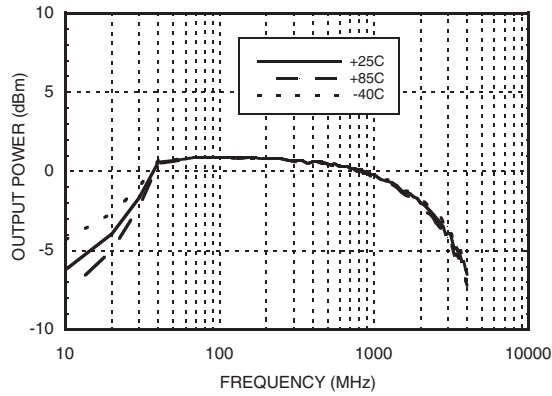
During the Uncalibrated Sideband and Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The “Uncalibrated, +25 °C” Sideband and Carrier Suppression plots were measured at room temperature, while the “Uncalibrated, over Temperature” Sideband and Carrier Suppression plots represent the worst case uncalibrated suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

The “Calibrated, + 25 °C” Sideband Suppression data was plotted after a manual adjustment of the I/Q amplitude balance and I/Q phase offset (skew) at +25 °C, and at each LO input power level. The +25 °C adjustment settings were held constant during tests over temperature. The “Calibrated, over Temperature” plots represent the worst case calibrated Sideband Suppression levels at T= -40 °C, +25 °C, and +85 °C.

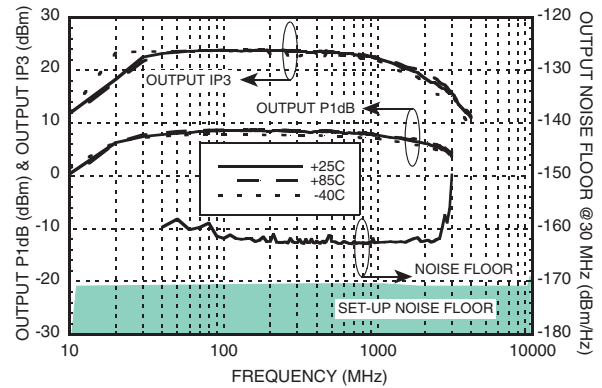
The “Calibrated, +25 °C” Carrier Suppression data was plotted after a manual adjustment of the Ip/In & Qp/Qn DC offsets at +25 °C, and at each LO input power level. The +25 °C adjustment settings were held constant during tests over temperature. The “Calibrated, over Temperature” plots represent the worst case Carrier Suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

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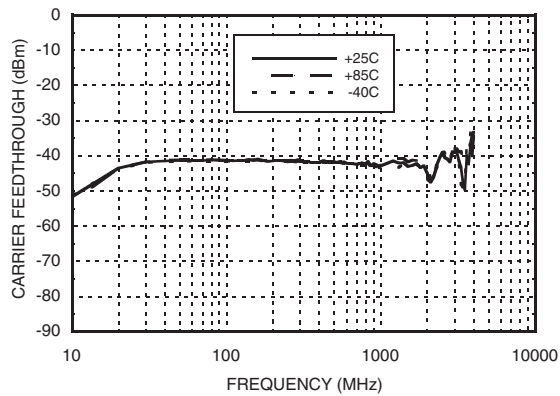
Wideband Performance vs. Frequency



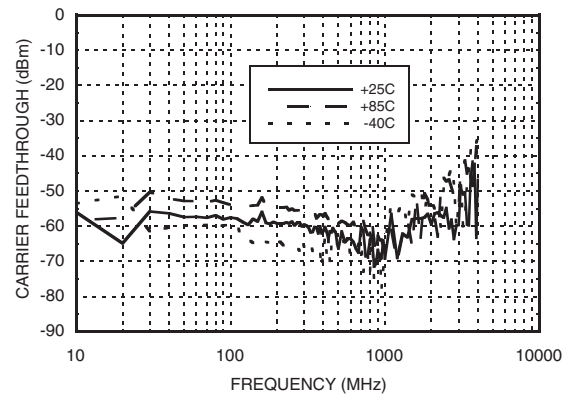
Output IP3, P1dB & Noise Floor @ 30 MHz Offset vs. Frequency



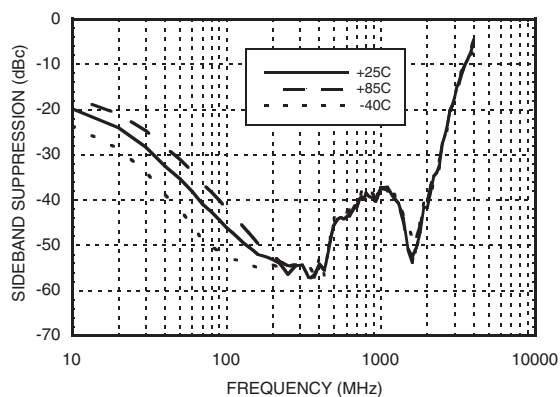
Uncalibrated Carrier Feedthrough [1] vs. Frequency Over Temperature



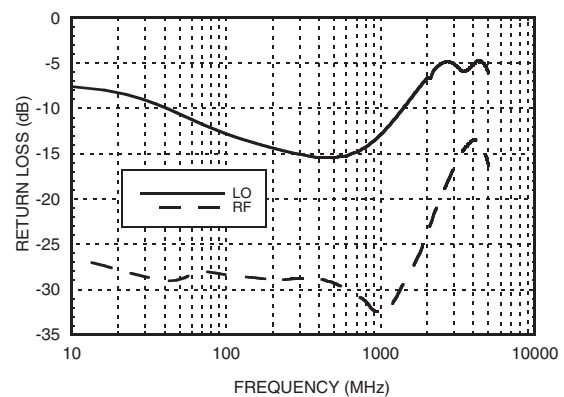
Calibrated Carrier Feedthrough [1] vs. Frequency Over Temperature



Sideband Suppression vs. Frequency



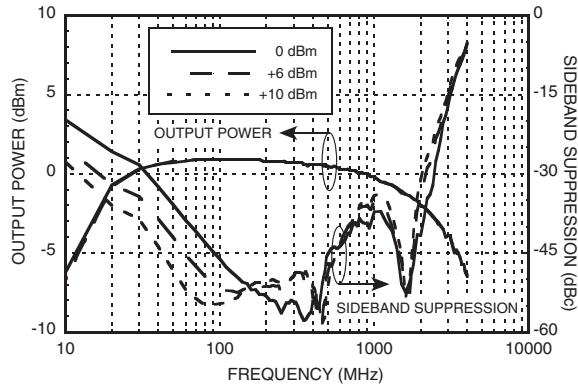
Return Loss vs. Frequency



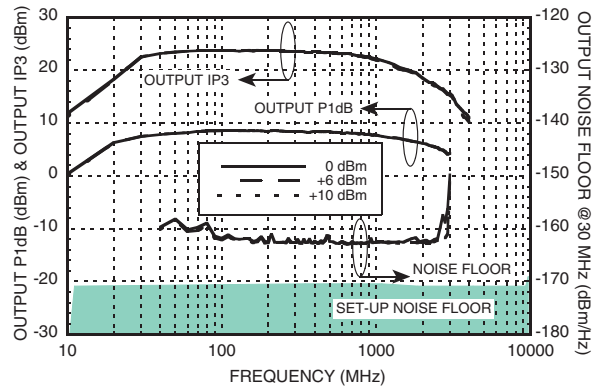
[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

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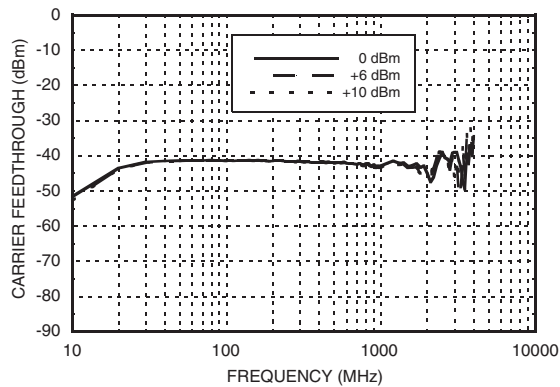
Wideband Performance vs. Frequency Over LO Power



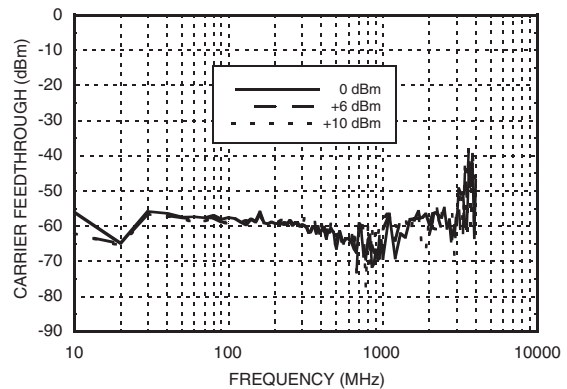
Output IP3, P1dB & Noise Floor @ 30 MHz Offset vs. Frequency Over LO Power



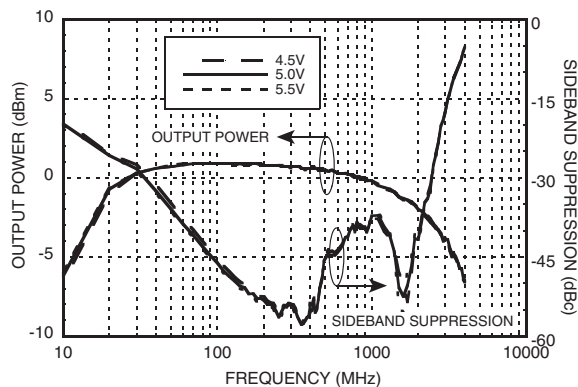
Uncalibrated Carrier Feedthrough [1] vs. Frequency Over LO Power



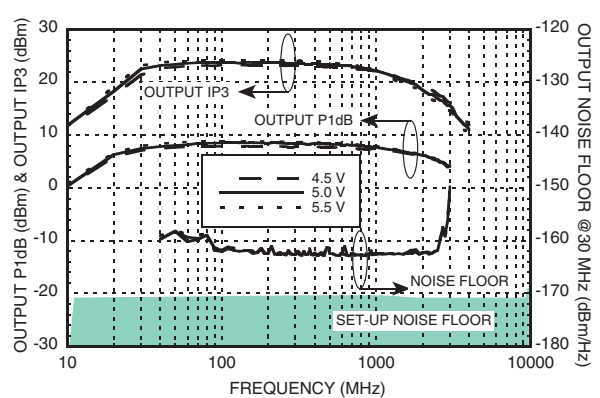
Calibrated Carrier Feedthrough [1] vs. Frequency Over LO Power



Wideband Performance vs. Frequency Over Supply Voltage



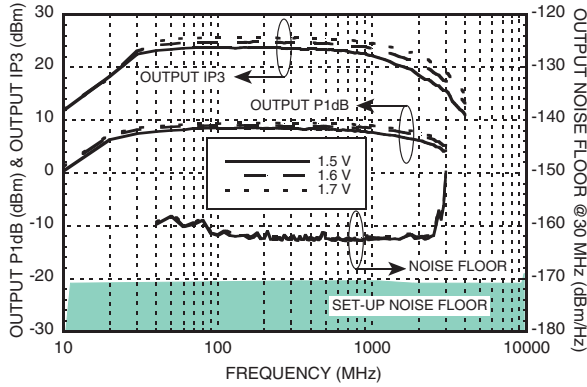
Output IP3, P1dB & Noise Floor @ 30 MHz Offset vs. Frequency Over Supply Voltage



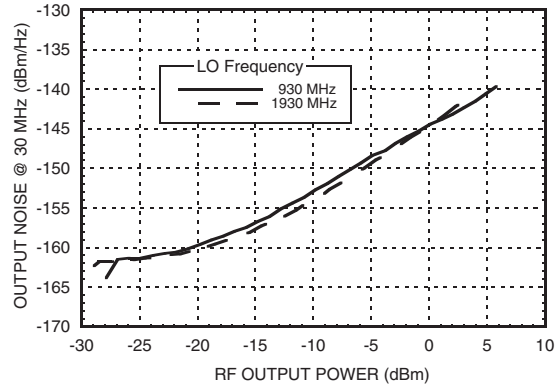
[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

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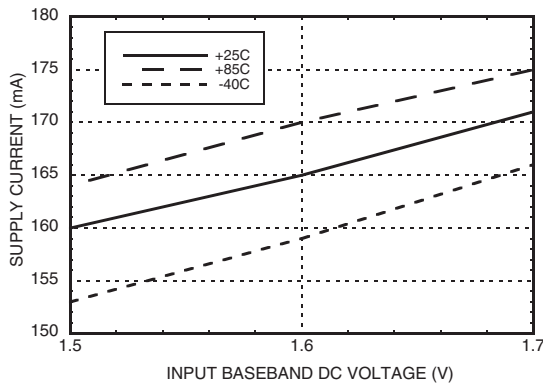
Output IP3, P1dB & Noise Floor @ 30 MHz Offset vs. Frequency Over Input Baseband DC Voltage



Output Noise @ 30 MHz Offset vs. RF Output Power



Supply Current vs. Input Baseband DC Voltage



Absolute Maximum Ratings

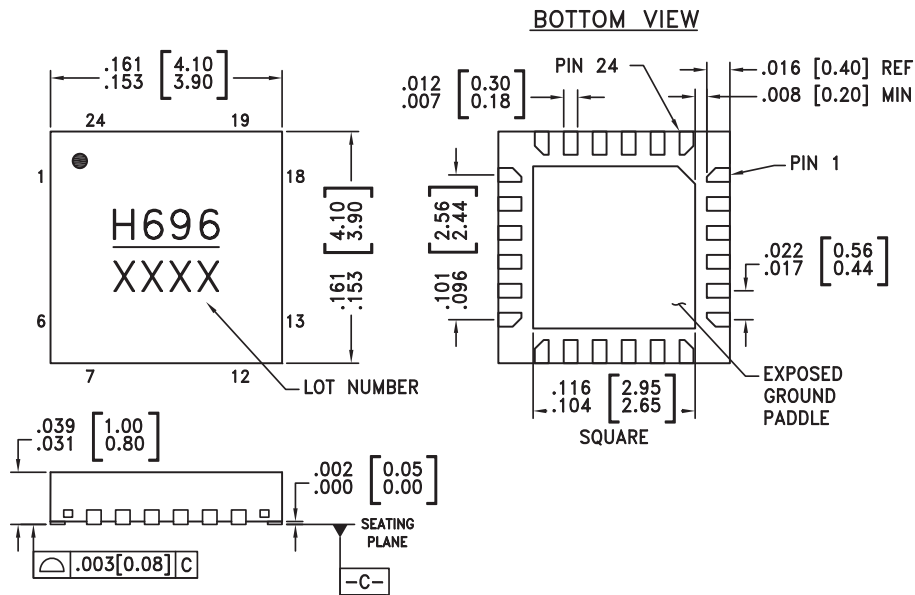
Vcc1, Vcc2	+6V
LO Input Power	+18 dBm
Baseband Input Voltage (AC + DC) (Reference to GND)	0V to +2.8V
Junction Temperature	150 °C
Continuous P _{diss} (T = 85°C) (Derate 30 mW/°C above 85°C)	1.8 Watts
Thermal Resistance (R _{th}) (junction to ground paddle)	34 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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Outline Drawing




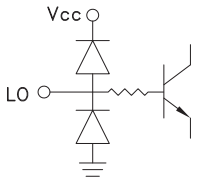
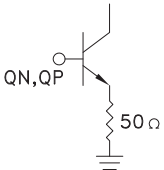
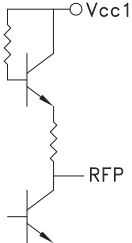
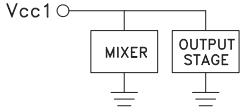
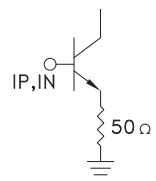
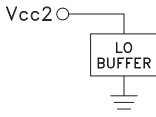
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[1]
HMC696LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H696 XXXX

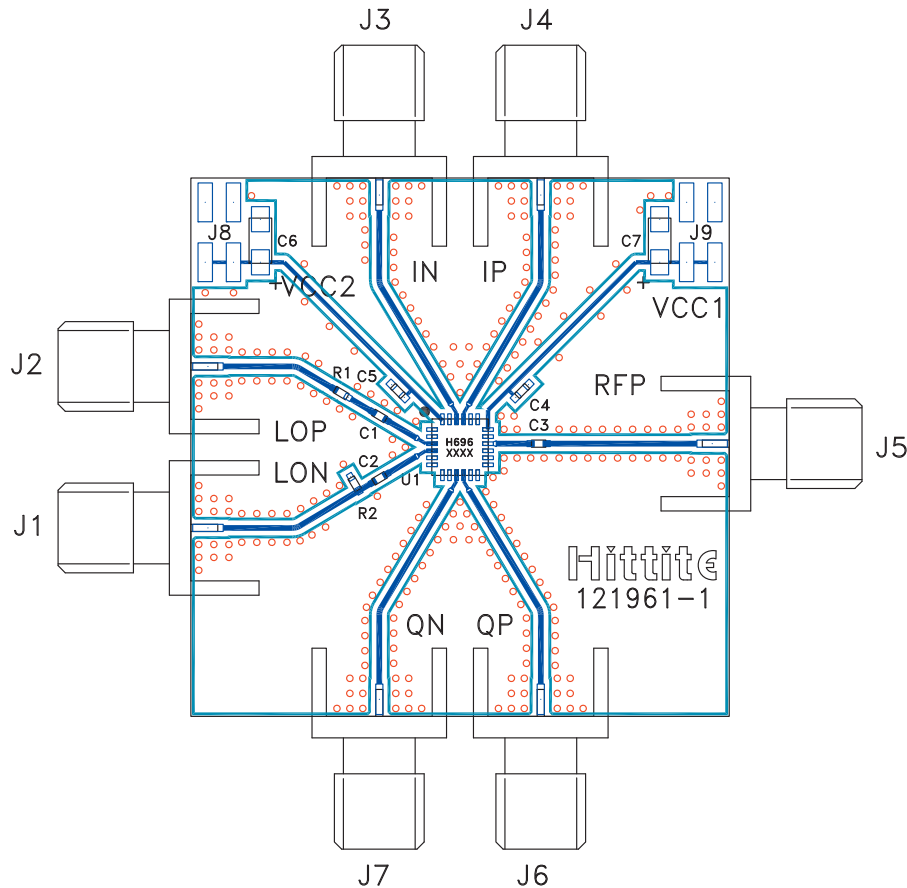
[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 7, 13, 15	N/C	Not connected.	
2, 5, 8, 11, 12, 14, 17, 19, 20, 23	GND	These pins and the ground paddle should be connected to a high quality RF/DC ground.	
3, 4	LOP, LON	LO inputs. Need DC decoupling capacitors. The ports could be driven single ended or differentially.	
9, 10	QN, QP	Q channel differential baseband input. These high impedance ports should be biased around 1.5V DC. Nominal recommended baseband input is around 700 mV pp differential.	
16	RFOUT	DC coupled and matched to 50 Ohms, output requires blocking capacitor.	
18	Vcc1	Supply voltage for the mixer and output stages 74mA @ +5V.	
21, 22	IP, IN	I channel differential baseband input. These high impedance ports should be at the same bias voltage (VbbDC) as QN & QP.	
24	Vcc2	Supply voltage for the LO stage 85mA @ +5V.	

Evaluation PCB



List of Materials for Evaluation PCB 121963 [1]

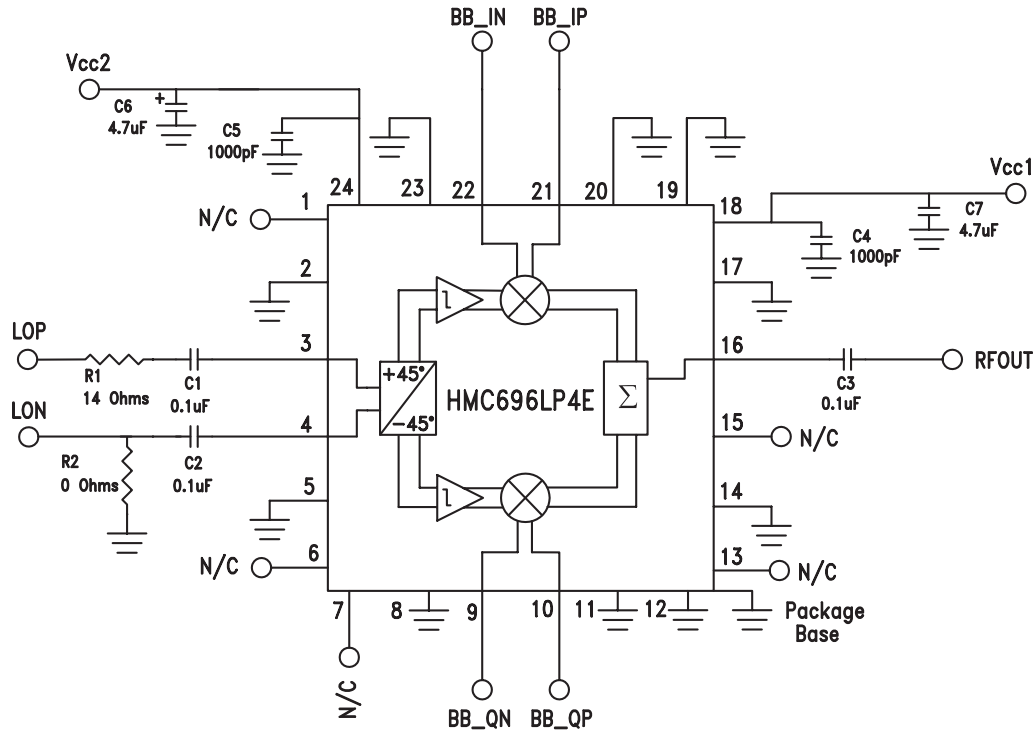
Item	Description
J1 - J7	PCB Mount SMA Connector
J8, J9	DC Molex Connector
C1 - C3	0.1 μ F Chip Capacitor, 0402 Pkg.
C4, C5	1000 pF Chip Capacitor, 0402 Pkg.
C6, C7	4.7 μ F, Case A, Tantalum
R1	14 Ohm Resistor, 0402 Pkg.
R2	0 Ohm Resistor, 0402 Pkg.
U1	HMC696LP4E Modulator
PCB [2]	121961 Eval Board

[1] Reference this number when ordering complete evaluation PCB

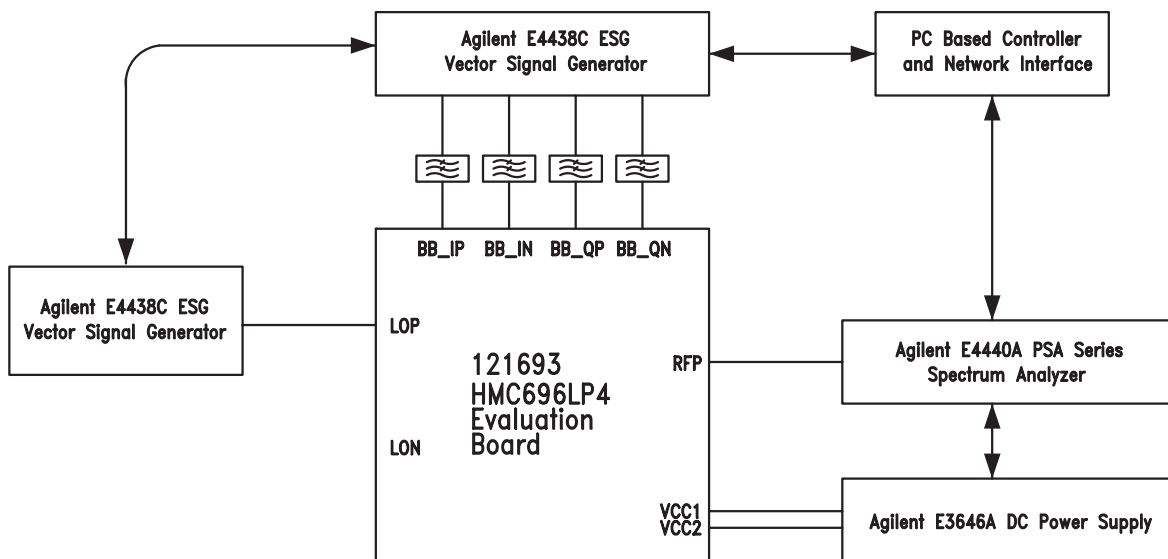
[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application & Evaluation PCB Schematic



Characterization Set-up





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Notes: