Ultrafast, 4 ns Single-Supply Comparators

Data Sheet

AD8611/AD8612

FEATURES

- 4 ns propagation delay at 5 V
- Single-supply operation: 3 V to 5 V
- 100 MHz input
- Latch function

APPLICATIONS

- High speed timing
- Clock recovery and clock distribution
- Line receivers
- Digital communications
- Phase detectors
- High speed sampling
- Read channel detection
- PCMCIA cards
- Zero-crossing detector
- High speed analog-to-digital converter (ADC)
- Upgrade for LT1394 and LT1016 designs

PIN CONFIGURATIONS

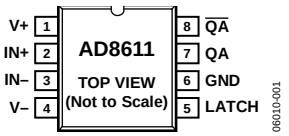

Figure 1. 8-Lead Narrow Body SOIC (R-8)

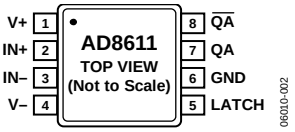

Figure 2. 8-Lead MSOP (RM-8)

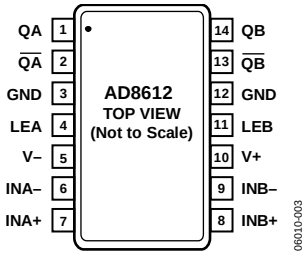

Figure 3. 14-Lead TSSOP (RU-14)

GENERAL DESCRIPTION

The AD8611/AD8612 are single and dual 4 ns comparators with latch function and complementary output. The latch is not functional if V_{CC} is less than 4.3 V.

Fast 4 ns propagation delay makes the AD8611/AD8612 good choices for timing circuits and line receivers. Propagation delays for rising and falling signals are closely matched and tracked over temperature. This matched delay makes the AD8611/AD8612 good choices for clock recovery because the duty cycle of the output matches the duty cycle of the input.

The AD8611 has the same pinout as the LT1016 and LT1394, with lower supply current and a wider common-mode input range, which includes the negative supply rail.

The AD8611/AD8612 are specified over the industrial temperature range (−40°C to +85°C). The AD8611 is available in both 8-lead MSOP and narrow 8-lead SOIC surface-mount packages. The AD8612 is available in a 14-lead TSSOP surface-mount package.

Rev. B

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8/2006—Rev. 0 to Rev. A

Updated Format ... Universal
Added No Latch if V_{CC} < 4.3 V ... Universal
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4/2000—Revision 0: Initial Version

SPECIFICATIONS

$V+ = 5.0$ V, $V- = V_{GND} = 0$ V, $T_A = 25°C$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
		$-40°C \le T_A \le +85°C$			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	$V_{CM} = 0$ V	−6	−4		µA
	I_B	$-40°C \le T_A \le +85°C$	−7	−4.5		µA
Input Offset Current	I_{OS}	$V_{CM} = 0$ V			±4	µA
Input Common-Mode Voltage Range	V_{CM}		0.0		3.0	V
Common-Mode Rejection Ratio	CMRR	$0 \text{ V} \le V_{CM} \le 3.0$ V	55	85		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10$ kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
LATCH ENABLE INPUT						
Logic 1 Voltage Threshold	V_{IH}	$V_{CC} > 4.3$ V	2.0	1.65		V
Logic 0 Voltage Threshold	V_{IL}	$V_{CC} > 4.3$ V		1.60	0.8	V
Logic 1 Current	I_{IH}	$V_{CC} > 4.3$ V, $V_{LH} = 3.0$ V	−1.0	−0.3		µA
Logic 0 Current	I_{IL}	$V_{CC} > 4.3$ V, $V_{LL} = 0.3$ V	−5	−2.7		µA
Latch Enable						
Pulse Width	$t_{PW(E)}$	$V_{CC} > 4.3$ V		3		ns
Setup Time	t_S	$V_{CC} > 4.3$ V		0.5		ns
Hold Time	t_H	$V_{CC} > 4.3$ V		0.5		ns
DIGITAL OUTPUTS						
Logic 1 Voltage	V_{OH}	$I_{OH} = 50$ µA, $\Delta V_{IN} > 250$ mV	3.0	3.35		V
Logic 1 Voltage	V_{OH}	$I_{OH} = 3.2$ mA, $\Delta V_{IN} > 250$ mV	2.4	3.4		V
Logic 0 Voltage	V_{OL}	$I_{OL} = 3.2$ mA, $\Delta V_{IN} > 250$ mV		0.25	0.4	V
DYNAMIC PERFORMANCE						
Input Frequency	f_{MAX}	400 mV p-p sine wave		100		MHz
Propagation Delay	t_P	200 mV step with 100 mV overdrive[1]		4.0	5.5	ns
		$-40°C \le T_A \le +85°C$		5		ns
Propagation Delay	t_P	100 mV step with 5 mV overdrive		5		ns
Differential Propagation Delay (Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV step with 100 mV overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		2.5		ns
Fall Time		80% to 20%		1.1		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$4.5 \text{ V} \le V+ \le 5.5$ V	55	73		dB
V+ Supply Current[2]	I+			5.7	10	mA
		$-40°C \le T_A \le +85°C$			10	
Ground Supply Current[2]	I_{GND}	$V_O = 0$ V, $R_L = \infty$		3.5	7	mA
		$-40°C \le T_A \le +85°C$			7	mA
V− Supply Current[2]	I−			2.2	4	mA
		$-40°C \le T_A \le +85°C$			5	mA

[1] Guaranteed by design.
[2] Per comparator.

V+ = 3.0 V, V− = VGND = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
Input Bias Current	I_B	V_{CM} = 0 V	−6	−4.0		µA
	I_B	−40°C ≤ T_A ≤ +85°C	−7	−4.5		µA
Input Common-Mode Voltage Range	V_{CM}		0		1.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.0 V	55			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = −3.2 mA, V_{IN} > 250 mV	1.2[1]			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA, V_{IN} > 250 mV			0.3	V
LATCH ENABLE INPUT		Not functional if V_{CC} < 4.3 V				
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	2.7 V ≤ V+ ≤ 6 V		46		dB
Supply Currents		V_O = 0 V, R_L = ∞				
V+ Supply Current[2]	I+	−40°C ≤ T_A ≤ +85°C		4.5	6.5	mA
					10	mA
Ground Supply Current[2]	I_{GND}	−40°C ≤ T_A ≤ +85°C		2.5	3.5	mA
					5.5	mA
V− Supply Current[2]	I−			2	3.5	mA
		−40°C ≤ T_A ≤ +85°C			4.8	mA
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	100 mV step with 20 mV overdrive[3]		4.5	6.5	ns

[1] Output high voltage without pull-up resistor. It can be useful to have a pull-up resistor to V+ for 3 V operation.
[2] Per comparator.
[3] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Total Analog Supply Voltage	7.0 V
Digital Supply Voltage	7.0 V
Input Voltage	VCC +0.3 V to VEE −0.3 V
Differential Input Voltage	±5 V
Output Short-Circuit Duration to GND	Indefinite
Input Current	±5 mA
Storage Temperature Range	
R, RU, RM Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	
R, RU, RM Packages	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC (R)	158	43	°C/W
8-Lead MSOP (RM)	240	43	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, a device in socket for P-DIP and a device soldered in circuit board for SOIC and TSSOP.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

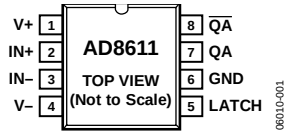


Figure 4. 8-Lead Narrow Body SOIC Pin Configuration

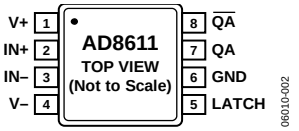


Figure 5. 8-Lead MSOP Pin Configuration

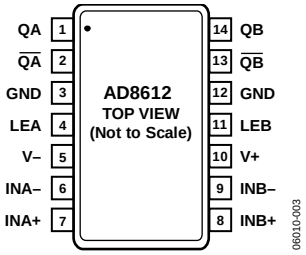


Figure 6. 14-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
SOIC and MSOP	**TSSOP**	**Mnemonic**	**Description**
1	10	V+	Positive Supply Terminal.
2		IN+	Noninverting Analog Input of the Differential Input Stage.
3		IN–	Inverting Analog Input of the Differential Input Stage.
4	5	V–	Negative Supply Terminal.
5		LATCH	Latch Enable Input.
6	3, 12	GND	Negative Logic Supply
7	1	QA	One of Two Complementary Output for Channel A.
8	2	$\overline{QA}$	One of Two Complementary Output for Channel A.
	14	QB	One of Two Complementary Output for Channel B.
	13	$\overline{QB}$	One of Two Complementary Output for Channel B.
	4	LEA	Channel A Latch Enable.
	11	LEB	Channel B Latch Enable.
	7	INA+	Noninverting Analog Input of the Differential Input Stage for Channel A.
	6	INA–	Inverting Analog Input of the Differential Input Stage for Channel A.
	8	INB+	Noninverting Analog Input of the Differential Input Stage for Channel B.
	9	INB–	Inverting Analog Input of the Differential Input Stage for Channel B.

TYPICAL PERFORMANCE CHARACTERISTICS

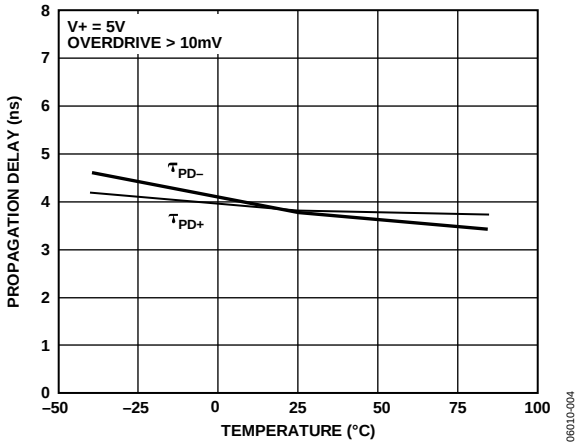


Figure 7. Propagation Delay vs. Temperature

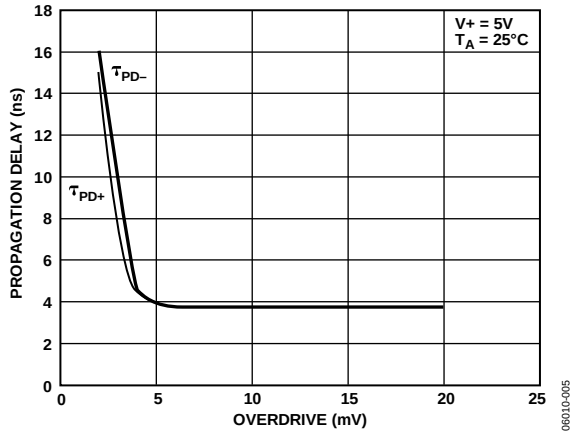


Figure 8. Propagation Delay vs. Overdrive

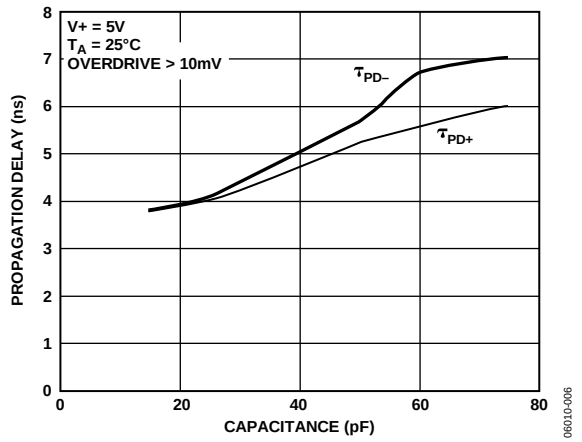


Figure 9. Propagation Delay vs. Load Capacitance

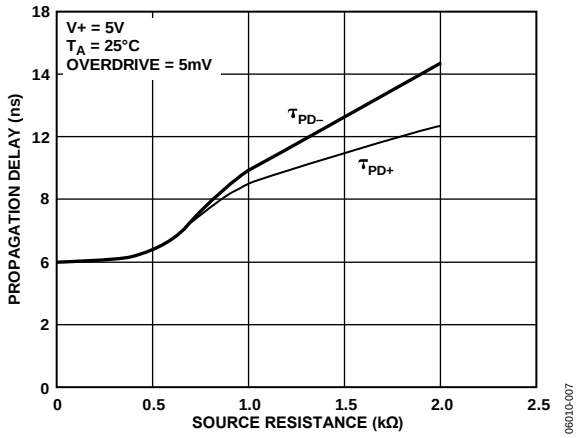


Figure 10. Propagation Delay vs. Source Resistance

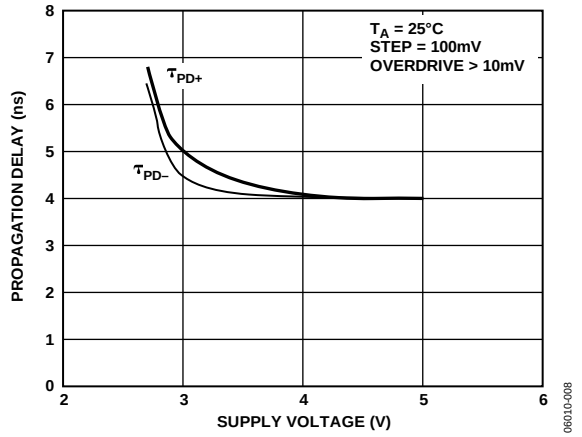


Figure 11. Propagation Delay vs. Supply Voltage

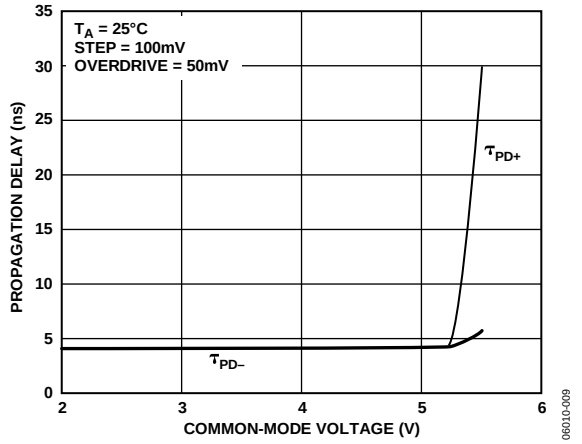


Figure 12. Propagation Delay vs. Common-Mode Voltage

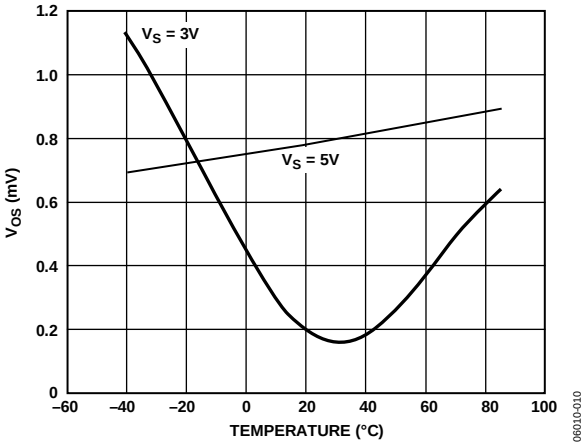


Figure 13. Offset Voltage vs. Temperature

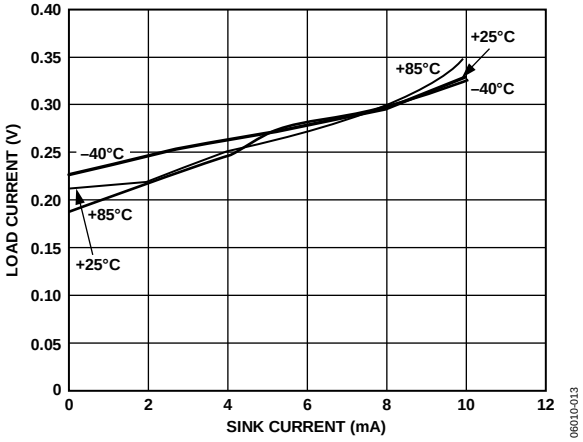


Figure 16. Output Low Voltage vs. Load Current (Sinking) Over Temperature

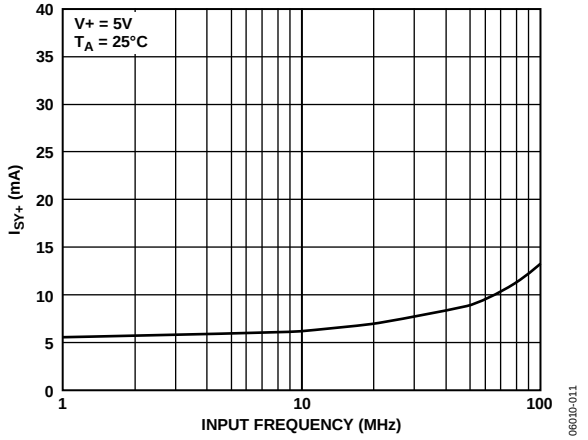


Figure 14. Supply Current vs. Input Frequency

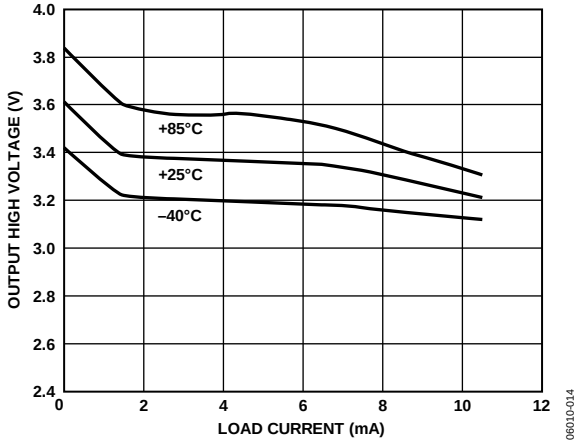


Figure 17. Output High Voltage vs. Load Current (Sourcing) Over Temperature

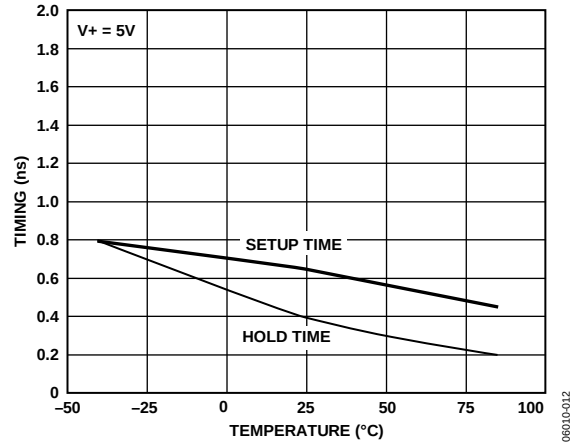


Figure 15. Latch Setup and Hold Time vs. Temperature

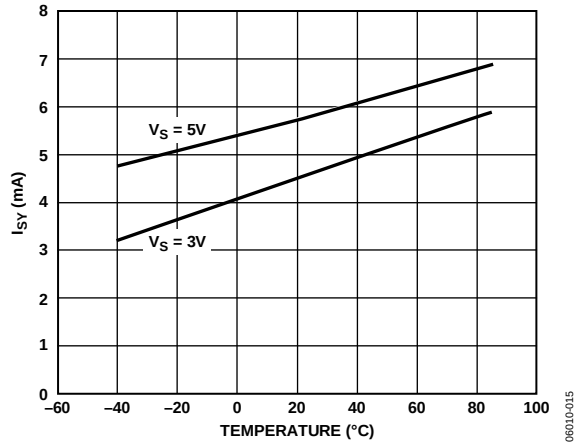


Figure 18. Supply Current vs. Temperature

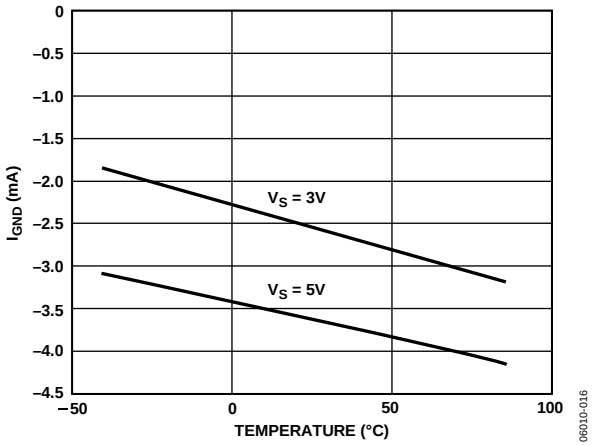


Figure 19. I_{GND} vs. Temperature

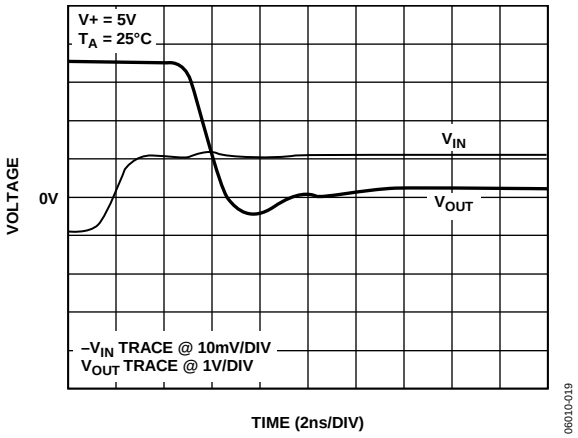


Figure 22. Falling Edge Response

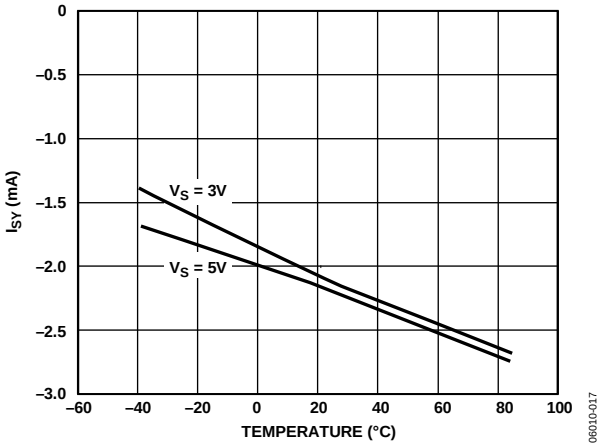


Figure 20. I_{SY-} vs. Temperature

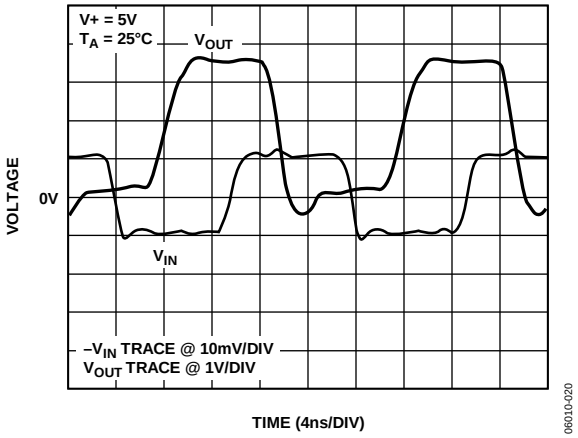


Figure 23. Response to a 50 MHz, 100 mV Input Sine Wave

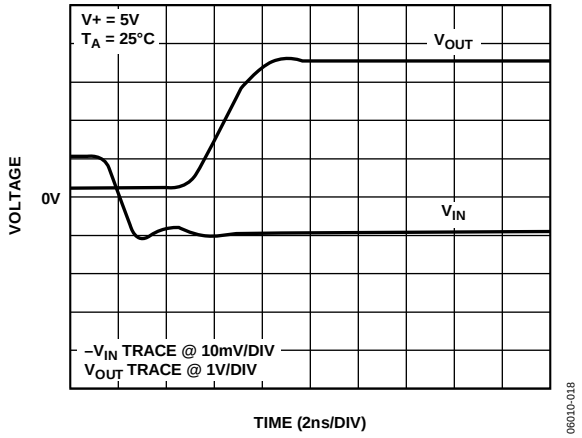


Figure 21. Rising Edge Response

APPLICATIONS INFORMATION

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator or amplifier, proper design and layout of the AD8611/AD8612 must ensure optimal performance. Excess stray capacitance or improper grounding can limit the maximum performance of high speed circuitry.

Minimizing resistance from the source to the comparator input is necessary to minimize the propagation delay of the circuit. Source resistance in combination with the equivalent input capacitance of the AD8611/AD8612 creates an R-C filter that could cause a lagged voltage rise at the input to the comparator. The input capacitance of the AD8611/AD8612 in combination with stray capacitance from an input pin to ground results in several picofarads of equivalent capacitance. Using a surface-mount package and a minimum of input trace length, this capacitance is typically around 3 pF to 5 pF. A combination of 3 kΩ source resistance and 3 pF of input capacitance yields a time constant of 9 ns, which is slower than the 4 ns propagation delay of the AD8611/AD8612. Source impedances must be less than 1 kΩ for best performance.

Another important consideration is the proper use of power-supply-bypass capacitors around the comparator. A 1 μF bypass capacitor must be placed within 0.5 inches of the device between each power supply pin and ground. Another 10 nF ceramic capacitor must be placed as close as possible to the device in parallel with the 1 μF bypass capacitor. The 1 μF capacitor reduces any potential voltage ripples from the power supply, and the 10 nF capacitor acts as a charge reservoir for the comparator during high frequency switching.

A continuous ground plane on the PC board is also recommended to maximize circuit performance. A ground plane can be created by using a continuous conductive plane over the surface of the circuit board, only allowing breaks in the plane for necessary traces and vias. The ground plane provides a low inductive current return path for the power supply, thus eliminating any potential differences at various ground points throughout the circuit board caused from ground bounce. A proper ground plane can also minimize the effects of stray capacitance on the circuit board.

UPGRADING THE LT1394 AND LT1016

The AD8611 single comparator is pin-for-pin compatible with the LT1394 and LT1016 and offers an improvement in propagation delay over both comparators. These devices can easily be replaced with the higher performance AD8611; however, there are differences, so it is useful to ensure that the system still operates properly.

The five major differences between the AD8611 and the LT1016 include input voltage range, input bias currents, propagation delay, output voltage swing, and power consumption. Input common-mode voltage is found by taking the average of the two voltages at the inputs to the comparator.

The LT1016 has an input voltage range from 1.25 V above the negative supply to 1.5 V below the positive supply. The AD8611 input voltage range extends down to the negative supply voltage to within 2 V of V+. If the input common-mode voltage is exceeded, input signals must be shifted or attenuated to bring them into range, keeping in mind the note about source resistance in the Optimizing High Speed Performance section.

For example, an AD8611 powered from a 5 V single supply has its noninverting input connected to a 1 V peak-to-peak, high frequency signal centered around 2.3 V and its inverting input connected to a fixed 2.5 V reference voltage. The worst-case input common-mode voltage to the AD8611 is 2.65 V. This is well below the 3.0 V input common-mode voltage range to the comparator. Note that signals much greater than 3.0 V result in increased input currents and can cause the comparator to operate more slowly.

The input bias current to the AD8611 is 7 μA maximum over temperature (−40°C to +85°C). This is identical to the maximum input bias current for the LT1394, and half of the maximum I_B for the LT1016. Input bias currents to the AD8611 and LT1394 flow out from the comparator inputs, as opposed to the LT1016 whose input bias current flows into its inputs. Using low value resistors around the comparator and low impedance sources will minimize any potential voltage shifts due to bias currents.

The AD8611 is able to swing within 200 mV of ground and within 1.5 V of positive supply voltage. This is slightly more output voltage swing than the LT1016. The AD8611 also uses less current than the LT1016—5 mA as compared to 25 mA of typical supply current.

The AD8611 has a typical propagation delay of 4 ns, compared with the LT1394 and LT1016, whose propagation delays are typically 7 ns and 10 ns, respectively.

MAXIMUM INPUT FREQUENCY AND OVERDRIVE

The AD8611 can accurately compare input signals up to 100 MHz with less than 10 mV of overdrive. The level of overdrive required increases with ambient temperature, with up to 50 mV of overdrive recommended for a 100 MHz input signal and an ambient temperature of +85°C.

It is not recommend to use an input signal with a fundamental frequency above 100 MHz because the AD8611 could draw up to 20 mA of supply current and the outputs may not settle to a definite state. The device returns to its specified performance once the fundamental input frequency returns to below 100 MHz.

OUTPUT LOADING CONSIDERATIONS

The AD8611 can deliver up to 10 mA of output current without increasing its propagation delay. The outputs of the device must not be connected to more than 40 TTL input logic gates or drive less than 400 Ω of load resistance.

The AD8611 output has a typical output swing between ground and 1 V below the positive supply voltage. Decreasing the output load resistance to ground lowers the maximum output voltage due to the increase in output current. Table 6 shows the typical output high voltage vs. load resistance to ground.

Table 6. Maximum Output Voltage vs. Resistive Load

Output Load to Ground	$V+ - V_{OUT, HI}$ (typ)
300 Ω	1.5 V
500 Ω	1.3 V
1 kΩ	1.2 V
10 kΩ	1.1 V
>20 kΩ	1.0 V

Connecting a 500 Ω to 2 kΩ pull-up resistor to V+ on the output helps increase the output voltage so that it is closer to the positive rail; in this configuration, however, the output voltage will not reach its maximum until 20 ns to 50 ns after the output voltage switches. This is due to the R-C time constant between the pull-up resistor and the output and load capacitances. The output pull-up resistor cannot improve propagation delay.

The AD8611 is stable with all values of capacitive load; however, loading an output with greater than 30 pF increases the propagation delay of that channel. Capacitive loads greater than 500 pF also create some ringing on the output wave. Table 7 shows propagation delay vs. several values of load capacitance. The loading on one output of the AD8611 does not affect the propagation delay of the other output.

Table 7. Propagation Delay vs. Capacitive Load

C_L (pF)	t_{PD} Rising (ns)	t_{PD} Falling (ns)
<10	3.5	3.5
33	5	5
100	8	7
390	14.5	10
680	26	15

USING THE LATCH TO MAINTAIN A CONSTANT OUTPUT

With the V_{CC} supply at a nominal 5 V, the latch input to the AD8611/AD8612 can retain data at the output of the comparator. When the latch voltage goes high, the output voltage remains in its previous state, independent of changes in the input voltage.

The setup time for the AD8611/AD8612 is 0.5 ns and the hold time is 0.5 ns. Setup time is defined as the minimum amount of time the input voltage must remain in a valid state before the latch is activated for the latch to function properly. Hold time is defined as the amount of time the input must remain constant after the latch voltage goes high for the output to remain latched to its voltage.

The latch input is TTL and CMOS compatible, so a logic high is a minimum of 2.0 V and a logic low is a maximum of 0.8 V. The latch circuitry in the AD8611/AD8612 has no built-in hysteresis.

At or below approximately 4.1 V, the latch pin becomes unresponsive and must normally be tied low for low V_{CC} operation.

INPUT STAGE AND BIAS CURRENTS

The AD8611 and AD8612 each use a bipolar PNP differential input stage. This enables the input common-mode voltage range to extend from within 2.0 V of the positive supply voltage to 200 mV below the negative supply voltage. Therefore, using a single 5 V supply, the input common-mode voltage range is −200 mV to +3.0 V. Input common-mode voltage is the average of the voltages at the two inputs. For proper operation, the input common-mode voltage must be kept within the common-mode voltage range.

The input bias current for the AD8611/AD8612 is 4 μA, which is the amount of current that flows from each input of the comparator. This bias current goes to zero on an input that is high and doubles on an input that is low, which is a characteristic common to any bipolar comparator. Care must be taken in choosing resistances to be connected around the comparator because large resistors could significantly decrease the voltage due to the input bias current.

The input capacitance for the AD8611/AD8612 is typically 3 pF. This is measured by inserting a 5 kΩ source resistance in series with the input and measuring the change in propagation delay.

USING HYSTERESIS

Hysteresis can easily be added to a comparator through the addition of positive feedback. Adding hysteresis to a comparator offers an advantage in noisy environments where it is undesirable for the output to toggle between states when the input signal is close to the switching threshold. Figure 24 shows a simple method for configuring the AD8611 or AD8612 with hysteresis.

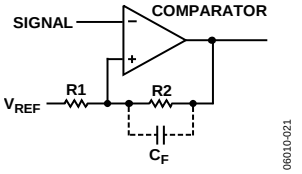


Figure 24. Configuring the AD8611/AD8612 with Hysteresis

In Figure 24, the input signal is connected directly to the inverting input of the comparator. The output is fed back to the noninverting input through R1 and R2. The ratio of R1 to R1 + R2 establishes the width of the hysteresis window, with V_{REF} setting the center of the window, or the average switching voltage. The QA or QB output switches low when the input voltage is greater than V_{HI}, and does not switch high again until the input voltage is less than V_{LO}, as given in Equation 1:

$$V_{HI} = \left(V+ - 1.5\,V_{REF}\right)\frac{R1}{R1+R2} + V_{REF}$$

$$V_{LO} = V_{REF} \times \frac{R2}{R1+R2} \quad (1)$$

where $V+$ is the positive supply voltage.

The capacitor C_F is optional and can be added to introduce a pole into the feedback network. This has the effect of increasing the amount of hysteresis at high frequencies, which is useful when comparing relatively slow signals in high frequency noise environments. At frequencies greater than f_P, the hysteresis window approaches V_{HI} = V+ − 1.5 V and V_{LO} = 0 V. For frequencies less than f_P, the threshold voltages remain as in Equation 1.

CLOCK TIMING RECOVERY

Comparators are often used in digital systems to recover clock timing signals. High speed square waves transmitted over any distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high speed comparator can recover the distorted waveform while maintaining a minimum of delay.

Figure 25 shows V_{OUT} vs. V_{IN} as the AD8611 recovers a 65 MHz, 100 mV peak-to-peak distorted clock signal into a 4 V peak-to-peak square wave. The lower trace is the input to the AD8611, and the upper trace is the QA or QB output from the comparator. The AD8611 is powered from a 5 V single supply.

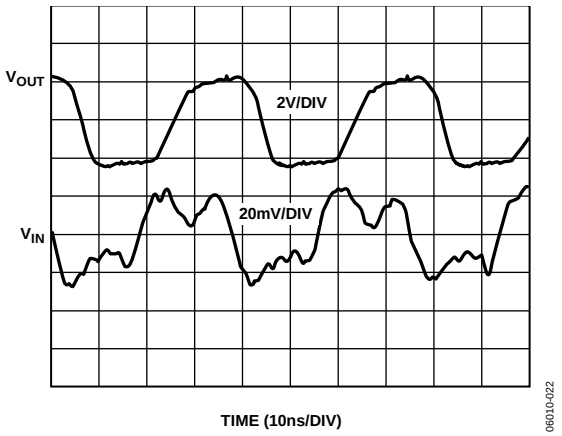


Figure 25. Using the AD8611 to Recover a Noisy Clock Signal

A 5 V, HIGH SPEED WINDOW COMPARATOR

A window comparator circuit detects when a signal is between two fixed voltages. The AD8612 can create a high speed window comparator, as shown in Figure 26. In this example, the reference window voltages are set as:

$$V_{HI} = \frac{R2}{R1 + R2} \qquad V_{LO} = \frac{R4}{R3 + R4}$$

The output of the A1 comparator goes high when the input signal exceeds V_{HI}, and the output of A2 goes high only when V_{IN} drops below V_{LO}. When the input voltage is between V_{HI} and V_{LO}, both comparator outputs are low, turning off both Q1 and Q2, thus driving V_{OUT} to a high state. If the input signal goes outside of the reference voltage window, V_{OUT} goes low.

To ensure a minimum of switching delay, the use of high speed transistors is recommended for Q1 and Q2. Using the AD8612 with 2N3960 transistors provides a total propagation delay from V_{IN} to V_{OUT} of less than 10 ns.

Table 8. Window Comparator Output States

V_{OUT}	Input Voltage
≈ 200 mV	$V_{IN} < V_{LO}$
+5 V	$V_{LO} < V_{IN} < V_{HI}$
≈ 200 mV	$V_{IN} > V_{HI}$

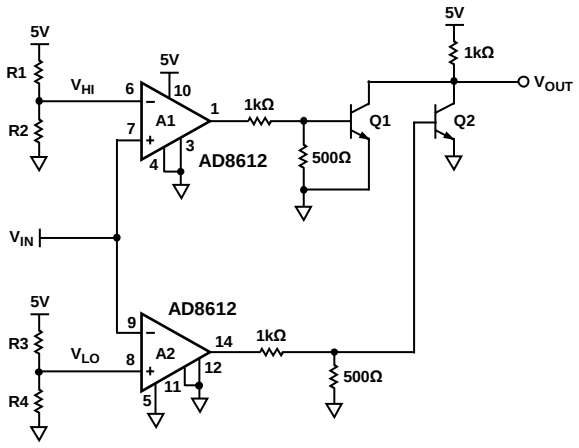


Figure 26. A High Speed Window Comparator

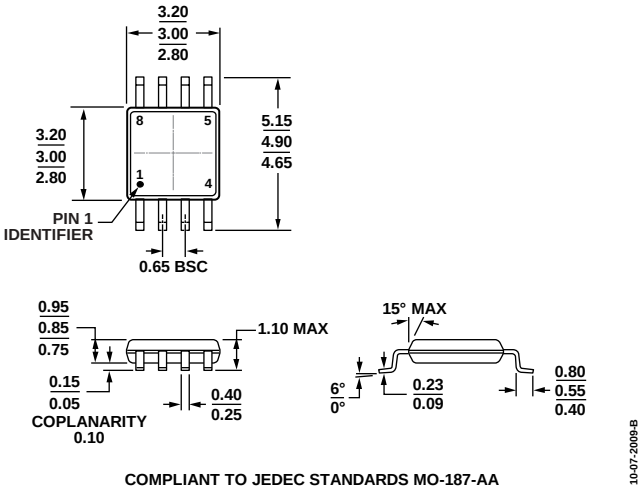
SPICE Model

```
* AD8611 SPICE Macro-Model Typical Values
* 1/2000, Ver. 1.0
* TAM/ADSC
*
* Node assignments
*                non-inverting input
*                |     inverting input
*                |     |      positive supply
*                |     |      |            negative supply
*                |     |      |            |         Latch
*                |     |      |            |         |        DGND
*                |     |      |            |         |        |       Q
*                |     |      |            |         |        |       |     QNOT
*                |     |      |            |         |        |       |     |
.SUBCKT AD8611   1     2      99           50        80       51      45    65
*
* INPUT STAGE
*
*
Q1               4     3      5          PIX
Q2               6     2      5          PIX
IBIAS            99    5      800E-6
RC1              4     50     1E3
RC2              6     50     1E3
CL1              4     6      3E-13
CIN              1     2      3E-12
VCM1             99    7      DC         1.9
D1               5     7      DX
EOS              3     1      POLY(1)    (31,98)   1E-3     1
*
* Reference Voltages
*
EREF             98    0   POLY(2)       (99,0)    (50,0)   0   0.5         0.5
RREF             98    0   100E3
*

* CMRR = 66dB, ZERO AT 1 kHz
```

```
*
ECM1          30       98       POLY(2)   (1,98)    (2,98)   0     0.5       0.5
RCM1          30       31       10E3
RCM2          31       98       5
CCM1          30       31       15.9E-9
*
* Latch Section
*

RX               80     51     100E3
E1               10     98     (4,6)      1
S1               10     11     (80,51)    SLATCH1
R2               11     12     1
C3               12     98     5          4E-12
E2               13     98     (12,98)    1
R3               12     13     500
*
* Power Supply Section
*
GSY1             99     52     POLY(1)    (99,50)   4E-3      -2     6E-4
GSY2             52     50     POLY(1)    (99,50)   3         7E-3   -.6E-3
RSY              52     51     10
*
* Gain Stage Av = 250 fp=100 MHz
*
G2               98     20     (12,98)    0.25
R1               20     98     1000
C1               20     98     10E-13
E3               97     0      (99,0)     1
E4               52     0      (51,0)     1
V1               97     21     DC         0.8
V2               22     52     DC         0.8
D2               20     21     DX
D3               22     20     DX
*
* Q Output
*
Q3               99      41    46         NOX
```

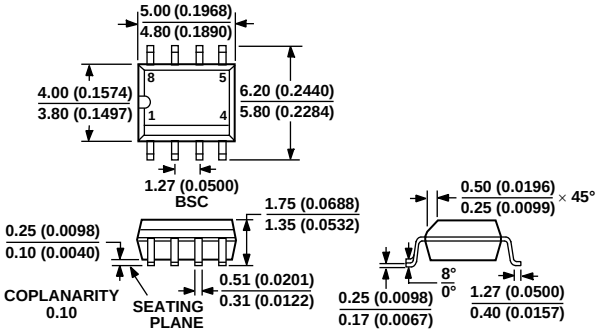
```
Q4              47      42      51          NOX
RB1             43      41      2000
RB2             40      42      2000
CB1             99      41      0.5E-12
CB2             42      51      1E-12
RO1             46      44      1
D4              44      45      DX
RO2             47      45      500
EO1             97      43      (20,51)     1
EO2             40      51      (20,51)     1
*
* Q NOT Output
*
Q5              99      61      66          NOX
Q6              67      62      51          NOX
RB3             63      61      2000
RB4             60      62      2000
CB3             99      61      0           5E-12
CB4             62      51      1E-12
RO3             66      64      1
D5              64      65      DX
RO4             67      65      500
EO3             63      51      (20,51)     1
EO4             97      60      (20,51)     1
*
* MODELS
*
.MODEL PIX PNP(BF=100,IS=1E-16)
.MODEL NOX NPN(BF=100,VAF=130,IS=1E-14)
.MODEL DX D(IS=1E-14)
.MODEL SLATCH1 VSWITCH(ROFF=1E6,RON=500,
+VOFF=2.1,VON=1.4)
.ENDS AD8611
```

OUTLINE DIMENSIONS



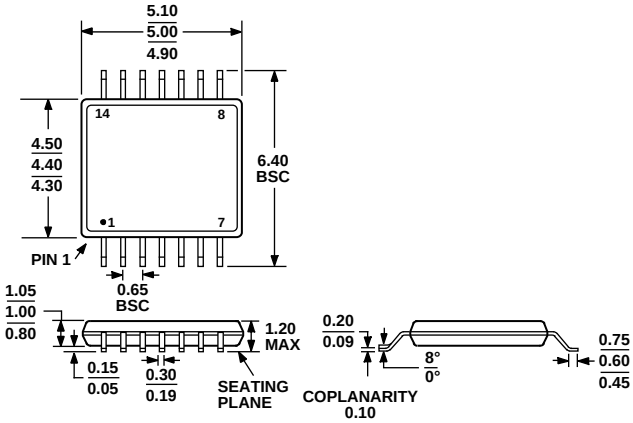
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 27. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 29. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8611ARMZ-REEL	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	G1A
AD8611ARMZ-R2	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	G1A
AD8611AR	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611ARZ	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611ARZ-REEL	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8611ARZ-REEL7	–40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
AD8612ARUZ	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
AD8612ARUZ-REEL	–40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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