Dual Fractional-N/Integer-N Frequency Synthesizer

Data Sheet

ADF4252

FEATURES

- 3.0 GHz fractional-N/1.2 GHz integer-N
- 2.7 V to 3.3 V power supply
- Separate V_P allows extended tuning voltage to 5 V
- Programmable dual modulus prescaler
  - RF: 4/5, 8/9
  - IF: 8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- 3-wire serial interface
- Digital lock detect
- Power-down mode
- Programmable modulus on fractional-N synthesizer
- Trade off noise vs. spurious performance

APPLICATIONS

- Base stations for mobile radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless handsets (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs
- Communications test equipment
- CATV equipment

GENERAL DESCRIPTION

The ADF4252 is a dual fractional-N/integer-N frequency synthesizer that can be used to implement local oscillators (LO) in the upconversion and downconversion sections of wireless receivers and transmitters. Both the RF and IF synthesizers consist of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. The RF synthesizer has a Σ-Δ-based fractional interpolator that allows programmable fractional-N division. The IF synthesizer has programmable integer-N counters. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).

Control of all the on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

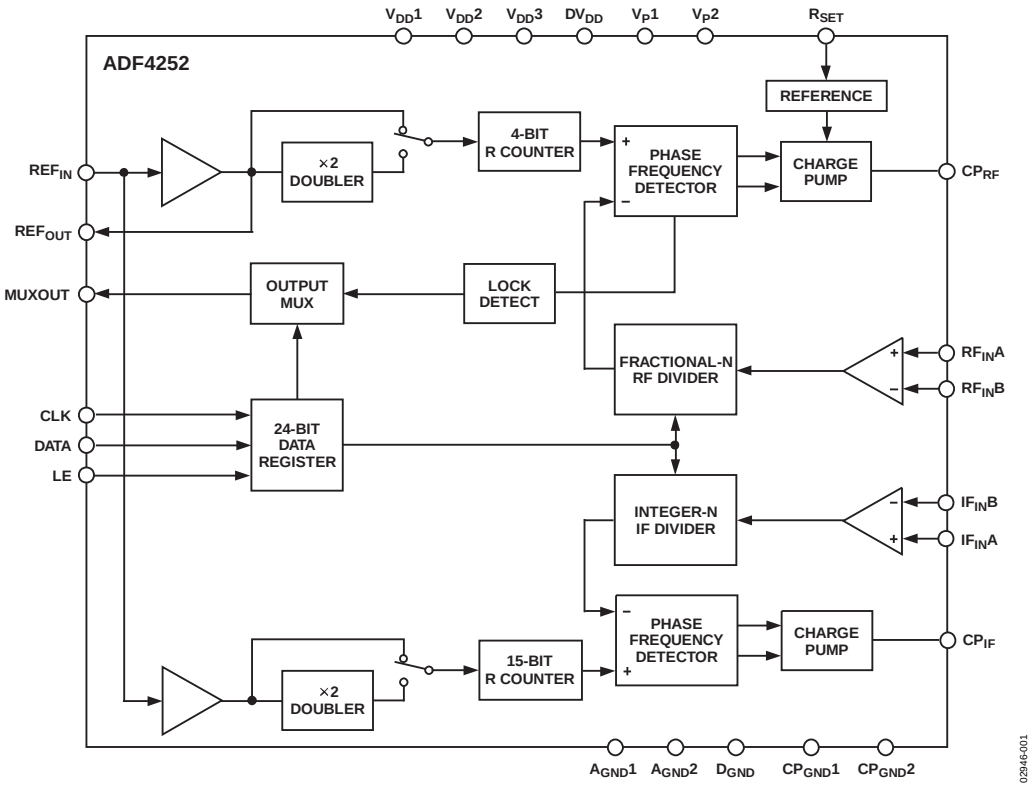

Figure 1.

Rev. E Document Feedback

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SPECIFICATIONS

$V_{DD}1 = V_{DD}2 = V_{DD}3 = DV_{DD} = 3$ V ± 10%, $DV_{DD} < V_P1$, $V_P2 < 5.5$ V, GND = 0 V, $R_{SET} = 2.7$ kΩ, dBm referred to 50 Ω, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
RF Input Frequency ($RF_{IN}A$, $RF_{IN}B$)[2]	0.25		3.0	GHz	
RF Input Sensitivity	−10		0	dBm	
RF Input Frequency ($RF_{IN}A$, $RF_{IN}B$)[2]	0.1		3.0	GHz	Input level = −8 dBm minimum, 0 dBm maximum
RF Phase Detector Frequency			30	MHz	Guaranteed by design
Allowable Prescaler Output Frequency			375	MHz	
IF CHARACTERISTICS					
IF Input Frequency ($IF_{IN}A$, $IF_{IN}B$)[2]	50		1200	MHz	
IF Input Sensitivity	−10		0	dBm	
IF Phase Detector Frequency			55	MHz	Guaranteed by design
Allowable Prescaler Output Frequency			150	MHz	
REFERENCE CHARACTERISTICS					
REF_{IN} Input Frequency			250	MHz	For f < 10 MHz, use dc-coupled square wave (0 V to V_{DD})
REF_{IN} Input Sensitivity	0.5		$V_{DD}1$	V p-p	AC-coupled; when dc-coupled, use 0 V to V_{DD} max (CMOS-compatible)
REF_{IN} Input Current			±100	μA	
REF_{IN} Input Capacitance			10	pF	
CHARGE PUMP					
RF I_{CP} Sink/Source					See Figure 37
High Value		4.375		mA	
Low Value		625		μA	
IF I_{CP} Sink/Source					See Figure 41
High Value		5		mA	
Low Value		625		μA	
I_{CP} Three-State Leakage Current		1		nA	
RF Sink and Source Current Matching		2		%	0.5 V < V_{CP} < V_P − 0.5
R_{SET} Range	1.5	2.7	5.6	kΩ	See Figure 37
IF Sink and Source Current Matching		2		%	
I_{CP} vs. V_{CP}		2		%	0.5 V < V_{CP} < V_P − 0.5
I_{CP} vs. Temperature		2		%	$V_{CP} = V_P/2$
LOGIC INPUTS					
V_{INH}, Input High Voltage	1.35			V	
V_{INL}, Input Low Voltage			0.6	V	
I_{INH}/I_{INL}, Input Current			±1	μA	
C_{IN} Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	V_{DD} − 0.4			V	I_{OH} = 0.2 mA
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 0.2 mA

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES					
$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	2.7		3.3	V	
DV_{DD}	$V_{DD}1$			V	
V_P1, V_P2	$V_{DD}1$		5.5	V	
I_{DD}[3]					
RF + IF		13	16	mA	
RF Only		10	13	mA	
IF Only		4	5.5	mA	
Power-Down Mode		1		μA	
RF NOISE AND SPURIOUS CHARACTERISTICS					
Noise Floor		−141		dBc/Hz	At 20 MHz PFD frequency
In-Band Phase Noise Performance[4]					At VCO output
Lowest Spur Mode		−90		dBc/Hz	R_{FOUT} = 1.8 GHz, PFD = 20 MHz
Low Noise and Spur Mode		−95		dBc/Hz	R_{FOUT} = 1.8 GHz, PFD = 20 MHz
Lowest Noise Mode		−103		dBc/Hz	R_{FOUT} = 1.8 GHz, PFD = 20 MHz
Spurious Signals					See the Typical Performance Characteristics section

[1] Operating temperature range = −40°C to +85°C.
[2] Use a square wave for frequencies less than f_{MIN}.
[3] RF = 1 GHz, RF PFD = 10 MHz, MOD = 4095, IF = 500 MHz, IF PFD = 200 kHz, REF = 10 MHz, V_{DD} = 3 V, V_P1 = 5 V, and V_P2 = 3 V.
[4] The in-band phase noise is measured with the EVAL-ADF4252EB2 evaluation board and the HP5500E phase noise test system. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz at 0 dBm). f_{OUT} = 1.74 GHz, f_{REF} = 20 MHz, N = 87, MOD = 100, Channel Spacing = 200 kHz, V_{DD} = 3.3 V, and V_P = 5 V.

TIMING CHARACTERISTICS

$V_{DD}1 = V_{DD}2 = V_{DD}3 = DV_{DD}$ = 3 V ± 10%, $DV_{DD} < V_P1$, V_P2 < 5.5 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	10	ns min	LE setup time
t_2	10	ns min	DATA to CLOCK setup time
t_3	10	ns min	DATA to CLOCK hold time
t_4	25	ns min	CLOCK high duration
t_5	25	ns min	CLOCK low duration
t_6	10	ns min	CLOCK to LE setup time
t_7	20	ns min	LE pulse width

[1] Guaranteed by design, but not production tested.

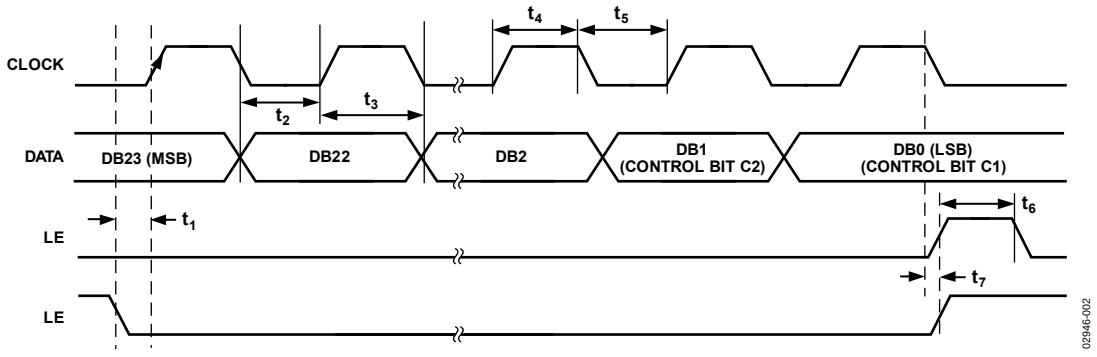

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter[1]	Rating
$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, DV_{DD} to GND[2]	−0.3 V to +4 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
RFINA to RFINB	±600 mV
V_P1, V_P2 to GND	−0.3 V to +5.8 V
V_P1, V_P2 to $V_{DD}1$	−3.3 V to +3.5 V
Digital Input/Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog Input/Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	122°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] This device is a high performance RF integrated circuit with an ESD rating of <2 kΩ, and it is ESD sensitive. Proper precautions must be taken for handling and assembly.

[2] GND is $CP_{GND}1$, $A_{GND}1$, D_{GND}, $A_{GND}2$, and $CP_{GND}2$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

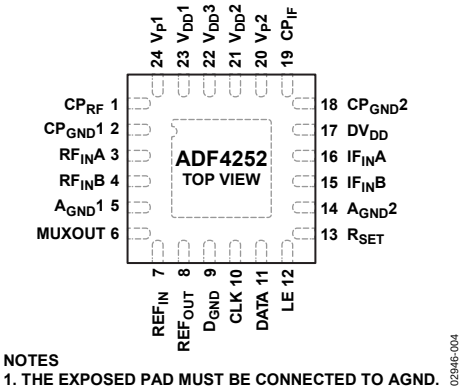

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	CP_{RF}	RF Charge Pump Output. This pin is normally connected to a loop filter that drives the input to an external VCO.
2	$CP_{GND}1$	RF Charge Pump Ground.
3	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is normally taken from the VCO.
4	$RF_{IN}B$	Complementary Input to the RF Prescaler.
5	$A_{GND}1$	Analog Ground for the RF Synthesizer.
6	MUXOUT	This multiplexer output allows either the RF or IF lock detect, the scaled RF or IF, or the scaled reference frequency to be accessed externally.
7	REF_{IN}	Reference Input. This pin is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator.
8	REF_{OUT}	Reference Output.
9	D_{GND}	Digital Ground for the Fractional Interpolator.
10	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
11	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. This input is a high impedance CMOS input.
12	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the seven latches, the latch being selected using the control bits.
13	R_{SET}	Connecting a resistor between this pin and ground sets the minimum charge pump output current. The relationship between I_{CP} and R_{SET} is $I_{CP\_MIN} = 1.6875/R_{SET}$. Therefore, with R_{SET} = 2.7 kΩ, I_{CP_MIN} = 0.625 mA.
14	$A_{GND}2$	Ground for the IF Synthesizer.
15	$IF_{IN}B$	Complementary Input to the IF Prescaler.
16	$IF_{IN}A$	Input to the IF Prescaler. This small signal input is normally taken from the IF VCO.
17	DV_{DD}	Positive Power Supply for the Fractional Interpolator Section. Decoupling capacitors to the ground plane must be placed as close as possible to this pin. DV_{DD} must have the same voltage as $V_{DD}1$, $V_{DD}2$, and $V_{DD}3$.
18	$CP_{GND}2$	IF Charge Pump Ground.
19	CP_{IF}	IF Charge Pump Output. This pin is normally connected to a loop filter that drives the input to an external VCO.
20	V_P2	IF Charge Pump Power Supply. Decoupling capacitors to the ground plane must be placed as close as possible to this pin. This voltage must be greater than or equal to $V_{DD}2$.
21	$V_{DD}2$	Positive Power Supply for the IF Section. Decoupling capacitors to the ground plane must be placed as close as possible to this pin. $V_{DD}2$ has a value 3 V ± 10%. $V_{DD}2$ must have the same voltage as $V_{DD}1$, $V_{DD}3$, and DV_{DD}.
22	$V_{DD}3$	Positive Power Supply for the RF Digital Section. Decoupling capacitors to the ground plane must be placed as close as possible to this pin. $V_{DD}3$ has a value 3 V ± 10%. $V_{DD}3$ must have the same voltage as $V_{DD}1$, $V_{DD}2$, and DV_{DD}.
23	$V_{DD}1$	Positive Power Supply for the RF Analog Section. Decoupling capacitors to the ground plane must be placed as close as possible to this pin. $V_{DD}1$ has a value 3 V ± 10%. $V_{DD}1$ must have the same voltage as $V_{DD}2$, $V_{DD}3$, and DV_{DD}.
24	V_P1	RF Charge Pump Power Supply. Decoupling capacitors to the ground plane must be placed as close as possible to this pin. This voltage must be greater than or equal to $V_{DD}1$.
	EPAD	Exposed Pad. The exposed pad must be connected to A_{GND}.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4 to Figure 15 attained using the EVAL-ADF4252EB1 evaluation board; measurements from HP8562E spectrum analyzer.

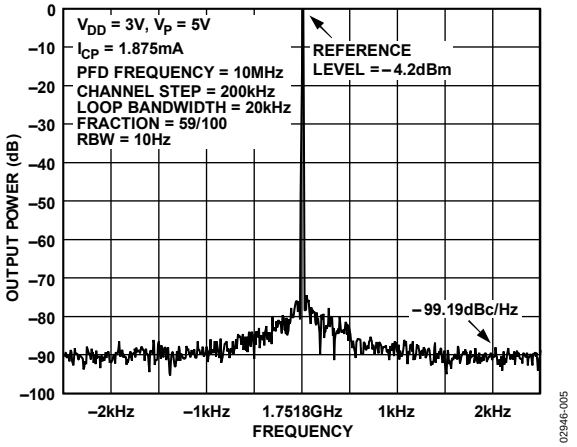

Figure 4. Phase Noise Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution

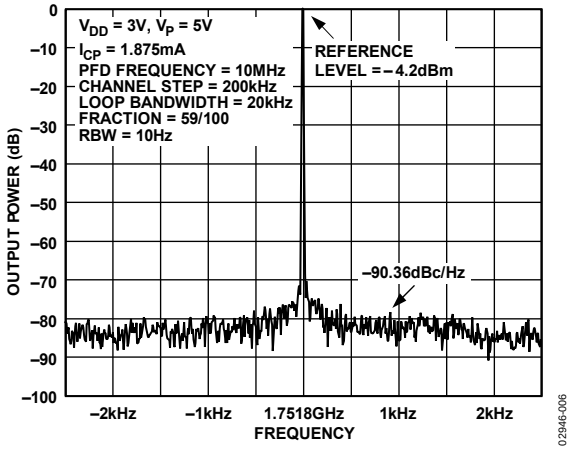

Figure 5. Phase Noise Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution

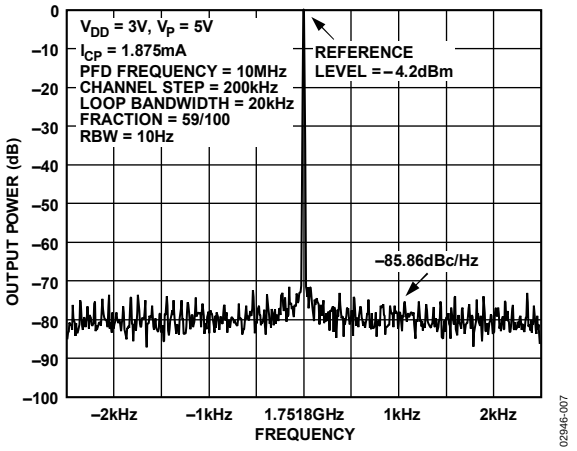

Figure 6. Phase Noise Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution

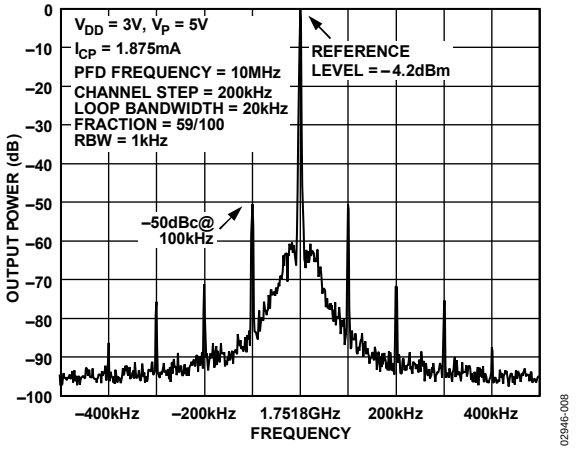

Figure 7. Spurious Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution

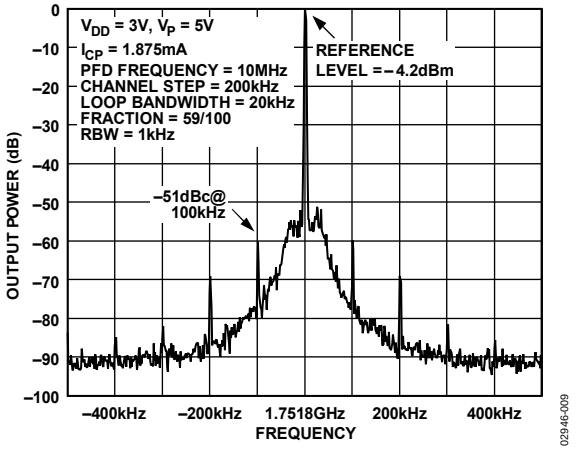

Figure 8. Spurious Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution

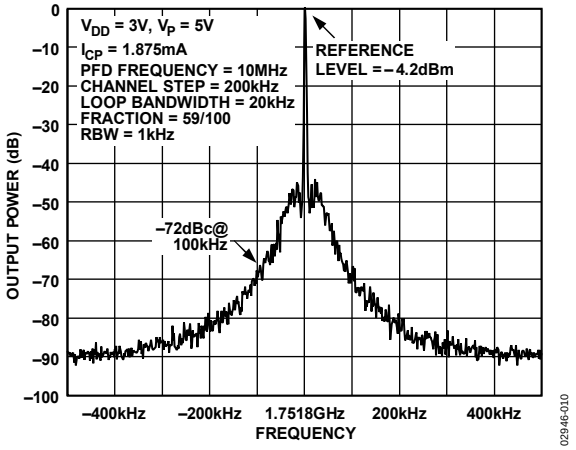

Figure 9. Spurious Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution

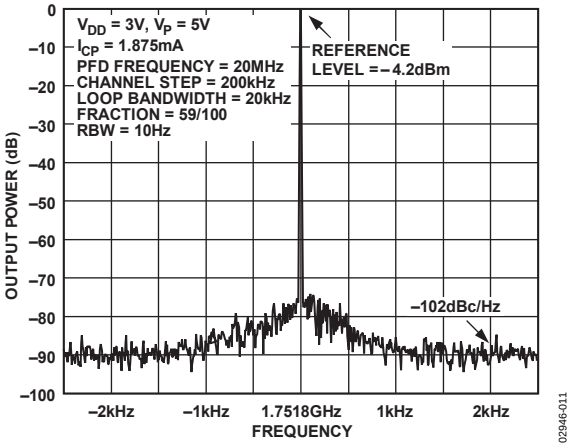

Figure 10. Phase Noise Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution

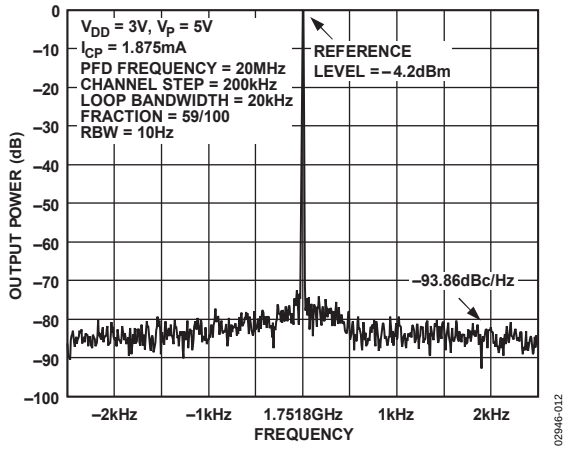

Figure 11. Phase Noise Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution

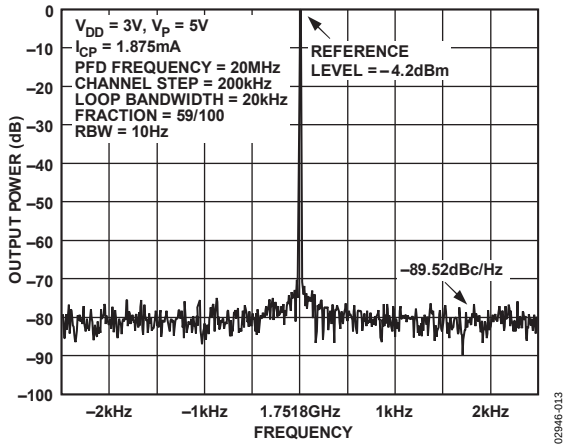

Figure 12. Phase Noise Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution

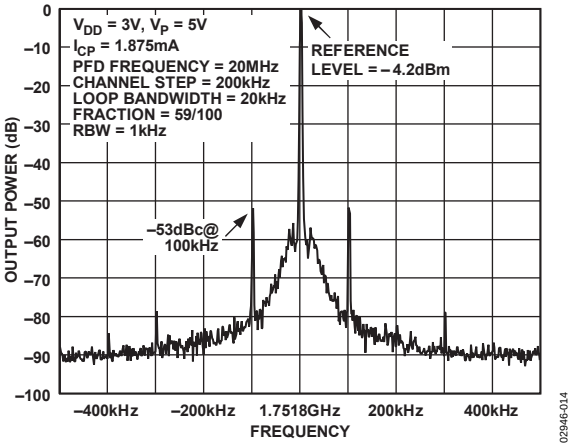

Figure 13. Spurious Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution

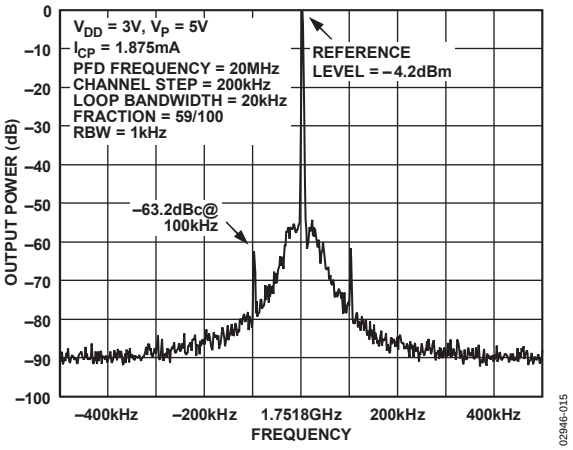

Figure 14. Spurious Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution

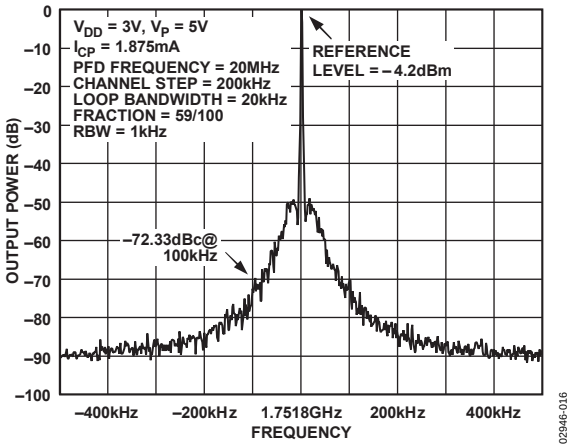

Figure 15. Spurious Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution

For Figure 16 to Figure 21, across all fractional channel steps from f = 0/130 to f = 129/130, RF_{OUT} = 1.45 GHz, INT = 55, REF_{IN} = 26 MHz, and loop bandwidth = 40 kHz. Plots attained using the EVAL-ADF4252EB2 evaluation board.

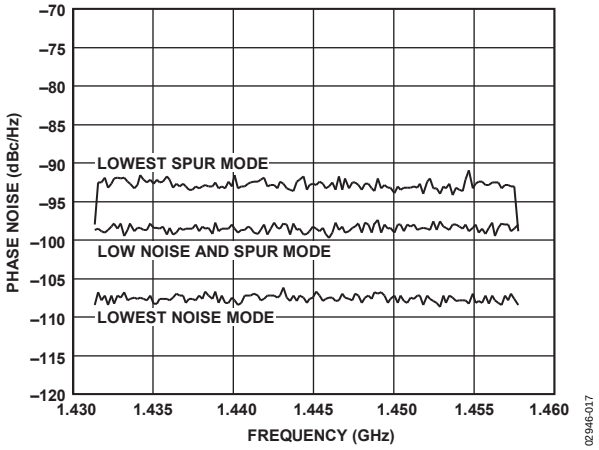

Figure 16. In-Band Phase Noise vs. Frequency

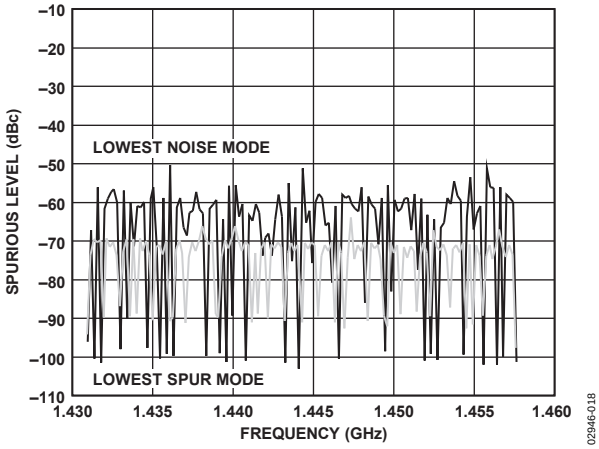

Figure 17. 100 kHz Spur vs. Frequency

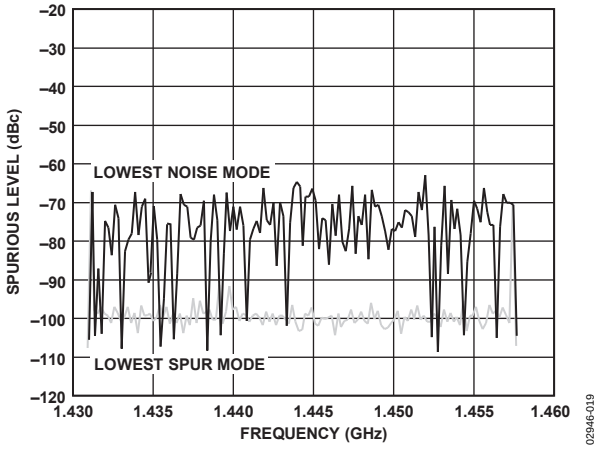

Figure 18. 200 kHz Spur vs. Frequency

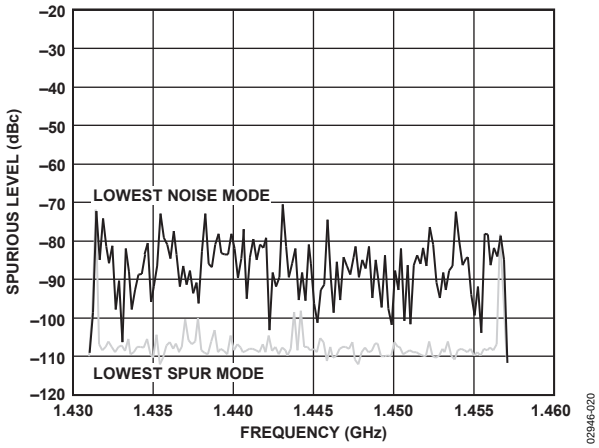

Figure 19. 400 kHz Spur vs. Frequency

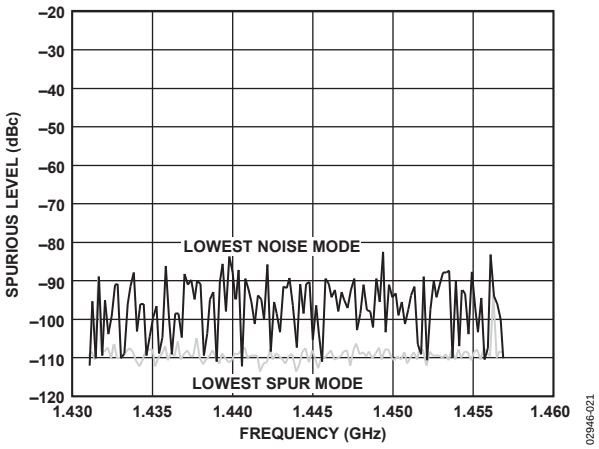

Figure 20. 600 kHz Spur vs. Frequency

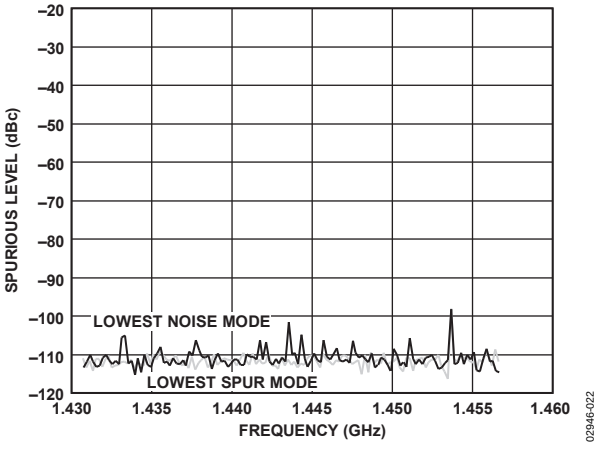

Figure 21. 3 MHz Spur vs. Frequency

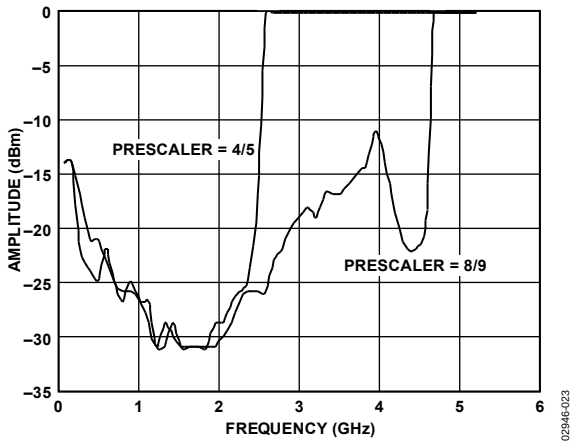

Figure 22. RF Input Sensitivity

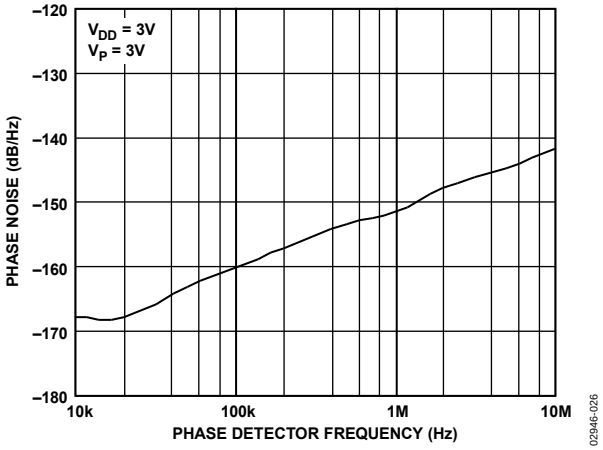

Figure 25. Phase Noise (Referred to CP Output) vs. PFD Frequency, IF Side

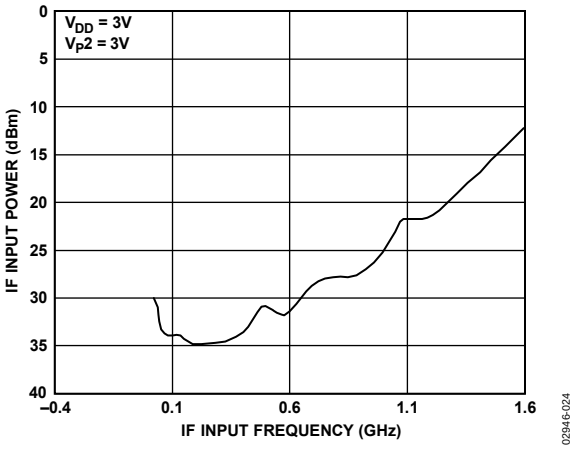

Figure 23. IF Input Sensitivity

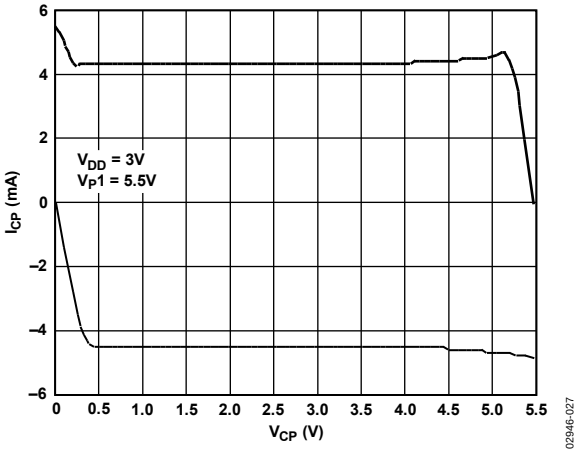

Figure 26. RF Charge Pump Output Characteristics

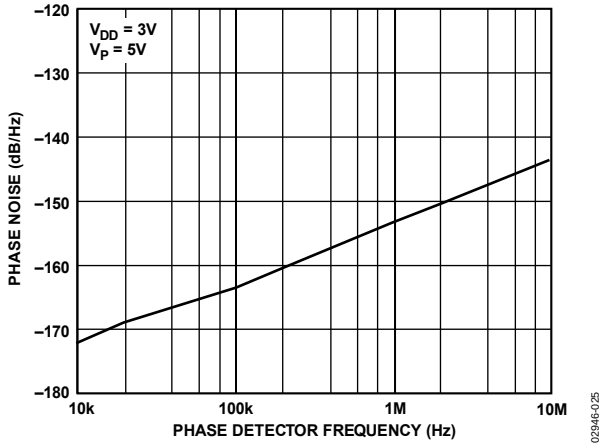

Figure 24. Phase Noise (Referred to CP Output) vs. PFD Frequency, RF Side

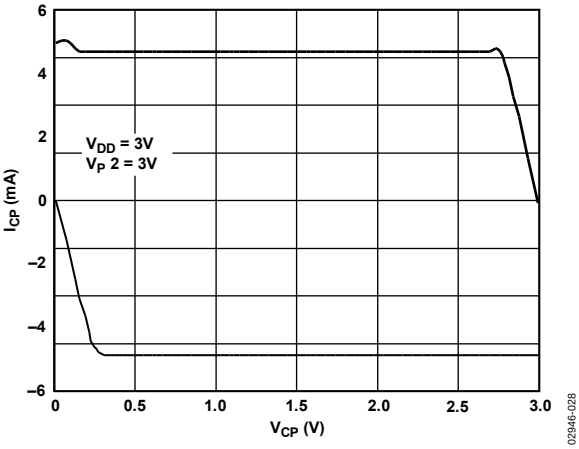

Figure 27. IF Charge Pump Output Characteristics

DETAILED FUNCTIONAL BLOCK DIAGRAM

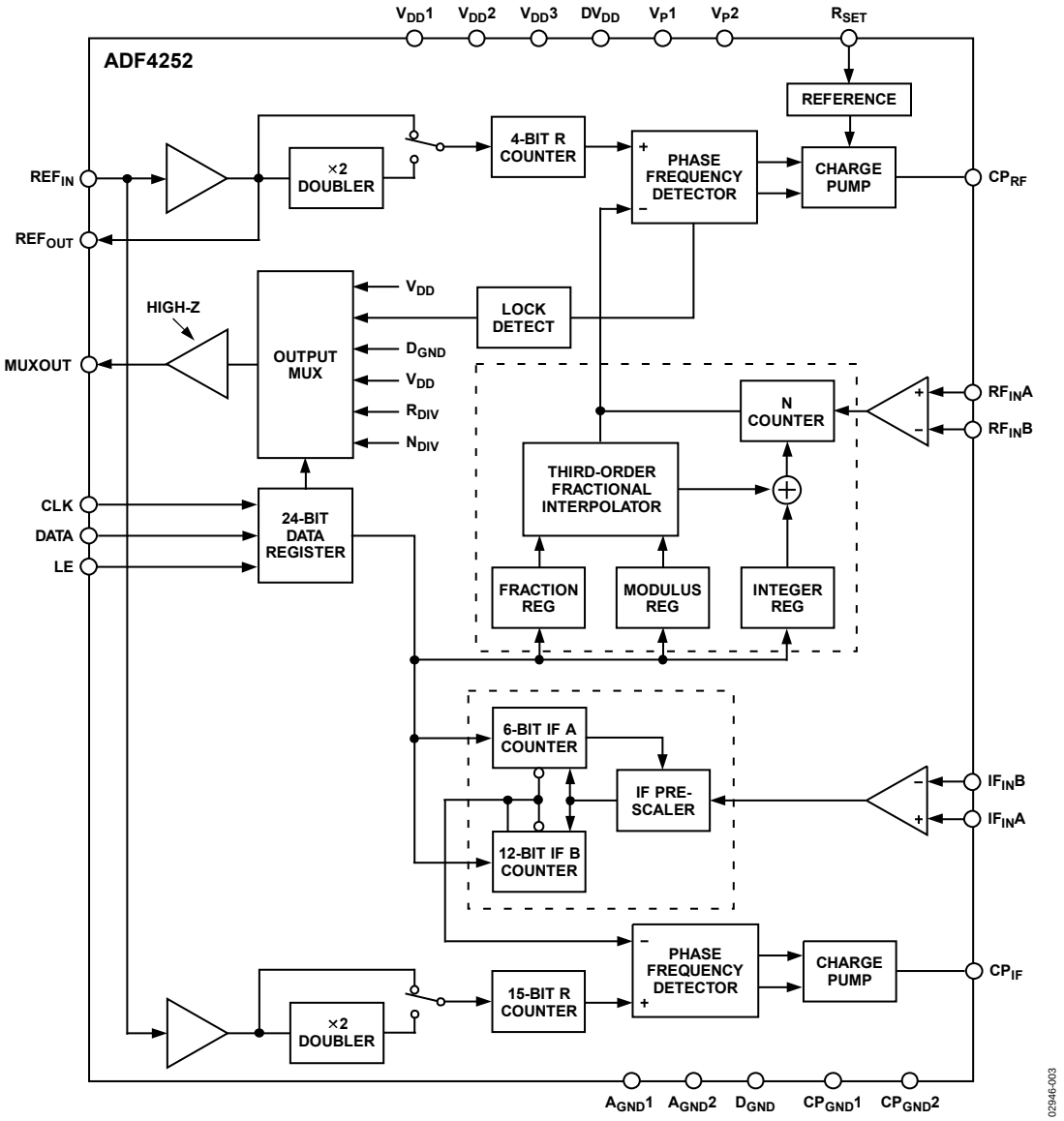

Figure 28. Detailed Functional Block Diagram

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 29. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. This ensures that there is no loading of the REFIN pin on power-down.

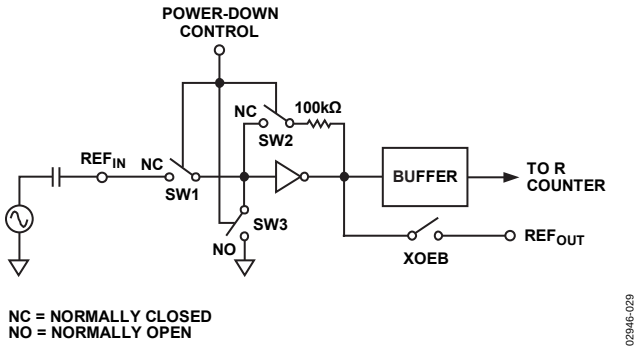

Figure 29. Reference Input Stage

RF AND IF INPUT STAGE

The RF input stage is shown in Figure 30. The IF input stage is the same. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the N counter.

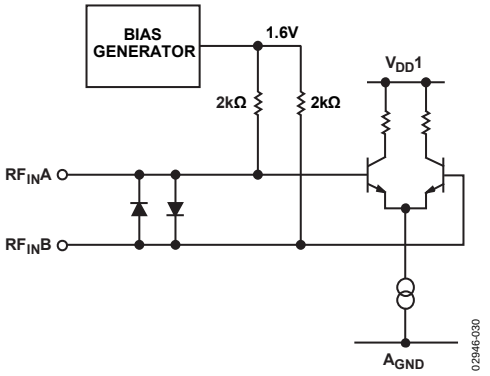

Figure 30. RF Input Stage

RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 31 to 255 are allowed.

INT, FRAC, MOD, AND R RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the RF R counter, make it possible to generate output frequencies that are spaced by fractions of the RF phase frequency detector (PFD). The equation for the RF VCO frequency (RF_{OUT}) is

$$RF_{OUT} = f_{PFD} \times \left(INT + \frac{FRAC}{MOD} \right) \quad (1)$$

where:
RF_{OUT} is the output frequency of external VCO.
f_{PFD} is the PFD frequency (see Equation 2).
INT is the preset divide ratio of the binary 8-bit counter (31 to 255).
FRAC is the preset fractional ratio of the binary 12-bit programmable FRAC counter (0 to MOD).
MOD is the preset modulus ratio of the binary 12-bit programmable FRAC counter (2 to 4095).

$$f_{PFD} = REF_{IN} \times \frac{(1+D)}{R} \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the RF REF_{IN} doubler bit.
R is the preset divide ratio of the binary 4-bit programmable reference counter (1 to 15).

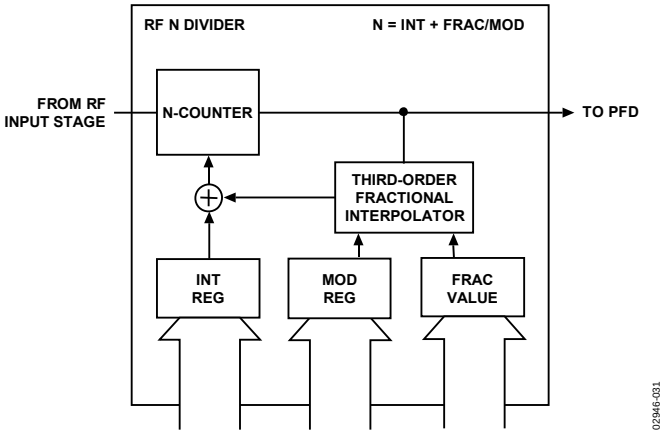

Figure 31. N Counter

RF R COUNTER

The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the RF PFD. Division ratios from 1 to 15 are allowed.

IF R COUNTER

The 15-bit IF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the IF PFD. Division ratios from 1 to 32,767 are allowed.

IF PRESCALER (P/P + 1)

The dual modulus IF prescaler (P/P + 1), along with the IF A and B counters, enables the large division ratio, N, to be realized (N = PB + A). Operating at CML levels, the prescaler takes the clock from the IF input stage and divides it down to a manageable frequency for the CMOS IF A and B counters.

IF A AND B COUNTERS

The IF A and B CMOS counters combine with the dual modulus IF prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are guaranteed to work when the prescaler output is 150 MHz or less.

PULSE SWALLOW FUNCTION

The IF A and B counters, in conjunction with the dual modulus IF prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. See the Device Programming after Initial Power-Up section for examples. The equation for the IF VCO (IF_{OUT}) frequency is

$$IF_{OUT} = [(P \times B) + A] \times f_{PFD} \quad (3)$$

where:

IF_{OUT} is the output frequency of the external VCO.
P is the preset modulus of IF dual modulus prescaler.
B is the preset divide ratio of the binary 12-bit counter (3 to 4095).
A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).
f_{PFD} is obtained using Equation 2.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 32 is a simplified schematic. The antibacklash pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

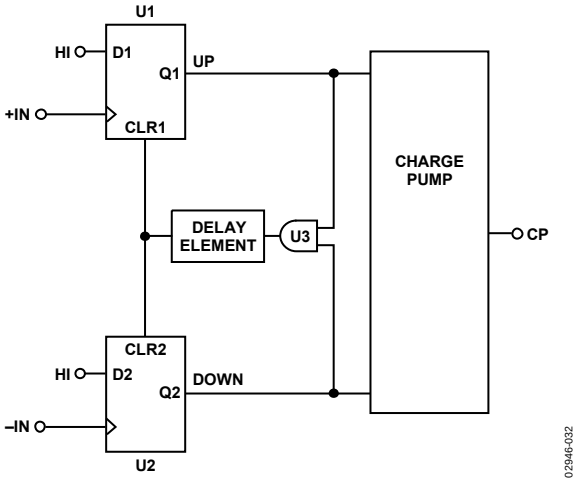

Figure 32. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4252 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M4, M3, M2, and M1 in the master register. Table 5 shows the full truth table. Figure 33 shows the MUXOUT section in block diagram format.

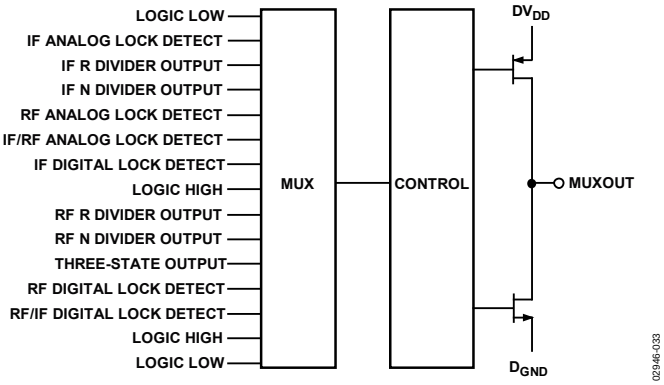

Figure 33. MUXOUT Circuit

LOCK DETECT

MUXOUT can be programmed for two types of lock detect: digital and analog. Digital is active high. The N-channel open-drain analog lock detect must be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow low going pulses.

INPUT SHIFT REGISTER

Data is clocked in on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input register to one of seven latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C2, C1, and C0) in the shift register. These are the three LSBs: DB2, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5. Figure 34 summarizes how the registers are programmed.

Table 5. Control Bit Truth Table

C2	C1	C0	Data Latch
0	0	0	RF N divider register
0	0	1	RF R divider register
0	1	0	RF control register
0	1	1	Master register
1	0	0	IF N divider register
1	0	1	IF R divider register
1	1	0	IF control register

REGISTER MAPS

RF N DIVIDER REGISTER

RESERVED	8-BIT RF INTEGER VALUE (INT)								12-BIT RF FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

RF R DIVIDER REGISTER

PRESCALER	RF REF IN DOUBLER	4-BIT RF R COUNTER				12-BIT INTERPOLATOR MODULUS VALUE (MOD)												CONTROL BITS		
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	P2	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

RF CONTROL REGISTER

NOISE AND SPUR SETTING 3	RESERVED			NOISE AND SPUR SETTING 2	RF CP CURRENT SETTING		RESERVED	RF PD POLARITY	NOISE AND SPUR SETTING 1	RF POWER-DOWN	RF CP THREE-STATE	RF COUNTER RESET	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
N3	T3	T2	T1	N2	CP2	CP1	0	P8	N1	P6	P5	P4	C3 (0)	C2 (1)	C1 (0)

MASTER REGISTER

MUXOUT				XO DISABLE	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M4	M3	M2	M1	P12	P11	P10	P9	C3 (0)	C2 (1)	C1 (1)

IF N DIVIDER REGISTER

IF CP GAIN	IF PRESCALER		12-BIT IF B COUNTER												6-BIT IF A COUNTER						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P15	P14	P13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C3 (1)	C2 (0)	C1 (0)

IF R DIVIDER REGISTER

IF REF IN DOUBLER	15-BIT IF R COUNTER														CONTROL BITS		
DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C3 (1)	C2 (0)	C1 (1)

IF CONTROL REGISTER

RF PHASE RESYNC		RESERVED		RF PHASE RESYNC	IF CP CURRENT SETTING			IF PD POLARITY	IF LDP	IF POWER-DOWN	IF CP THREE-STATE	IF COUNTER RESET	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PR3	PR2	T8	T7	PR1	CP3	CP2	CP1	P21	P20	P19	P18	P17	C3 (1)	C2 (1)	C1 (0)

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Figure 34. Register Summary

RESERVED	8-BIT RF INTEGER VALUE (INT)								12-BIT RF FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

P1	RESERVED
0	RESERVED

F12	F11	F10	.....	F3	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	0	.....	0	0	0	0
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

N8	N7	N6	N5	N4	N3	N2	N1	RF INTEGER VALUE (INT)*
0	0	0	1	1	1	1	1	31
0	0	1	0	0	0	0	0	32
0	0	1	0	0	0	0	1	33
0	0	1	0	0	0	1	0	34
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

*WHEN P = 8/9, N_{MIN} = 91

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Figure 35. RF N Divider Register Map

PRE-SCALER	RF REF_{IN} DOUBLER	4-BIT RF R COUNTER				12-BIT INTERPOLATOR MODULUS VALUE (MOD)												CONTROL BITS		
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	P2	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

P2	RF REF_{IN} DOUBLER
0	DISABLED
1	ENABLED

P3	RF PRESCALER
0	4/5
1	8/9

M12	M11	M10	.....	M3	M2	M1	INTERPOLATOR MODULUS VALUE (MOD) DIVIDE RATIO
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

R4	R3	R2	R1	RF R COUNTER DIVIDE RATIO
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

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Figure 36. RF R Divider Register Map

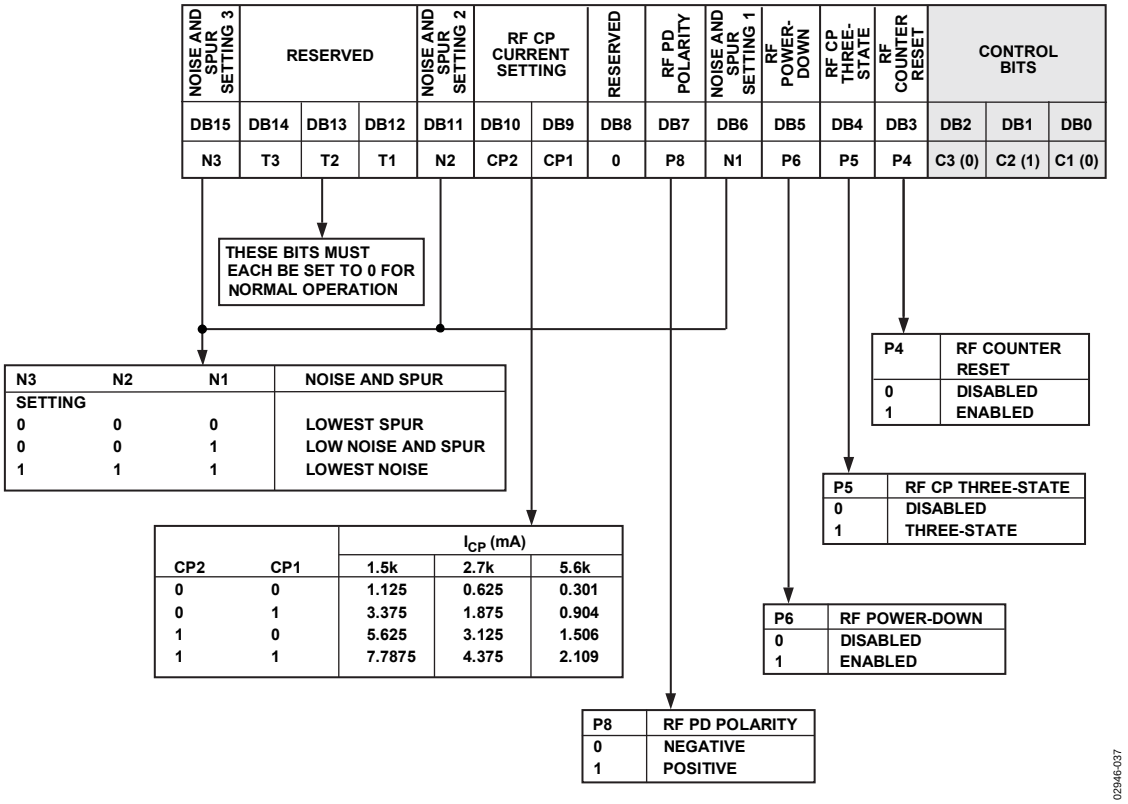

Figure 37. RF Control Register Map

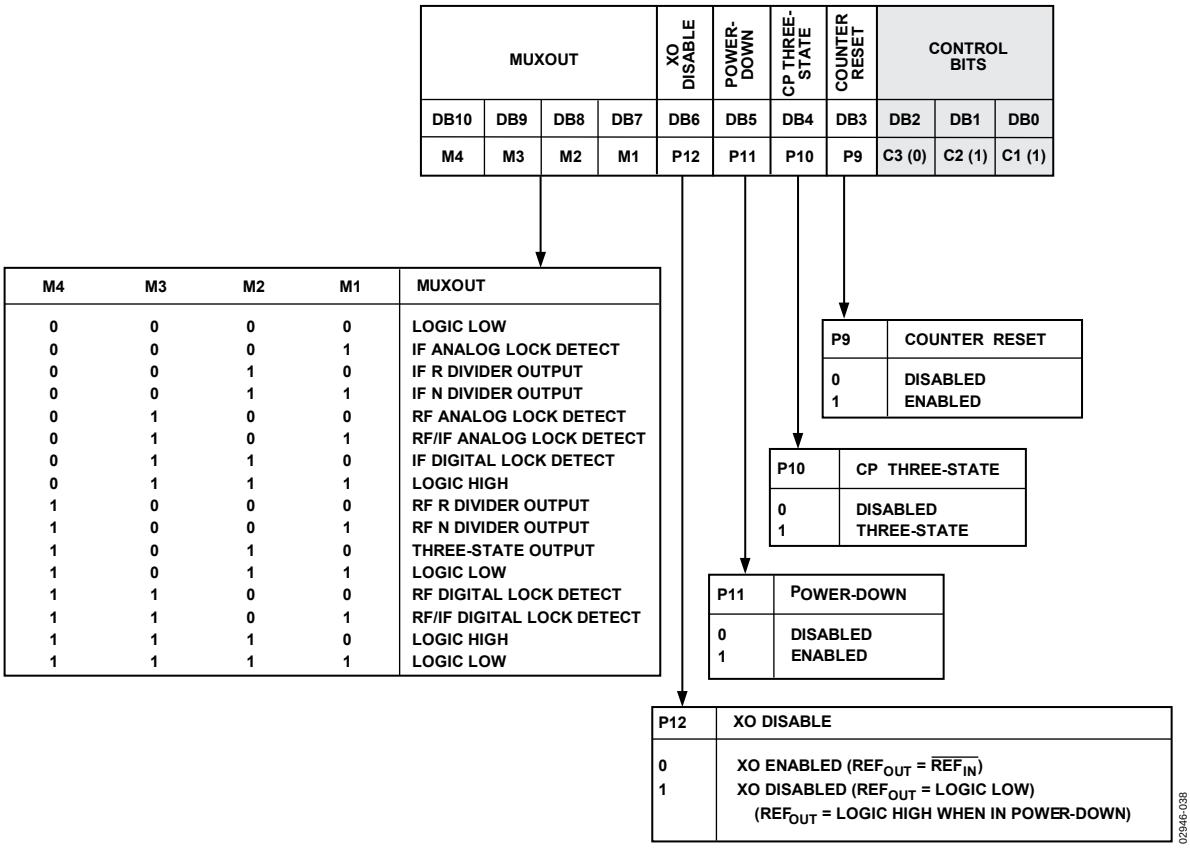

Figure 38. Master Register Map

IF CP GAIN	IF PRESCALER*		12-BIT IF B COUNTER*												6-BIT IF A COUNTER*						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P15	P14	P13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C3 (1)	C2 (0)	C1 (0)

P14	P13	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

P15	IF CP GAIN
0	DISABLED
1	ENABLED

A6	A5	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B12	B11	B10		B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

*N = BP + A, P IS PRESCALER VALUE. B MUST BE GREATER THAN OR EQUAL TO A FOR CONTIGUOUS VALUES OF N, N_{MIN} IS $(P^2 - P)$.

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Figure 39. IF N Divider Register Map

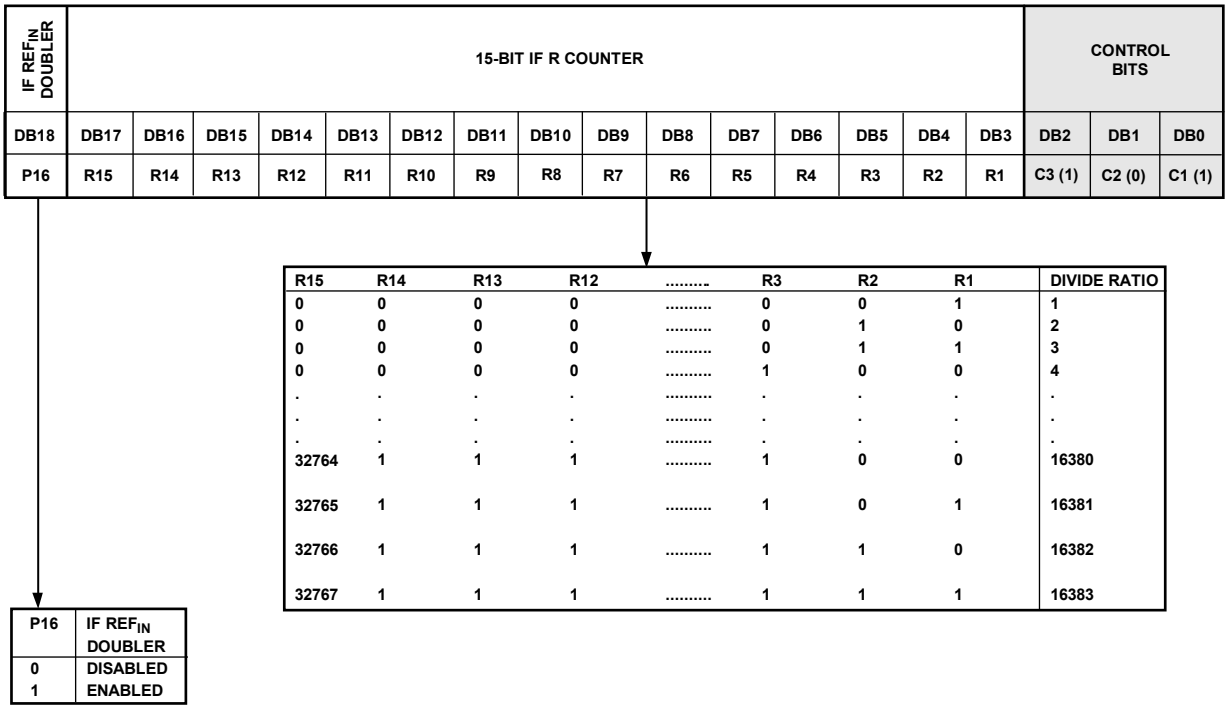


Figure 40. IF R Divider Register Map

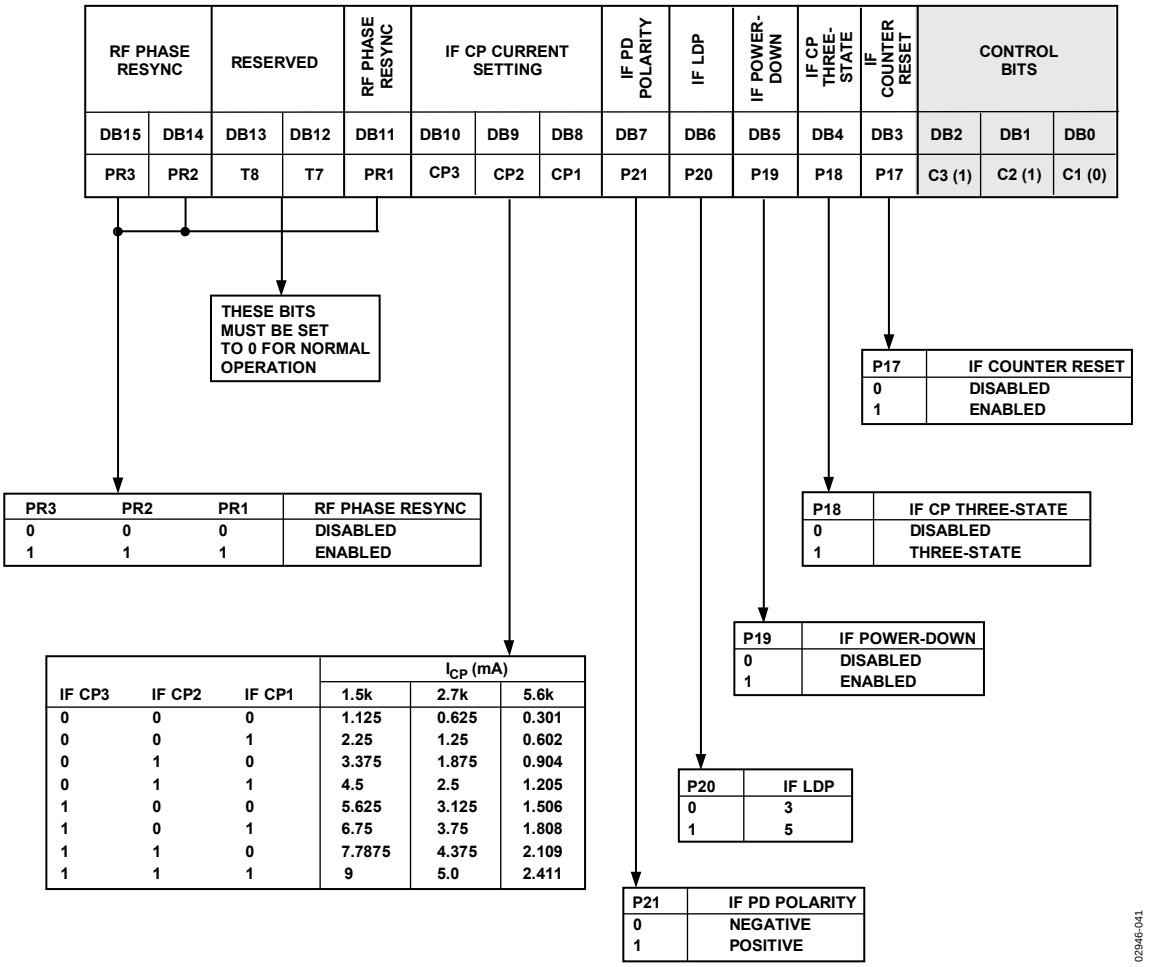


Figure 41. IF Control Register Map

REGISTER DESCRIPTIONS

RF N DIVIDER REGISTER (ADDRESS R0)

With Bits[2:0] of R0 set to 000, the on-chip RF N divider register is programmed. Figure 35 shows the input data format for programming this register.

8-Bit RF INT Value

These eight bits control what is loaded as the INT value. INT is used to determine the overall feedback division factor. It is used in Equation 1.

12-Bit RF FRAC Value

These 12 bits control what is loaded as the FRAC value into the fractional interpolator. FRAC is part of what determines the overall feedback division factor. It is used in Equation 1. The FRAC value must be less than or equal to the value loaded into the MOD register.

RF R DIVIDER REGISTER (ADDRESS R1)

With Bits[2:0] of R1 set to 001, the on-chip RF R divider register is programmed. Figure 36 shows the input data format for programming this register.

RF Prescaler (P/P + 1)

The RF dual-modulus prescaler (P/P +1), along with the INT, FRAC, and MOD counters, determine the overall division ratio from the RF_{IN} to the PFD input. Operating at CML levels, the prescaler takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS counters. The prescaler is based on a synchronous 4/5 core (see Figure 36).

RF REFIN Doubler

Setting this bit to 0 feeds the REF_{IN} signal directly to the 4-bit RF R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 4-bit RF R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional-N synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to REF_{IN} duty cycle in the lowest noise mode and in low noise and spur mode. The phase noise is insensitive to the REF_{IN} duty cycle when the doubler is disabled.

4-Bit RF R Counter

The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 15 are allowed.

12-Bit Interpolator Modulus

This programmable register sets the fractional modulus. The fractional modulus is the ratio of the PFD frequency to the channel step resolution on the RF output.

RF CONTROL REGISTER (ADDRESS R2)

With Bits[2:0] of R2 set to 010, the on-chip RF control register is programmed. Figure 37 shows the input data format for programming this register. Upon initialization, DB15 to DB11 must all be set to 0.

Noise and Spur Setting

The noise and spur setting (Bit 15, Bit 11, and Bit 06 of R2) is a feature that allows the user to optimize his or her design either for improved spurious performance or for improved phase noise performance. When set to 000, the lowest spurs setting is chosen. In this setting, dither is enabled. This randomizes the fractional quantization noise so that it looks more like white noise than spurious noise, which means that the device is optimized for improved spurious performance. This operation is normally used when the PLL closed-loop bandwidth is wide for fast locking applications. A wide-loop filter does not attenuate the spurs to a level that a narrow-loop bandwidth does. When these bits are set to 001, the low noise and spur setting is enabled. In this setting, dither is disabled. This optimizes the synthesizer to operate with improved noise performance. However, the spurious performance is degraded in this mode compared to the lowest spurs setting. To improve noise performance even further, another option is available that reduces the phase noise. This is the lowest noise setting: 111. As well as disabling the dither, it also ensures that the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow-loop filter bandwidth is available. The synthesizer ensures extremely low noise, and the filter attenuates the spurs. The Typical Performance Characteristics section gives the user an idea of the trade-off in a typical WCDMA setup for the different noise and spur settings.

RF Counter Reset

DB3 is the RF counter reset bit for the ADF4252. When this bit is 1, the RF synthesizer counters are held in reset. For normal operation, this bit must be 0.

RF Charge Pump Three-State

This bit puts the charge pump into three-state mode when programmed to a 1. It must be set to 0 for normal operation.

RF Power-Down

DB5 on the ADF4252 provides the programmable power-down mode. Setting this bit to a 1 performs a power-down on both the RF and IF sections. Setting this bit to 0 returns the RF and IF sections to normal operation. While in software power-down, the device retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active RF dc current paths are removed.
2. The RF synthesizer counters are forced to their load state conditions.
3. The RF charge pump is forced into three-state mode.
4. The RF digital lock detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

RF Phase Detector Polarity

DB7 on the ADF4252 sets the RF phase detector polarity. When the VCO characteristics are positive, this bit must be set to 1. When VCO characteristics are negative, this bit must be set to 0.

RF Charge Pump Current Setting

DB9 and DB10 set the RF charge pump current setting. This must be set to whatever charge pump current the loop filter has been designed with (see Figure 37).

RF Test Modes

These bits must be set to 000 for normal operation.

MASTER REGISTER (ADDRESS R3)

With Bits[2:0] of R3 set to 011, the on-chip master register is programmed. Figure 38 shows the input data format for programming the master register.

RF and IF Counter Reset

DB3 is the counter reset bit for the ADF4252. When this bit is 1, both the RF and IF R, INT, and MOD counters are held in reset. For normal operation, this bit must be 0. Upon power-up, the DB3 bit must be disabled, and the INT counter resumes counting in close alignment with the R counter (the maximum error is one prescaler cycle).

Charge Pump Three-State

This bit puts both the RF and IF charge pump into three-state mode when programmed to a 1. It must be set to 0 for normal operation.

Power-Down

Bit 3 of R3 on the ADF4252 provides the programmable power-down mode. Setting this bit to a 1 performs a power-down on both the RF and IF sections. Setting this bit to 0 returns the RF and IF sections to normal operation. While in software power-down, the device retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The RF and IF counters are forced to their load state conditions.
3. The RF and IF charge pumps are forced into three-state mode.
4. The digital lock detect circuitry is reset.
5. The RF_{IN} input and IF_{IN} input are debiased.
6. The oscillator input buffer circuitry is disabled.
7. The input register remains active and capable of loading and latching data.

XO Disable

Setting this bit to 1 disables the REF_{OUT} circuitry. This is set to 1 when using an external TCXO, VCXO, or other reference sources. This is set to 0 when using the REF_{IN} and REF_{OUT} pins to form an oscillator circuit.

MUXOUT Control

The on-chip multiplexer is controlled by Bits[10: 7] of R3 on the ADF4252. Figure 38 shows the truth table.

If the user updates the RF control register or the IF control register, the MUXOUT contents are lost. To retrieve the MUXOUT signal, the user must write to the master register.

Lock Detect

The digital lock detect output goes high if there are 40 successive PFD cycles with an input error of less than 15 ns. It stays high until a new channel is programmed or until the error at the PFD input exceeds 30 ns for one or more cycles. If the loop bandwidth is narrow compared to the PFD frequency, the error at the PFD inputs may drop below 15 ns for 40 cycles around a cycle slip; therefore, the digital lock detect may go falsely high for a short period until the error again exceeds 30 ns. In this case, the digital lock detect is reliable only as a loss of lock indicator.

IF N DIVIDER REGISTER (ADDRESS R4)

With Bits[2:0] of R4 set to 100, the on-chip IF N divider register is programmed. Figure 39 shows the input data format for programming this register.

IF CP Gain

When set to 1, this bit changes the IF charge pump current setting to its maximum value. When the bit is set to 0, the charge pump current reverts back to its previous state.

IF Prescaler

The dual-modulus prescaler (P/P + 1), along with the IF A and IF B counters, determine the overall division ratio, N, to be realized (N = PB + A) from the IF_{IN} to the IF PFD input. Operating at CML levels, the prescaler takes the clock from the IF input stage and divides it down to a manageable frequency for the CMOS counters. It is based on a synchronous 4/5 core. See Equation 2 and Figure 39.

IF B and IF A Counters

The IF A and IF B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency (REFIN) divided by R. The equation for the IF_{OUT} VCO frequency is given in Equation 2.

IF R DIVIDER REGISTER (ADDRESS R5)

With Bits[2:0] of R5 set to 101, the on-chip IF R divider register is programmed. Figure 40 shows the input data format for programming this register.

IF REF_{IN} Doubler

Setting this bit to 0 feeds the REF_{IN} signal directly to the 15-bit IF R counter. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 15-bit IF R counter.

15-Bit IF R Counter

The 15-bit IF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the IF phase frequency detector (PFD). Division ratios from 1 to 32,767 are allowed.

IF CONTROL REGISTER (ADDRESS R6)

With Bits[2:0] of R6 set to 110, the on-chip IF control register is programmed. Figure 41 shows the input data format for programming this register. Upon initialization, DB15 to DB11 must all be set to 0.

IF Counter Reset

DB3 is the IF counter reset bit for the ADF4252. When this bit is 1, the IF synthesizer counters are held in reset. For normal operation, this bit must be 0.

IF Charge Pump Three-State

This bit puts the IF charge pump into three-state mode when programmed to a 1. It must be set to 0 for normal operation.

IF Power-Down

DB5 on the ADF4252 provides the programmable power-down mode. Setting this bit to a 1 performs a power-down on the IF section. Setting this bit to 0 returns the section to normal operation. While in software power-down, the device retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active IF dc current paths are removed.
2. The IF synthesizer counters are forced to their load state conditions.
3. The IF charge pump is forced into three-state mode.
4. The IF digital lock detect circuitry is reset.
5. The IF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

IF Phase Detector Polarity

DB7 in the ADF4252 sets the IF phase detector polarity. When the VCO characteristics are positive, this bit must be set to 1. When VCO characteristics are negative, this bit must be set to 0.

IF Charge Pump Current Setting

DB8, DB9, and DB10 set the IF charge pump current setting. These bits must be set to whatever charge pump current the loop filter has been designed with (see Figure 39).

IF Test Modes

These bits must be set to 00 for normal operation.

RF Phase Resync

Setting the phase resync bits (Bit 15, Bit 14, Bit 11) to 111 enables the phase resync feature. With a fractional modulus of M, a fractional-N PLL can settle with any one of $(2 \times \pi)/M$ valid phase offsets with respect to the reference input. This is different than integer-N (where the RF output always settles to the same static phase offset with respect to the input reference, which is zero ideally) but does not matter in most applications where all that is required is consistent frequency lock.

For applications where a consistent phase relationship between the output and reference is required (that is, digital beamforming), the ADF4252 fractional-N synthesizer can be used with the phase resync feature enabled. This ensures that if the user programs the PLL to jump from Frequency (and Phase) A to Frequency (and Phase) B and back again to Frequency A, the PLL returns to the original phase (Phase A).

When enabled, phase resync activates every time the user programs the R0 or R1 register to set a new output frequency. However, if a cycle slip occurs in the settling transient after the phase re-resync operation, the phase resync is lost. This can be avoided by delaying the resync activation until the locking transient is close to its final frequency. In the IF R divider register, Bits[17:3] of R5 are used to set a time interval from when the new channel is programmed to the time the resync is activated. Although the time interval resolution available from the 15-bit IF R register is one REF_{IN} clock cycle, IF R must be programmed to be a value that is an integer multiple of the programmed MOD value to set a time interval that is at least as long as the lock time of the RF PLL loop.

For example, if REF_{IN} = 26 MHz, MOD = 130 to give 200 kHz output steps (f_{RES}), and the RF loop has a settling time of 150 µs, then IF_R must be programmed to 3900, as follows:

$$26\ \text{MHz} \times 150\ \mu\text{s} = 3900$$

Note that if it is required to use the IF synthesizer with phase resync enabled on the RF synth, the IF synth must operate with a PFD frequency of 26 MHz/3900.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initially applying power to the supply pins, there are three ways to operate the device.

RF AND IF SYNTHESIZERS OPERATIONAL

All registers must be written to when powering up both the RF and IF synthesizer.

RF SYNTHESIZER OPERATIONAL, IF POWER-DOWN

It is necessary to write to the R3, R2, R1, and R0 RF registers when powering up the RF synthesizer only. It is also necessary to write 0x0026 to R6, and to write all zeros to the R5, R4, and R3 IF registers.

IF SYNTHESIZER OPERATIONAL, RF POWER-DOWN

It is necessary to write to the R6, R5, R4, and R3 IF registers when powering up the IF synthesizer only. It is also necessary to write 0x0023 to R3, and to write all zeros to the R2, R1, and R0 RF registers.

RF SYNTHESIZER: AN EXAMPLE

Program the RF synthesizer as follows:

$$RF_{OUT} = \left(INT + \frac{FRAC}{MOD} \right) \times f_{PFD} \quad (4)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC$ is the fractionality.
MOD is the modulus.

$$f_{PFD} = \left(REF_{IN} \times \frac{1+D}{R} \right) \quad (5)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.

For example, in a GSM 1800 system where 1.8 GHz RF frequency output (RF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available and a 200 kHz channel resolution (f_{RES}) is required on the RF output.

$$MOD = \frac{REF_{IN}}{f_{RES}}$$

$$MOD = \frac{13\ \text{MHz}}{200\ \text{kHz}} = 65$$

Therefore, from Equation 5,

$$f_{PFD} = 13\ \text{MHz} \times \frac{1+0}{1} = 13\ \text{MHz}$$

$$1.8\ \text{GHz} = 13\ \text{MHz} \times \left(INT + \frac{FRAC}{65} \right)$$

where $INT = 138$ and $FRAC = 30$.

IF SYNTHESIZER: AN EXAMPLE

The IF synthesizer must be programmed as follows:

$$IF_{OUT} = [(P \times B) + A] \times f_{PFD} \quad (6)$$

where:
IF_{OUT} is the output frequency of the external voltage controlled oscillator (VCO).
P is the IF prescaler.
B is the B counter value.
A is the A counter value.

Equation 5 applies in this example as well.

For example, in a GSM1800 system, where 540 MHz IF frequency output (IF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available and a 200 kHz channel resolution (f_{RES}) is required on the IF output. The prescaler is set to 16/17. The IF REF_{IN} doubler is disabled.

By Equation 5,

$$200\ \text{kHz} = 13\ \text{MHz} \times \frac{1+0}{R}$$

if $R = 65$.

By Equation 6,

$$540\ \text{MHz} = 200\ \text{kHz} \times [(16 \times B) + A]$$

if $B = 168$ and $A = 12$.

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} sets the modulus to 65. This means that the RF output resolution (f_{RES}) is the 200 kHz (13 MHz/65) necessary for GSM.

REFERENCE DOUBLER AND REFERENCE DIVIDER

There is a reference doubler on-chip, which allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually results in an improvement in noise performance of 3 dB. It is important to note that the PFD cannot be operated above 30 MHz due to a limitation in the speed of the Σ-Δ circuit of the N divider.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4252 allows the user to program the modulus over a 12-bit range. This means that the user can set up the device in many different configurations for a specific application, when combined with the reference doubler and the 4-bit R counter.

For example, in an application that requires 1.75 GHz RF and 200 kHz channel step resolution, the system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. This 26 MHz is then fed into the PFD. The modulus is now programmed to divide by 130, which also results in 200 kHz resolution. This offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multistandard applications. If a dual-mode phone requires PDC and GSM1800 standards, the programmable modulus is a huge benefit. PDC requires 25 kHz channel step resolution, whereas GSM1800 requires 200 kHz channel step resolution. A 13 MHz reference signal can be fed directly to the PFD. The modulus is then programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz). The modulus would be reprogrammed to 65 for GSM1800 operation (13 MHz/65 = 200 kHz). It is important that the PFD frequency remains constant (13 MHz). This allows the user to design one loop filter that can be used in both setups without any stability issues. It is the ratio of the RF frequency to the PFD frequency that affects the loop design. Keeping this relationship constant, and instead changing the modulus factor, results in a stable filter.

SPURIOUS OPTIMIZATION AND FASTLOCK

As mentioned in the Noise and Spur Setting section, the device can be optimized for spurious performance. However, in fast locking applications, the loop bandwidth needs to be wide. Therefore, the filter does not provide much attenuation of the spurious outputs. The programmable charge pump can be used to avoid this issue. The filter is designed for a narrow-loop bandwidth so that steady-state spurious specifications are met. This is designed using the lowest charge pump current setting. To implement fast lock during a frequency jump, the charge pump current is set to the maximum setting for the duration of the jump. This has the effect of widening the loop bandwidth, which improves lock time. When the PLL has locked to the new frequency, the charge pump is again programmed to the lowest charge pump current setting. This narrows the loop bandwidth to its original cutoff frequency to allow better attenuation of the spurious outputs than the wide-loop bandwidth.

SPURIOUS SIGNALS—PREDICTING WHERE THEY APPEAR

Just as in integer-N PLLs, spurs appear at PFD frequency offsets on either side of the carrier (and multiples of the PFD frequency). In a fractional-N PLL, spurs also appear at frequencies equal to the RF_{OUT} channel step resolution (f_{RES}). The ADF4252 uses a high-order fractional interpolator engine, which results in spurs also appearing at frequencies equal to half of the channel step resolution. For example, examine the GSM1800 setup with a 26 MHz PFD and 200 kHz resolution. Spurs appear at ±26 MHz from the RF carrier (at an extremely low level due to filtering). Also, there are spurs at ±200 kHz from the RF carrier. Due to the fractional interpolator architecture used in the ADF4252, spurs also appear at ±100 kHz from the RF carrier. Harmonics of all spurs mentioned also appear. With the lowest spur setting enabled, the spurs are attenuated into the noise floor.

PRESCALER

The prescaler limits the INT value. With P = 4/5, N_{MIN} = 31. With P = 8/9, N_{MIN} = 91.

The prescaler can also influence the phase noise performance. If INT < 91, use a prescaler of 4/5. For applications where INT > 91, use P = 8/9 for optimum noise performance.

FILTER DESIGN—ADISIMPLL

A filter design and analysis program is available to help users implement their PLL design. Visit www.analog.com/ADIsimPLL for a free download of the ADIsimPLL™ software. The software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed.

INTERFACING

The ADF4252 has a simple SPI-compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that were clocked into the input register on each rising edge of SCLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the control bit truth table.

The maximum allowable serial clock rate is 20 MHz, which means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 INTERFACE

Figure 42 shows the interface between the ADF4252 and the ADuC812 microconverter. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the input/output port driving LE is brought low. Each latch of the ADF4252 needs (at most) a 24-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input must be brought high to complete the transfer.

The input/output port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

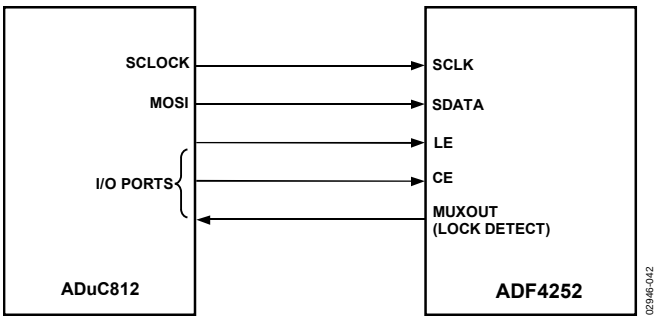


Figure 42. ADuC812 to ADF4252 Interface

ADSP-2181 INTERFACE

Figure 43 shows the interface between the ADF4252 and the ADSP-2181 digital signal processor. Each latch of the ADF4252 needs (at most) a 24-bit word. The easiest way to accomplish this using the ADSP-2181 is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

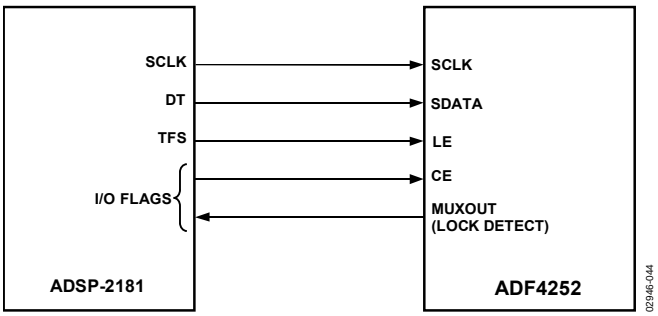


Figure 43. ADSP-2181 to ADF4252 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The leads on the chip scale package (CP-24-10) are rectangular. The printed circuit board pad for these must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land must be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board must be at least as large as this exposed pad. On the printed circuit board, there must be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they must be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz copper to plug the via.

The user must connect the printed circuit board to A_{GND}.

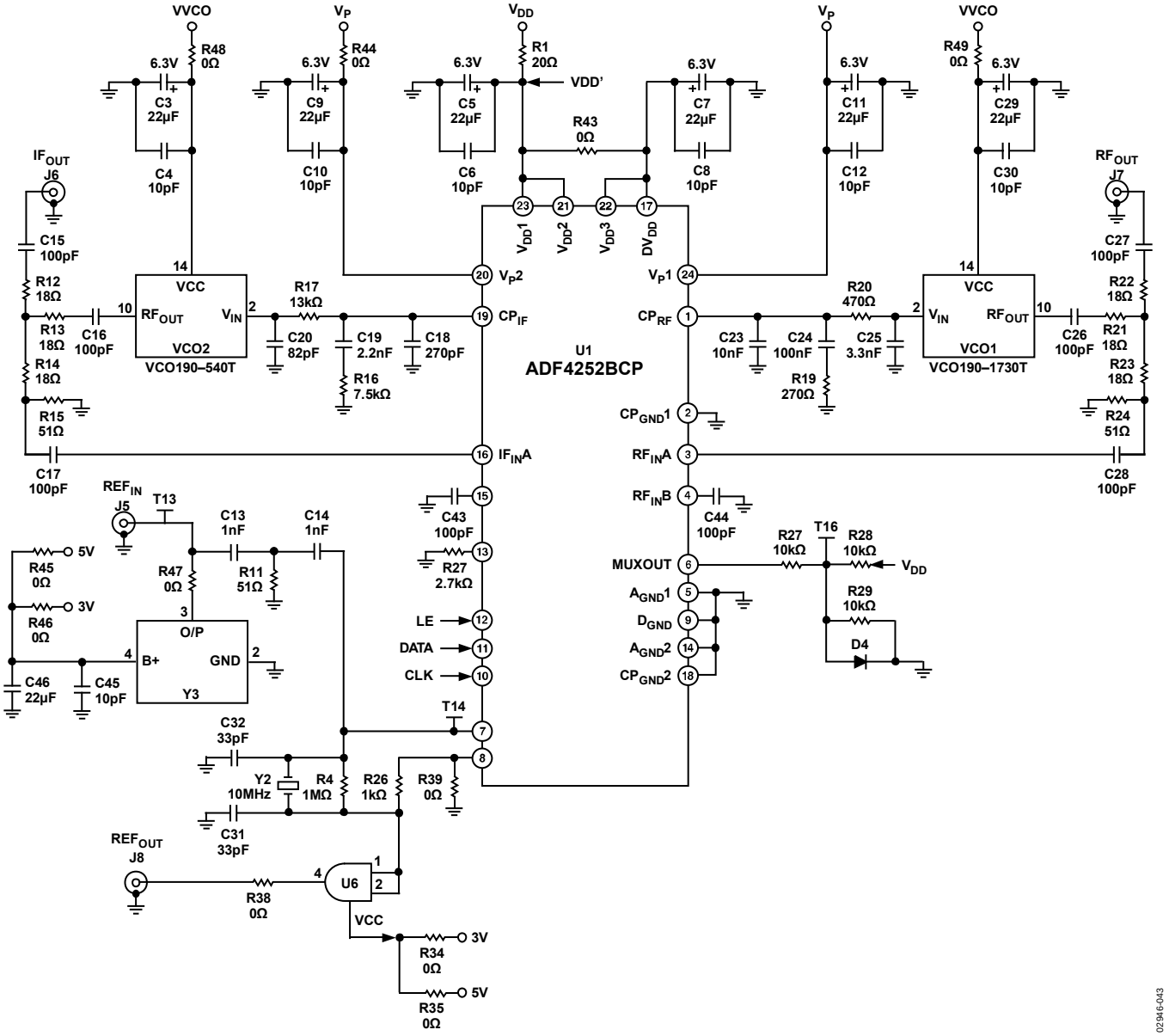
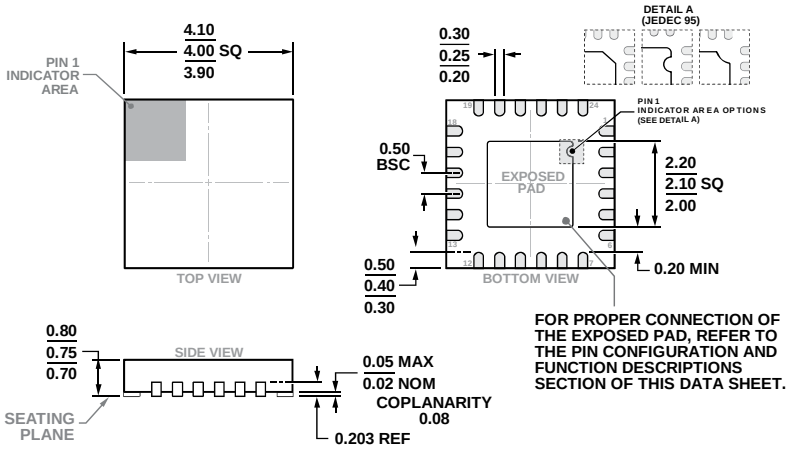


Figure 44. Typical PLL Circuit Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8

Figure 45. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4252BCPZ	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10
ADF4252BCPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10
ADF4252BCPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10
EVAL-ADF4252EBZ2		Evaluation Board	

[1] Z = RoHS Compliant Part.