19-1362; Rev 3; 6/07

Quad, SPST Analog Switch

General Description

The MAX4613 quad analog switch features on-resistance matching (4Ω max) between switches and guarantees on-resistance flatness over the signal range (9Ω max). This low on-resistance switch conducts equally well in either direction. It guarantees low charge injection (10pC max), low power consumption (35µW max), and an electrostatic discharge (ESD) tolerance of 2000V minimum per Method 3015.7. The new design offers lower off-leakage current over temperature (less than 5nA at +85°C).

The MAX4613 quad, single-pole/single-throw (SPST) analog switch has two normally closed switches and two normally open switches. Switching times are less than 250ns for t_{ON} and less than 70ns for t_{OFF}. Operation is from a single +4.5V to +40V supply or bipolar ±4.5V to ±20V supplies.

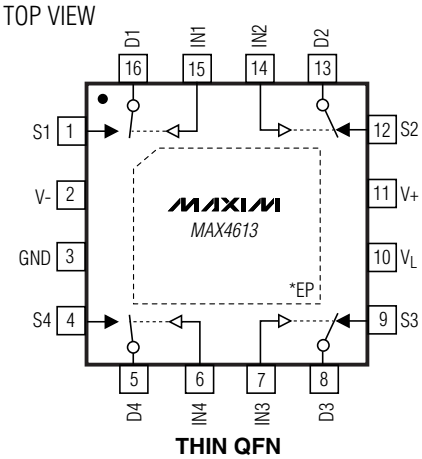
Applications

Sample-and-Hold Circuits	Communication Systems
Test Equipment	Battery-Operated Systems
Heads-Up Displays	PBX, PABX
Guidance and Control Systems	Audio Signal Routing
Military Radios	Modems/Faxes

Features

- **Pin Compatible with Industry-Standard DG213**
- **Guaranteed R_{ON} Match Between Channels (4Ω max)**
- **Guaranteed $R_{FLAT(ON)}$ Over Signal Range (9Ω max)**
- **Guaranteed Charge Injection (10pC max)**
- **Low Off-Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstands 2000V min ESD, per Method 3015.7**
- **Low $R_{DS(ON)}$ (85Ω max)**
- **Single-Supply Operation +4.5V to +40V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Pin Configurations/ Functional Diagrams/Truth Table



THIN QFN

*EP = EXPOSED PAD, CONNECT EP TO V+

Pin Configurations continued at end of data sheet.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4613CPE	0°C to +70°C	16 Plastic DIP
MAX4613CSE	0°C to +70°C	16 Narrow SO
MAX4613CEE	0°C to +70°C	16 QSOP
MAX4613CUE	0°C to +70°C	16 TSSOP**
MAX4613CC/D	0°C to +70°C	Dice*
MAX4613ETE	-40°C to +85°C	16 TQFN-EP*** (5mm x 5mm)
MAX4613EPE	-40°C to +85°C	16 Plastic DIP
MAX4613ESE	-40°C to +85°C	16 Narrow SO
MAX4613EEE	-40°C to +85°C	16 QSOP
MAX4613EUE	-40°C to +85°C	16 TSSOP**

*Contact factory for dice specifications.
**Contact factory for availability.
***EP = Exposed Pad

Quad, SPST Analog Switch

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND
V+ .....+44V
V- .....-44V
V+ to V- .....+44V
V_L .....(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs $V_{S\_}$ $V_{D\_}$ (Note 1) .....(V- - 2V) to (V+ + 2V)
or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S_ or D_
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 8.3mW/°C above +70°C) 667mW
Thin QFN (derate 33.3mW/°C above +70°C) 2667mW
TSSOP (derate 6.7mW/°C above +70°C) 457mW
Operating Temperature Ranges
MAX4613C_ _ .....0°C to +70°C
MAX4613E_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on S_, D_, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		-15		15	V
Drain-Source On-Resistance	$R_{DS(ON)}$	V_D = ±10V, I_S = 1mA	T_A = +25°C		55	70	Ω
			T_A = T_{MIN} to T_{MAX}			85	
On-Resistance Match Between Channels (Note 4)	$\Delta R_{DS(ON)}$	V_D = ±10V, I_S = 1mA	T_A = +25°C			4	Ω
			T_A = T_{MIN} to T_{MAX}			5	
On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V_D = ±5V, I_S = 1mA	T_A = +25°C			9	Ω
			T_A = T_{MIN} to T_{MAX}			15	
Source Leakage Current (Note 5)	$I_{S(OFF)}$	V_D = ±14V, V_S = ∓14V	T_A = +25°C	-0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V_D = ±14V, V_S = ∓14V	T_A = +25°C	-0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$ or $I_{S(ON)}$	V_D = ±14V, V_S = ±14V	T_A = +25°C	-0.50	0.08	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
INPUT							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		-0.5	-0.00001	0.5	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-0.5	-0.00001	0.5	µA
SUPPLY							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	V_S = ±10V, Figure 2	T_A = +25°C		150	250	ns
Turn-Off Time (Note 3)	t_{OFF}	V_S = ±10V, Figure 2	T_A = +25°C		90	120	ns
Break-Before-Make Time Delay (Note 3)	t_D	Figure 3	T_A = +25°C	5	20		ns
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0, R_{GEN} = 0, Figure 4	T_A = +25°C		5	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		60		dB
Crosstalk (Note 7)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		100		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		4		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		4		pF
Source-On Capacitance	$C_{S(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		16		pF
Drain-On Capacitance	$C_{D(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		16		pF

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}			0		12	V
Drain-Source On-Resistance	$R_{DS(ON)}$	V_L = 5V; V_D = 3V, 8V; I_S = 1mA	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range	V+, V-			4.5		40	V
Power-Supply Current	I+	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0 or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	

ELECTRICAL CHARACTERISTICS—Single Supply (continued)

(V+ = 12V, V- = 0, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

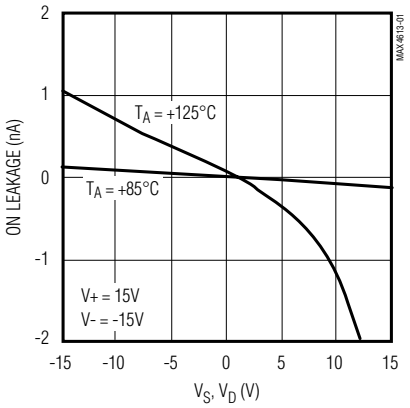
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	V_S = 8V, Figure 2	T_A = +25°C		300	400	ns
Turn-Off Time (Note 3)	t_{OFF}	V_S = 8V, Figure 2	T_A = +25°C		60	200	ns
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0, R_{GEN} = 0, Figure 4	T_A = +25°C		5	10	pC

Note 2: Typical values are for **design aid only,** are not guaranteed and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog signal range.
Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$, and $I_{S(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed at +25°C.
Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S).
Note 7: Between any two switches.

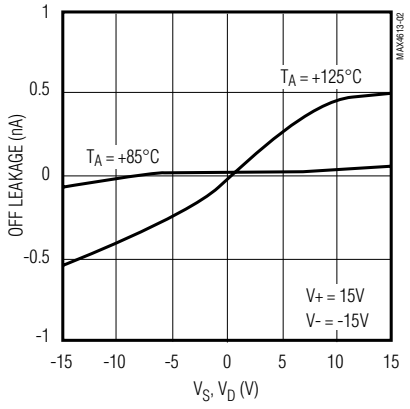
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

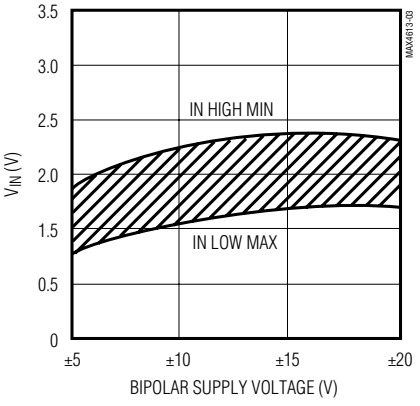
ON LEAKAGE CURRENTS



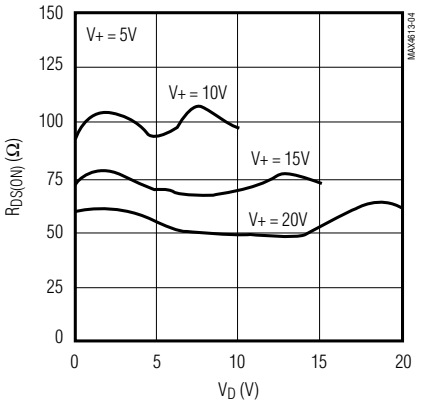
OFF LEAKAGE CURRENTS



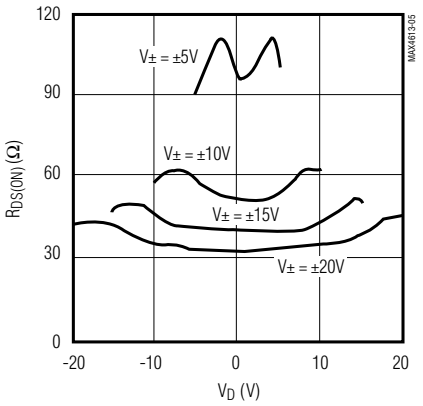
SWITCHING THRESHOLD vs. BIPOLAR SUPPLY VOLTAGE



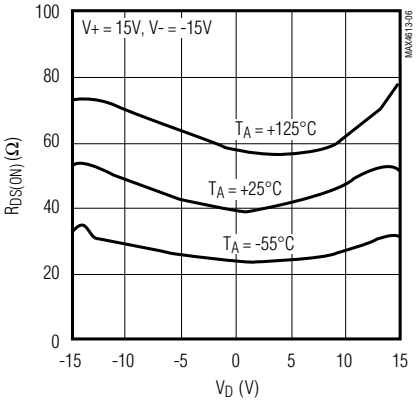
ON-RESISTANCE vs. V_D (UNIPOLAR SUPPLY VOLTAGE)



ON-RESISTANCE vs. V_D (BIPOLAR SUPPLY VOLTAGE)



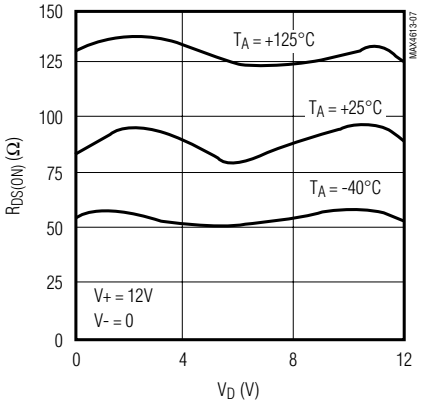
ON-RESISTANCE vs. V_D (BIPOLAR SUPPLY VOLTAGE AND TEMPERATURE)



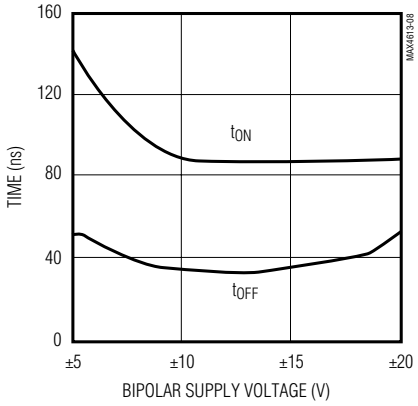
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

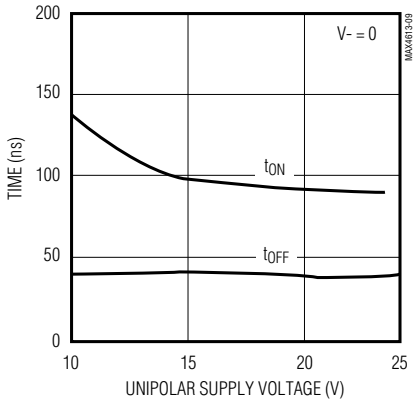
ON-RESISTANCE vs. V_D (UNIPOLAR SUPPLY VOLTAGE AND TEMPERATURE)



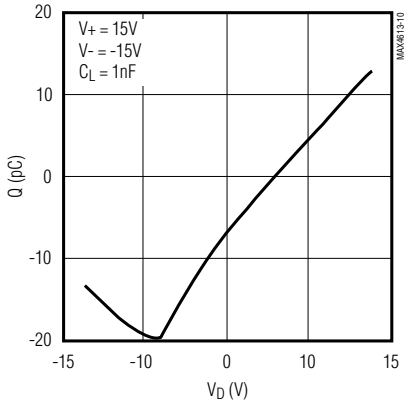
SWITCHING TIME vs. BIPOLAR SUPPLY VOLTAGE



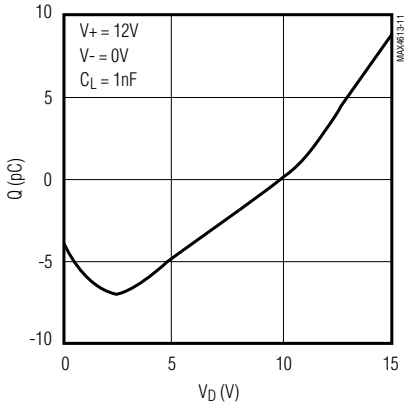
SWITCHING TIME vs. UNIPOLAR SUPPLY VOLTAGE



CHARGE INJECTION vs. V_D VOLTAGE



CHARGE INJECTION vs. V_D VOLTAGE



Quad, SPST Analog Switch

Pin Description

PIN		NAME	FUNCTION
DIP/SO/TSSOP	THIN QFN		
1, 8, 9, 16	6, 7, 14, 15	IN1–IN4	Logic Control Input
2, 7, 10, 15	5, 8, 13, 16	D1–D4	Analog-Switch Drain Output
3, 6, 11, 14	1, 4, 9, 12	S1–S4	Analog-Switch Source Output
4	2	V-	Negative-Supply Voltage Input
5	3	GND	Ground
12	10	V_L	Logic-Supply Voltage Input
13	11	V+	Positive-Supply Voltage Input—Connected to Substrate
—	EP	PAD	Exposed Pad. Connect PAD to V+.

Applications Information

General Operation

1) Switches are open when power is off.
2) IN_, D_, and S_ should not exceed V+ or V-, even with the power off.
3) Switch leakage is from each analog switch terminal to V+ or V-, not to other switch terminals.

Operation with Supply Voltages Other than ±15V

Using supply voltages less than ±15V will reduce the analog signal range. The MAX4613 operates with ±4.5V to ±20V bipolar supplies or with a +4.5V to +40V single supply; connect V- to GND when operating with a single supply. Also, all device types can operate with unbalanced supplies such as +24V and -5V. V_L must be connected to +5V to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with ±20V, ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V_L, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

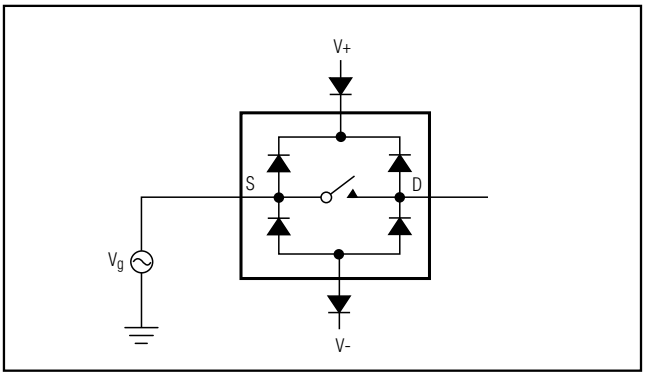


Figure 1. Overvoltage Protection Using External Blocking Diodes

Timing Diagrams/Test Circuits

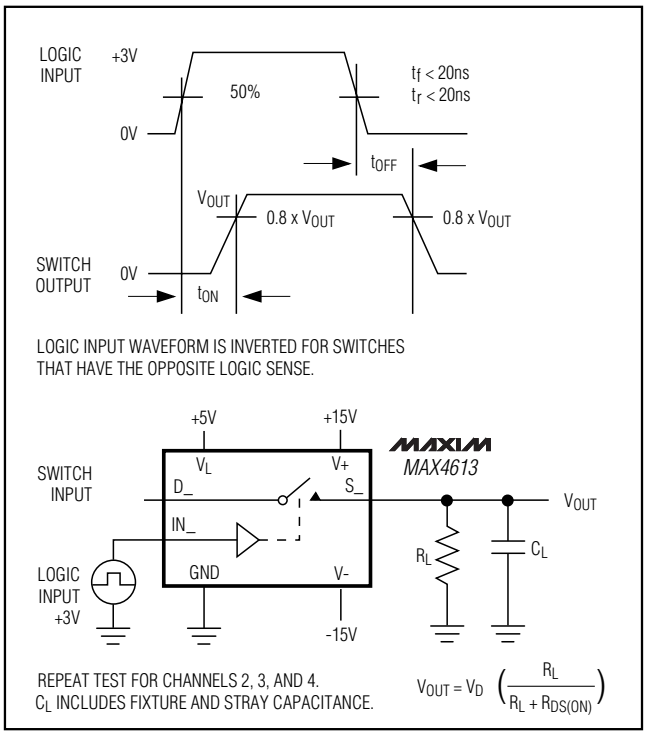


Figure 2. Switching Time

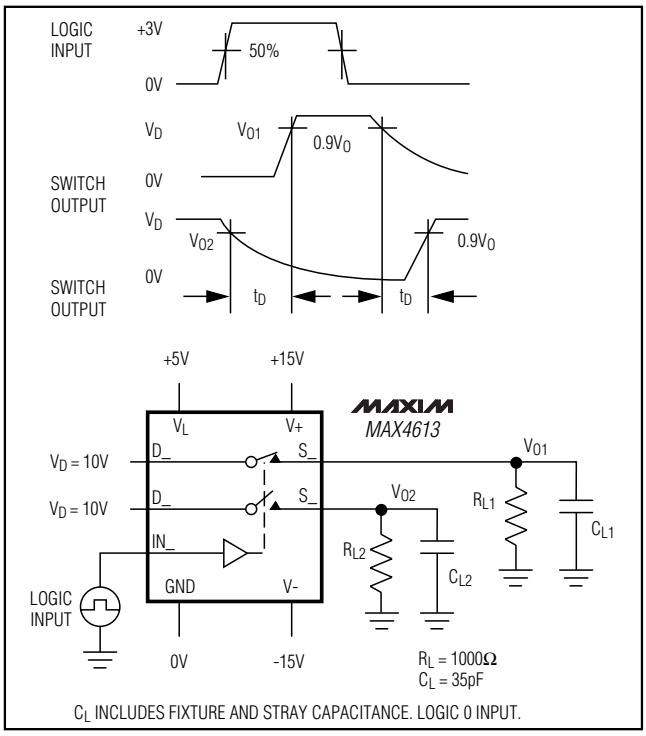


Figure 3. Break-Before-Make Test Circuit

Revision History

Pages changed at Rev 3: 1, 9, 10

Timing Diagrams/Test Circuits (continued)

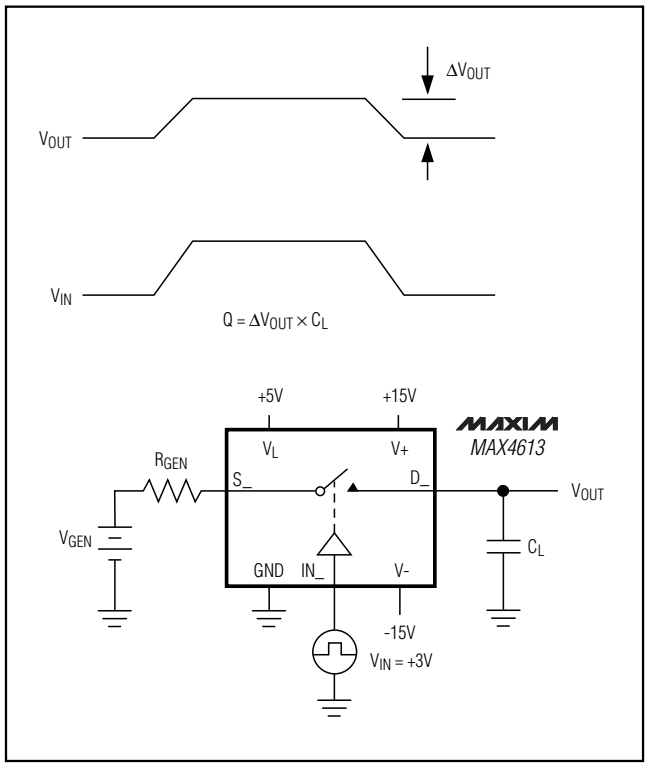


Figure 4. Charge Injection

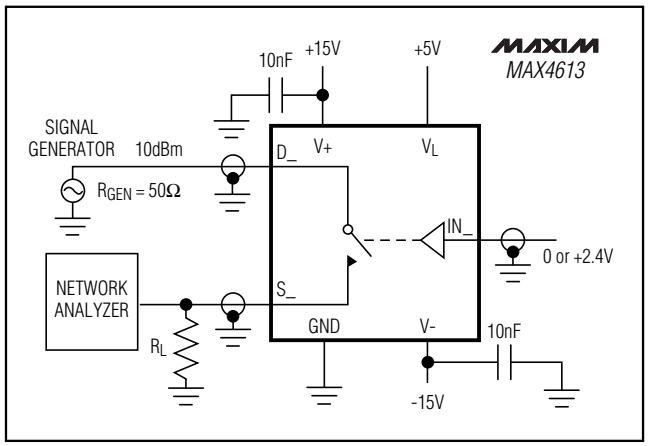


Figure 5. Off-Isolation Rejection Ratio

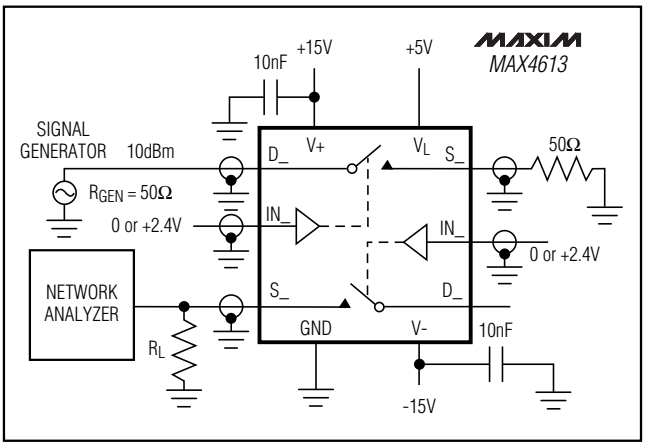


Figure 6. Crosstalk

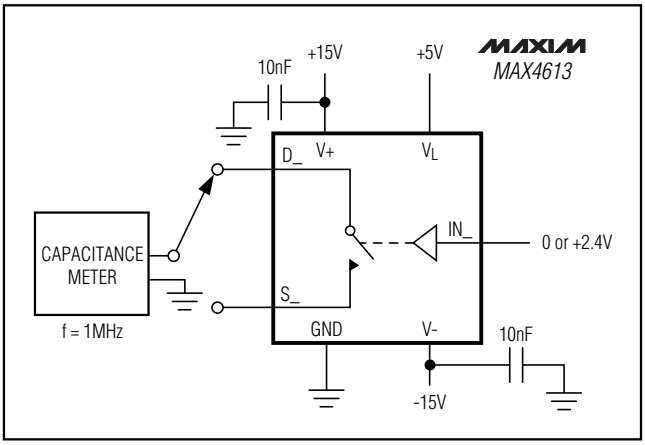


Figure 7. Source/Drain-Off Capacitance

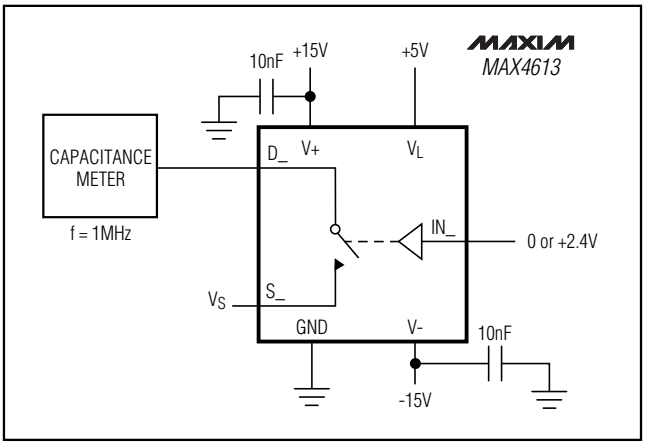
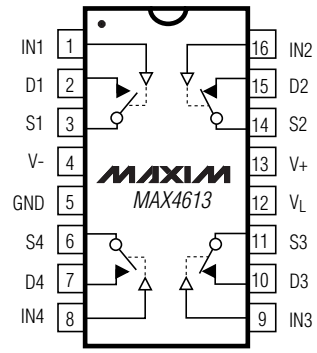


Figure 8. Source/Drain-On Capacitance

Pin Configurations (continued)



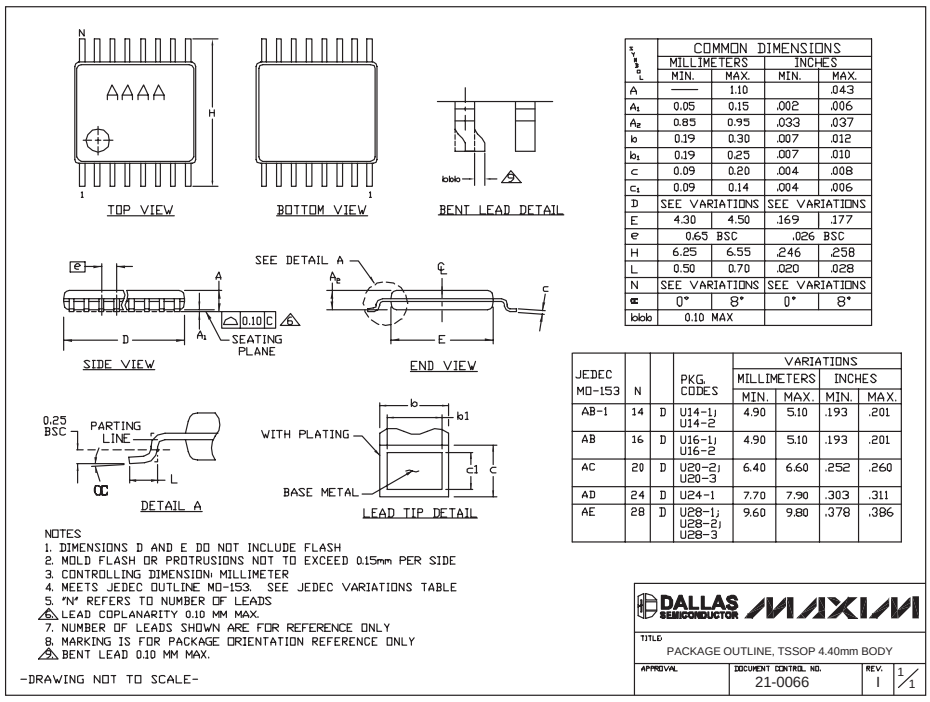
DIP/SO/QSOP/TSSOP

LOGIC	SW_1, SW_4	SW_2, SW_3
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



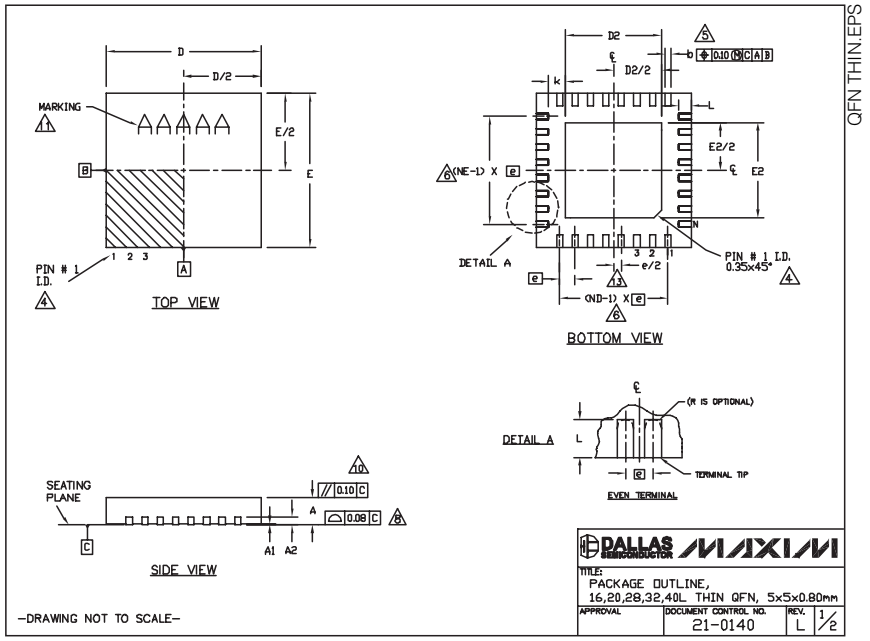
SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1; U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1; U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2; U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1; U28-2; U28-3	9.60	9.80	.378	.386

Quad, SPST Analog Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm
APPROVAL
DOCUMENT CONTROL NO. 21-0140
REV. L
2/2

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