R2A20152NS/SP

8-bit 2ch D/A Converter with Buffer Amplifiers for I²C BUS (Corresponds to Fast mode)

R03DS0013EJ0100
Rev.1.00
2011.09.05

Description

The R2A20152 is an integrated circuit semiconductor of CMOS structure with 2 channels of built in D/A converters with output buffer operational amplifiers. It is the characteristic improvement version of M62332.

The input interface is I²C Bus serial data method, and connects with a microcomputer with minimum wiring. It conforms FAST-MODE of I²C BUS Specifications.

The output circuit is composed of buffer operational amplifier with sync and source drive capacity of 1.0 mA or more, and it operates in the whole voltage range from VCC to ground.

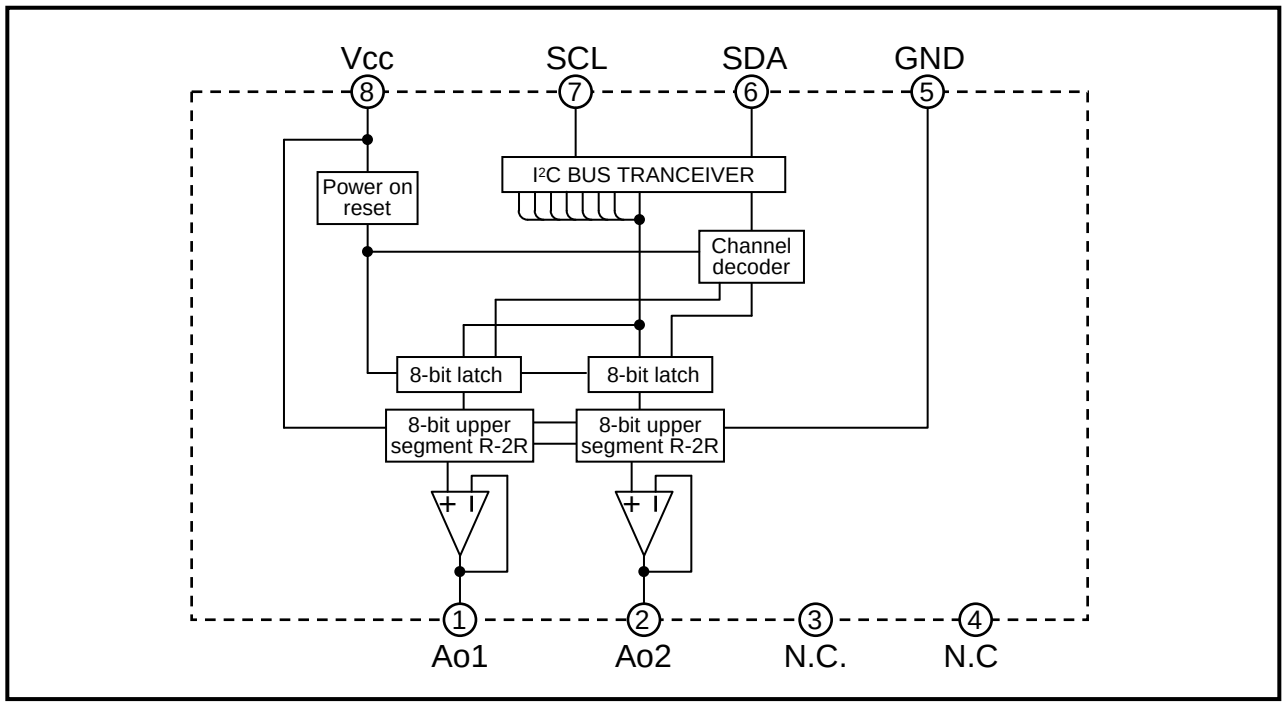
Features

- Guarantee Differential nonlinearity error : +/-0.7LSB, Nonlinearity error : +/-1.0LSB
- Digital data transfer format: I²C BUS serial data method (Corresponds to Fast mode: 400kHz)
- Output buffer operational amplifier: It operates in the whole voltage range from VCC to ground.
- High output current drive capacity: +/-1.0 mA over
- Very small size SON-8 package

Application

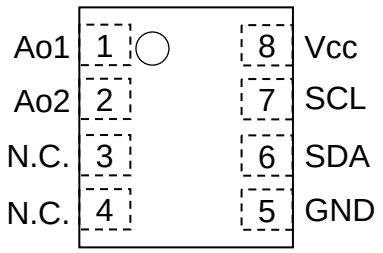
Conversion from digital data to analog control data for home-use and industrial equipment.
Signal gain control or automatic adjustment of LCD-TV, PDP-TV, LCD-monitor, or etc.
Blurring correction control or various control of the interchangeable lens of digital camera.

Block Diagram



Pin Arrangement

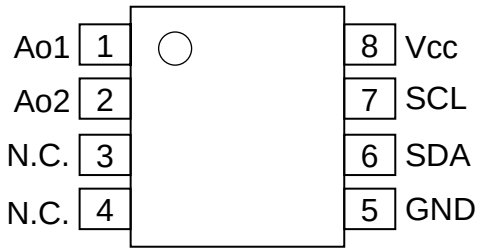
R2A20152NS



(Top view) N.C. : Not connected

Outline: PWSN0008KA-A (SON-8) [NS]

R2A20152SP



(Top view) N.C. : Not connected

Outline: PRSP0008DE-C (SOP-8) [SP]

Pin Description

Pin No.	Pin Name	Function
1	Ao1	8-bit resolution D-A converter output terminal (After power on, analog output of every channel is set in DAC data "00h")
2	Ao2	
3	N.C.	Not connected
4	N.C.	
5	GND	GND terminal
6	SDA	Serial data input terminal
7	SCL	Serial clock input terminal
8	Vcc	Power supply terminal

Absolute Maximum Ratings

Ta= 25deg, unless otherwise noted)

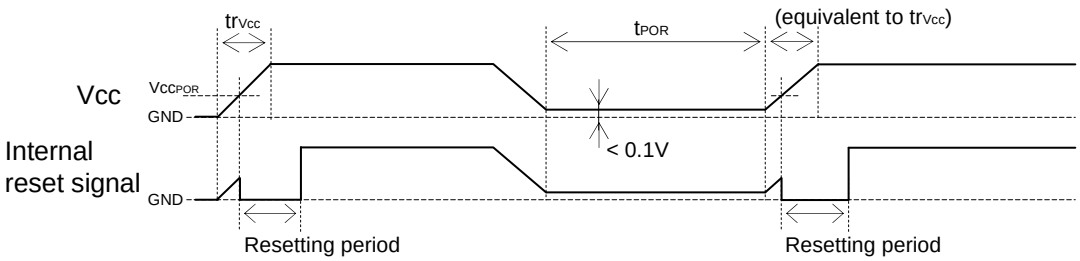
Item	Symbol	Condition	Ratings	Unit
Supply Voltage	Vcc		-0.3 to +6.5	V
Input Voltage	Vin		-0.3 to Vcc+0.3 < +6.5	V
Output Voltage	Vo		-0.3 to Vcc+0.3 < +6.5	V
Buffer amp. Output current	I_{AO}	Continuous	-2.0 to +2.0	mA
Power dissipation	Pd	Ta = +85deg	270(NS) / 272(SP)	mW
Thermal derating factor	K theta	Ta > +25deg	6.75(NS) / 6.8(SP)	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

Electrical Characteristics

(Vcc= +5V +/-10%, GND=0V, Ta= -30 to +85deg, unless otherwise noted)

Item	Symbol	Test Condition	Ratings			Unit
			Min.	Typ.	Max.	
Supply voltage	Vcc		2.7	5.0	5.5	V
Supply current	Icc	CLK = 500kHz, I_{AO} = 0µA, DATA: 6Ah (at maximum current)	0	0.5	1.5	mA
		SDA = SCL = GND, I_{AO} = 0µA	0	0.3	1.0	mA
Rise time of supply voltage *1	tr_{Vcc}	Vcc = 0 to 2.7V	100	-	-	µs
Internal reset operating voltage *1	Vcc_{POR}	Vcc = 0 to 2.7V	-	1.5	1.9	V
Power supply restart interval (Power supply OFF → ON) *1	t_{POR}	Vcc < 0.1V	1	-	-	ms
Input leak current	I_{ILK}	V_{IN} = 0 to Vcc	-10	-	10	µA
Input low voltage	V_{IL}		0	-	0.2Vcc	V
Input high voltage	V_{IH}		0.8Vcc	-	Vcc	V
Hysteresis of Schmitt trigger input (SDA, SCL)	Vhys		0.5	0.8	-	V
Output low voltage (SDA)	V_{OL}	Isink =3mA	-	-	0.4	V
Pulse width of spike noise	t_{SP}		0	-	50	ns
Buffer amplifier output voltage range	V_{AO}	I_{AO} = 100µA	0.1	-	Vcc – 0.1	V
		I_{AO} = 500µA	0.2	-	Vcc – 0.2	
Buffer amplifier output Drive range	I_{AO}	Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity	S_{DL}	Vcc = 5.12V (20mV/LSB), without load (I_{AO} = 0µA)	-0.7	-	0.7	LSB
Nonlinearity	S_L		-1.0	-	1.0	LSB
Zero code error	S_{ZERO}		-2.0	-	2.0	LSB
Full scale error	S_{FULL}		-2.0	-	2.0	LSB
Output capacitate load	C_O		-	-	0.1	µF
Buffer amplifier output impedance	R_O		-	5.0	-	ohm

*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (t_{POR}).

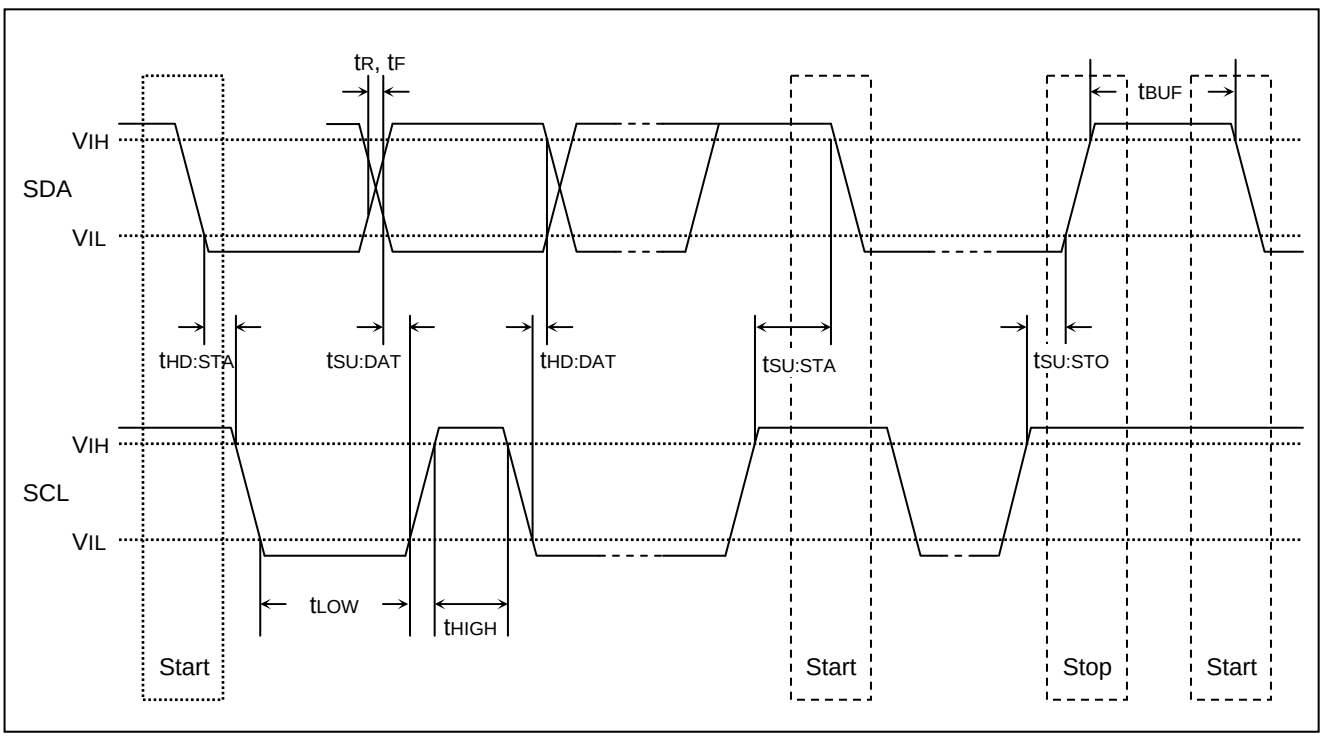


I²C BUS Line Characteristics

Item	Symbol	STANDARD MODE		FAST MODE		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	1.3	-	µs
Hold time (repeated) START condition After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data set-up time	$t_{SU:DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals	t_R	-	1000	-	300	ns
Fall time of both SDA and SCL signals	t_F	-	300	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	0.6	-	µs
Capacitive load of bus line	C_b	-	400	-	400	pF

Above values correspond with input level (V_{IH}min / V_{IL}max).

Timing Chart

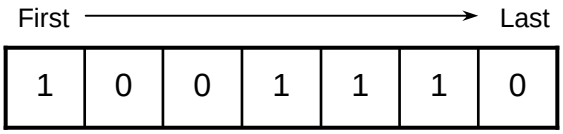


I²C BUS Format

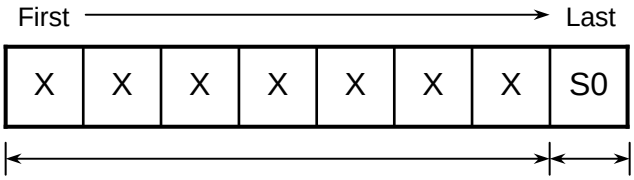
STA	Slave address	W	A	Sub address	A	DAC data	A	STP

Note: STA: START condition, W: write (SDA = Low), A: acknowledge bit, STP: STOP condition

• Slave address



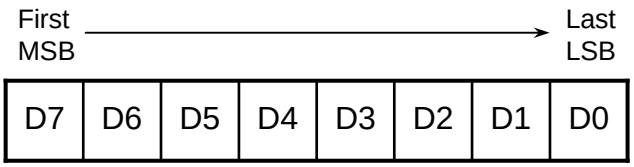
• Sub address



Channel select data

S0	Channel Selection
0	ch1 selection
1	ch2 selection

• DAC data

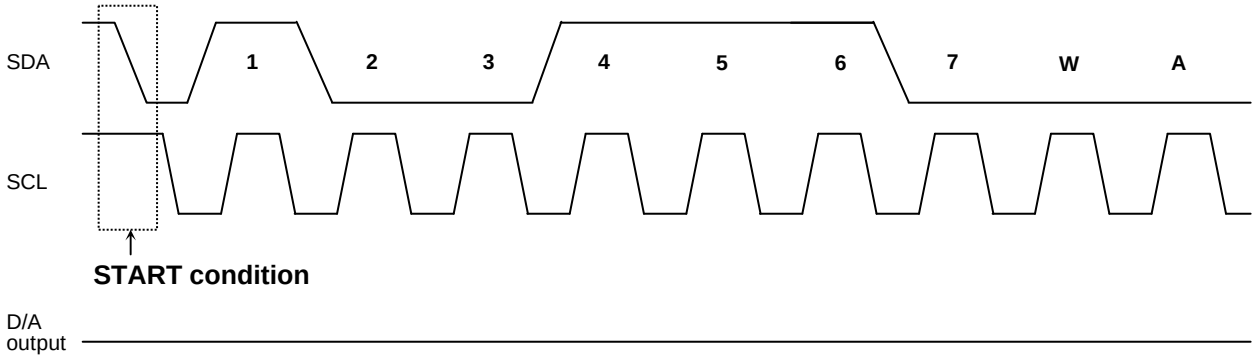


First MSB → Last LSB

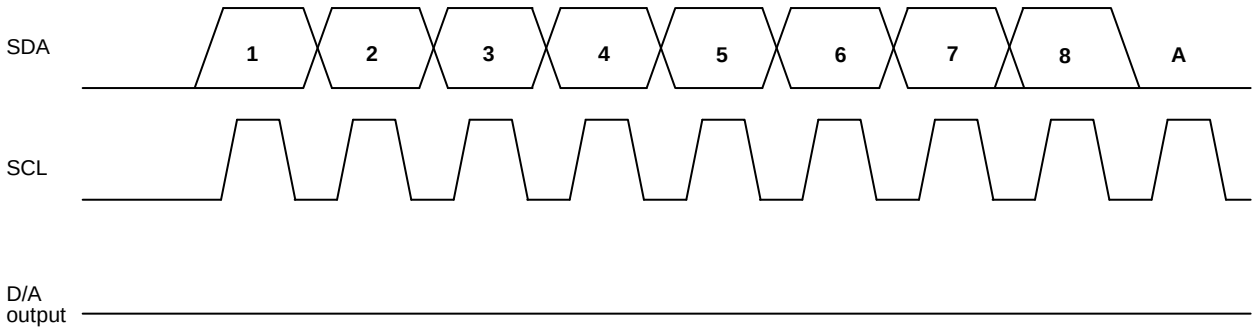
D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	Vcc / 256 X 1
0	0	0	0	0	0	0	1	Vcc / 256 X 2
0	0	0	0	0	0	1	0	Vcc / 256 X 3
0	0	0	0	0	0	1	1	Vcc / 256 X 4
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	Vcc / 256 X 255
1	1	1	1	1	1	1	1	Vcc

Data Timing Chart SCL and SDA (Model)

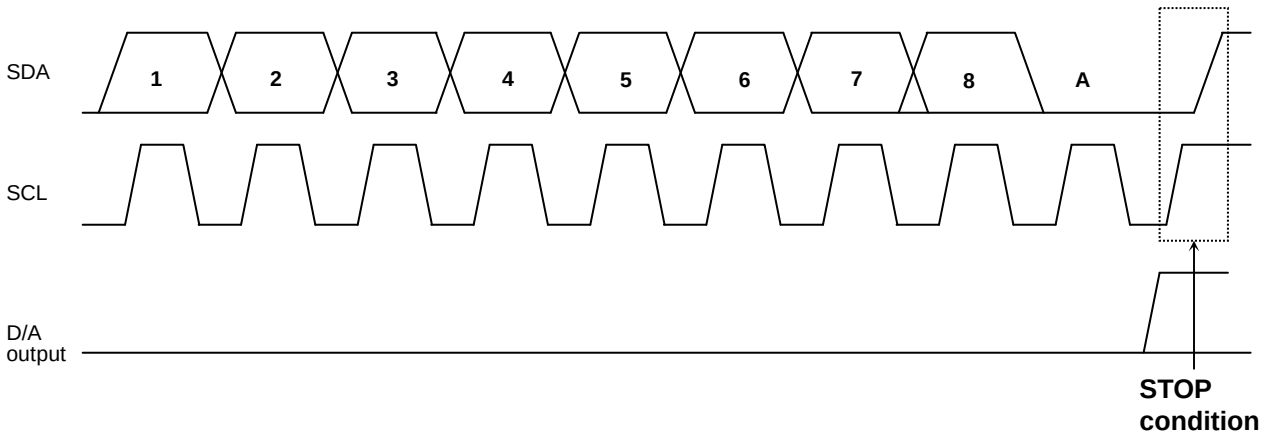
< START condition to sleve address bit >



< Sub address bit >

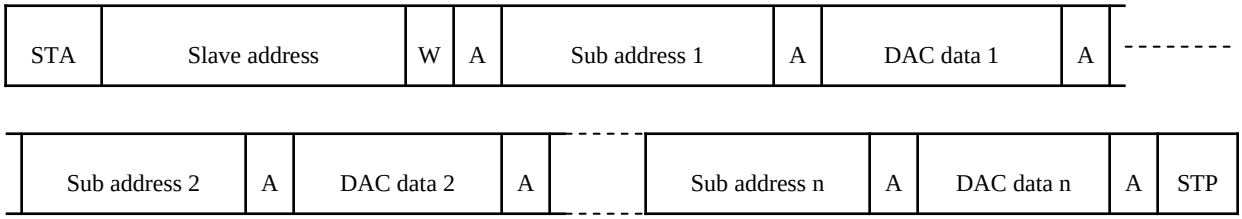


< DAC data bit to STOP condition >



- START condition With SCL at High, SDA goes from High to Low.
- STOP condition With SCL at High, SDA goes from Low to High.
  (Under normal condition, SDA must be changed, when SCL is Low.)
- Acknowledge bit The receiving IC has to pull down SDA line whenever receive slave data
  (Transmitting IC releases the SDA line just then transmit 8-bit data.)

Digital Data Formats

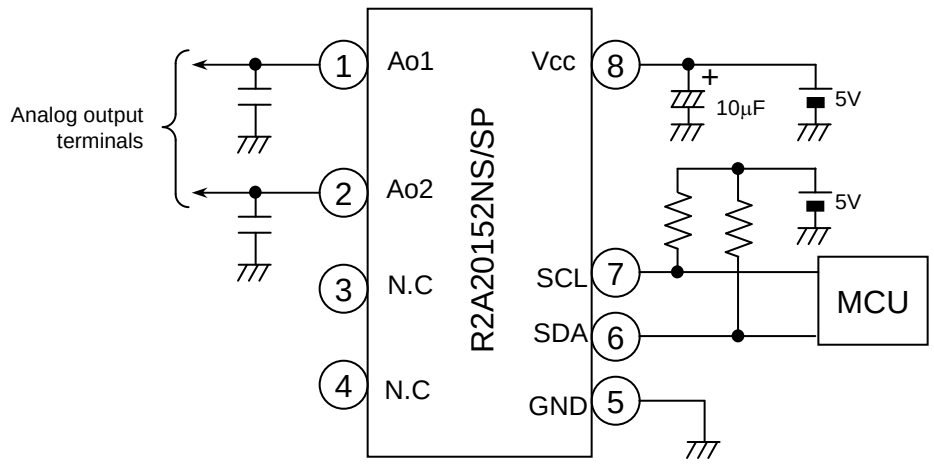


Note: After START condition, the master IC (MCU etc.) accesses the slave IC by slave address, and transmits the data to each channel by two bytes (sub address and DAC data).

Precaution for Use

1. Supply voltage terminal (VCC) is also used for D/A converter upper reference voltage setting. If ripple or spike is input this terminal, accuracy of D/A conversion is down. So, when use this device, please connect capacitor among VCC to GND for stable D/A conversion.
2. This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when the capacitor (0.1µF Max) is connected among output to GND for every noise elimination.

Standard Application Circuit



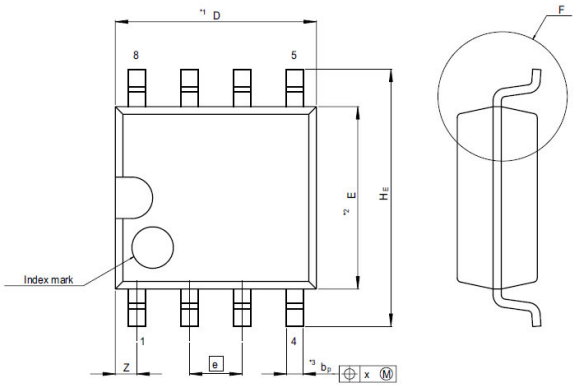
Ordering Information

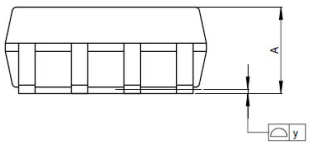
Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20152SP	SOP-8	PRSP0008DE-C	SP	Embossed Taping/2,500 pcs.
R2A20152NS	SON-8	PWSN0008KA-A	NS	Embossed Taping/5,000 pcs.

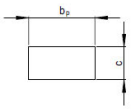
Package Dimensions

PRSP0008DE-C [SP]

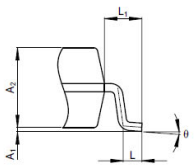
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g







Terminal cross section
(Ni/Pd/Au plating)



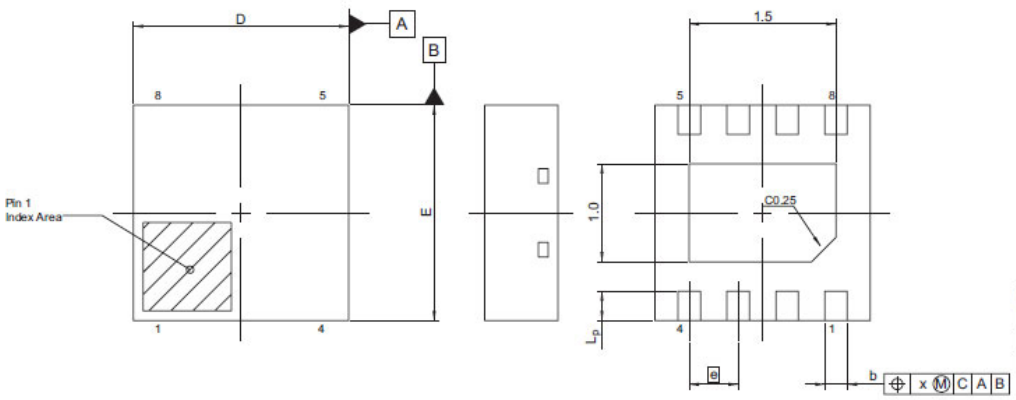
Detail F

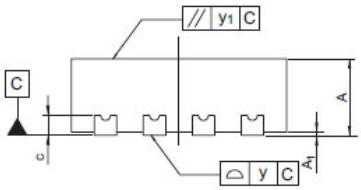
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A_2	—	1.85	—
A_1	0.00	0.1	0.20
A	—	—	2.03
b_p	0.34	0.4	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.7	6.2	6.5
e	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L_1	—	0.90	—

PWSN0008KA-A [NS]

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWSON8-2.2x2.2-0.50	PWSN0008KA-A	—	0.011g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	2.10	2.20	2.30
E	2.10	2.20	2.30
A_2	—	—	—
A	—	—	0.80
A_1	0	—	0.05
b	0.18	0.23	0.28
b_1	—	—	—
e	—	0.5	—
L_p	0.20	0.30	0.40
x	—	—	0.1
y	—	—	0.08
y_1	—	—	0.1
t	—	—	—
H_D	—	—	—
H_E	—	—	—
Z_D	—	—	—
Z_E	—	—	—
c	—	0.20	—
c_1	—	—	—

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