

**Revision History**

4M x 16 bit Low Power CMOS SRAM

**AS6C6416-55BIN 48ball FBGA PACKAGE**

Revision	Details	Date
Rev 1.0	Preliminary datasheet	June 08 2017

## FEATURE

- Fast access time : 55ns
- Low power consumption:  
Operating current : 12mA (TYP.)  
Standby current : 12μA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- **ROHS Compliant**
- Package : 48-ball 8mm x 10mm TFBGA

## GENERAL DESCRIPTION

The AS6C6416-55BIN is a 67,108,864-bit low power CMOS static random access memory organized as 4,194,304 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

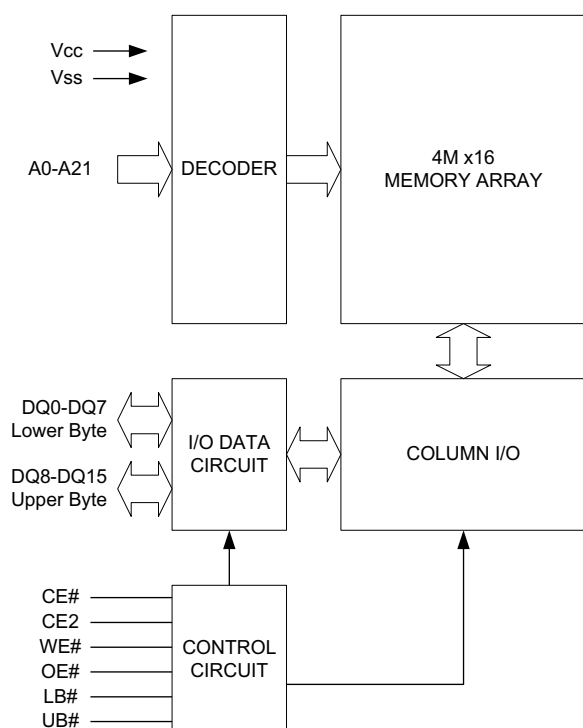
The AS6C6416-55BIN is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C6416-55BIN operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

## PRODUCT FAMILY

Product Family	Operating Temperature	V <sub>CC</sub> Range	Speed	Power Dissipation	
				Standby(I <sub>SB1</sub> , TYP. )	Operating(I <sub>CC</sub> , TYP.)
AS6C6416-55BIN	-40 ~ 85°C	2.7 ~ 3.6V	55ns	12μA	12mA

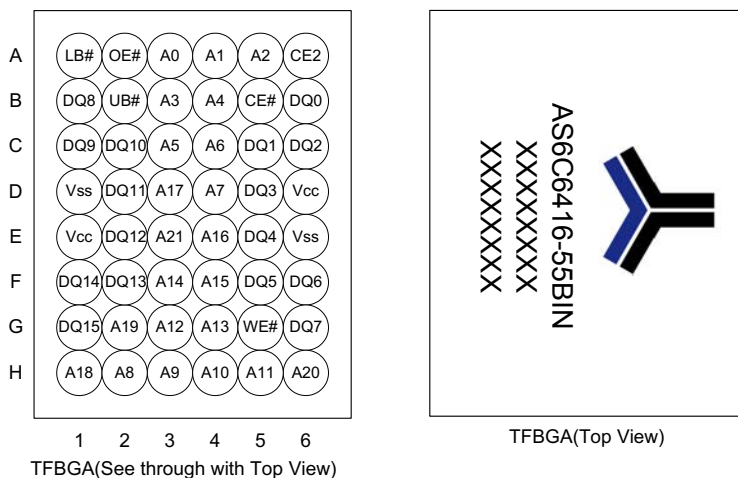
## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A21	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#, CE2	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on $V_{CC}$ relative to $V_{SS}$	$V_{T1}$	-0.5 to 4.6	V
Voltage on any other pin relative to $V_{SS}$	$V_{T2}$	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	$T_A$	-40 to 85(I grade)	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
							DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	X	High-Z	High-Z	$I_{SB1}$
	X	L	X	X	X	X	High-Z	High-Z	
	X	X	X	X	H	H	High-Z	High-Z	
Output Disable	L	H	H	H	L	X	High-Z	High-Z	$I_{CC}, I_{CC1}$
	L	H	H	H	X	L	High-Z	High-Z	
Read	L	H	L	H	L	H	$D_{OUT}$	High-Z	$I_{CC}, I_{CC1}$
	L	H	L	H	H	L	High-Z	$D_{OUT}$	
	L	H	L	H	L	L	$D_{OUT}$	$D_{OUT}$	
Write	L	H	X	L	L	H	$D_{IN}$	High-Z	$I_{CC}, I_{CC1}$
	L	H	X	L	H	L	High-Z	$D_{IN}$	
	L	H	X	L	L	L	$D_{IN}$	$D_{IN}$	

Note: H=  $V_{IH}$ , L=  $V_{IL}$ , X= Don't care.

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. <sup>*4</sup>	MAX.	UNIT
Supply Voltage	V <sub>CC</sub>			2.7	3.0	3.6	V
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>			2.2	-	V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>			- 0.2	-	0.6	V
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>		- 1	-	1	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> Output Disabled		- 1	-	1	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA		2.2	2.7	-	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA		-	-	0.4	V
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = MIN. CE# ≤0.2V and CE2 ≥V <sub>CC</sub> -0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> -0.2V		-	12	20	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤0.2V and CE2 ≥V <sub>CC</sub> -0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> -0.2V		-	3	5	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	40°C	-	12	36	μA
			85°C	-	-	160	μA

Notes:

1.  $V_{IH}(\max) = V_{CC} + 2.0V$  for pulse width less than 6ns.

2.  $V_{IL}(\min) = V_{SS} - 2.0V$  for pulse width less than 6ns.

3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.

4. Typical values, measured at  $V_{CC} = V_{CC}(\text{TYP.})$  and  $T_A = 25^\circ C$ , are included for reference only and are not guaranteed or tested.

## CAPACITANCE ( $T_A = 25^\circ C$ , $f = 1.0MHz$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	$C_{IN}$	-	15	pF
Input/Output Capacitance	$C_{I/O}$	-	20	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA$

## AC ELECTRICAL CHARACTERISTICS

### (1) READ CYCLE

PARAMETER	SYM.	AS6C6416-55BIN		UNIT
		MIN.	MAX.	
Read Cycle Time	$t_{RC}$	55	-	ns
Address Access Time	$t_{AA}$	-	55	ns
Chip Enable Access Time	$t_{ACE}$	-	55	ns
Output Enable Access Time	$t_{OE}$	-	30	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	20	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	20	ns
Output Hold from Address Change	$t_{OH}$	10	-	ns
LB#, UB# Access Time	$t_{BA}$	-	55	ns
LB#, UB# to High-Z Output	$t_{BHZ}^*$	-	20	ns
LB#, UB# to Low-Z Output	$t_{BLZ}^*$	10	-	ns

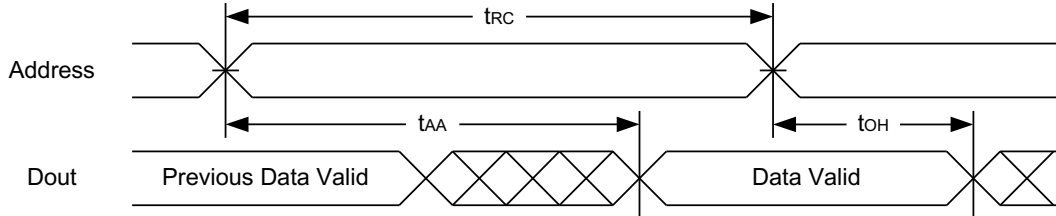
### (2) WRITE CYCLE

PARAMETER	SYM.	AS6C6416-55BIN		UNIT
		MIN.	MAX.	
Write Cycle Time	$t_{WC}$	55	-	ns
Address Valid to End of Write	$t_{AW}$	50	-	ns
Chip Enable to End of Write	$t_{CW}$	50	-	ns
Address Set-up Time	$t_{AS}$	0	-	ns
Write Pulse Width	$t_{WP}$	45	-	ns
Write Recovery Time	$t_{WR}$	0	-	ns
Data to Write Time Overlap	$t_{DW}$	25	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	20	ns
LB#, UB# Valid to End of Write	$t_{BW}$	50	-	ns

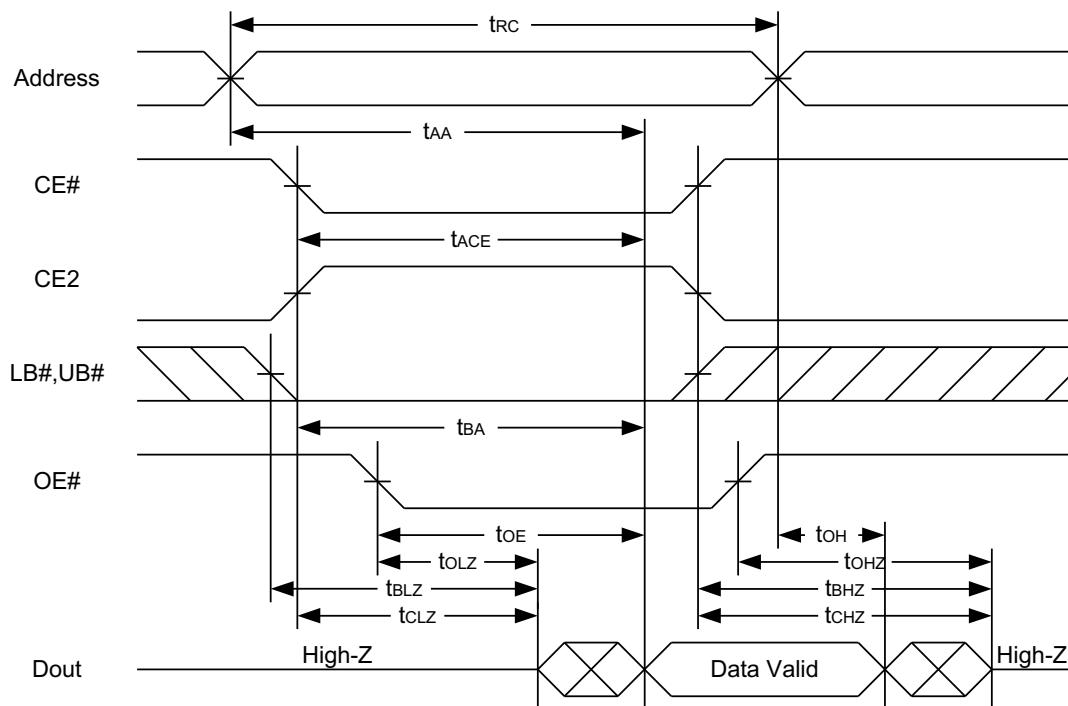
\*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

### READ CYCLE 1 (Address Controlled) (1,2)



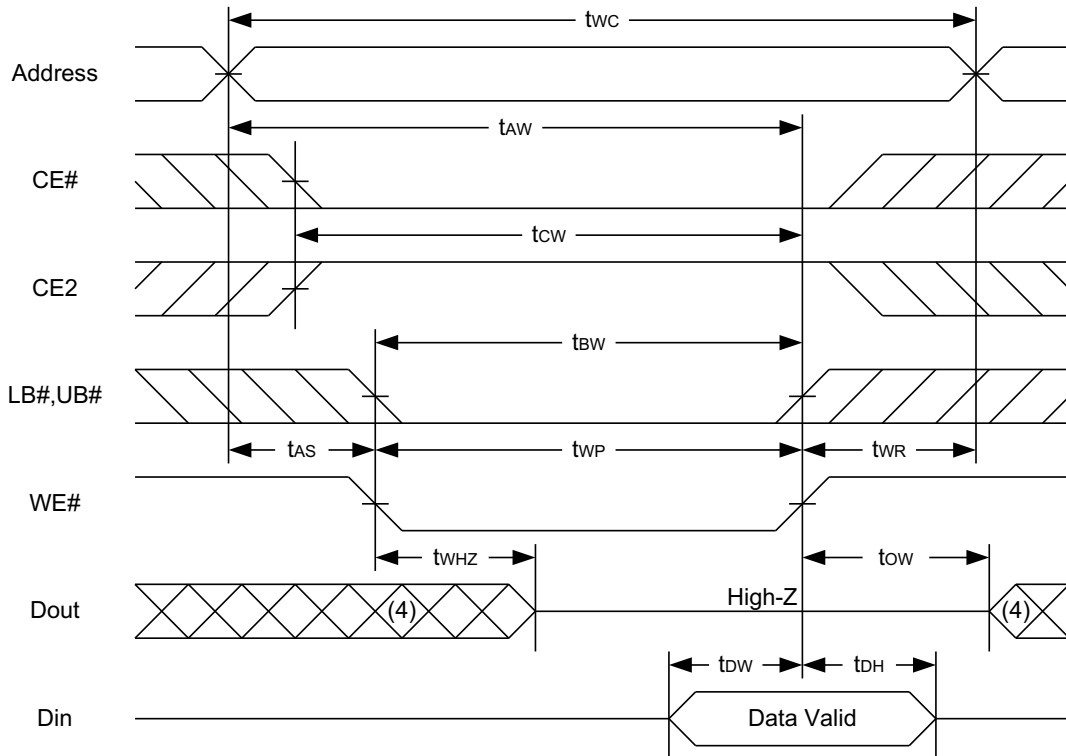
### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



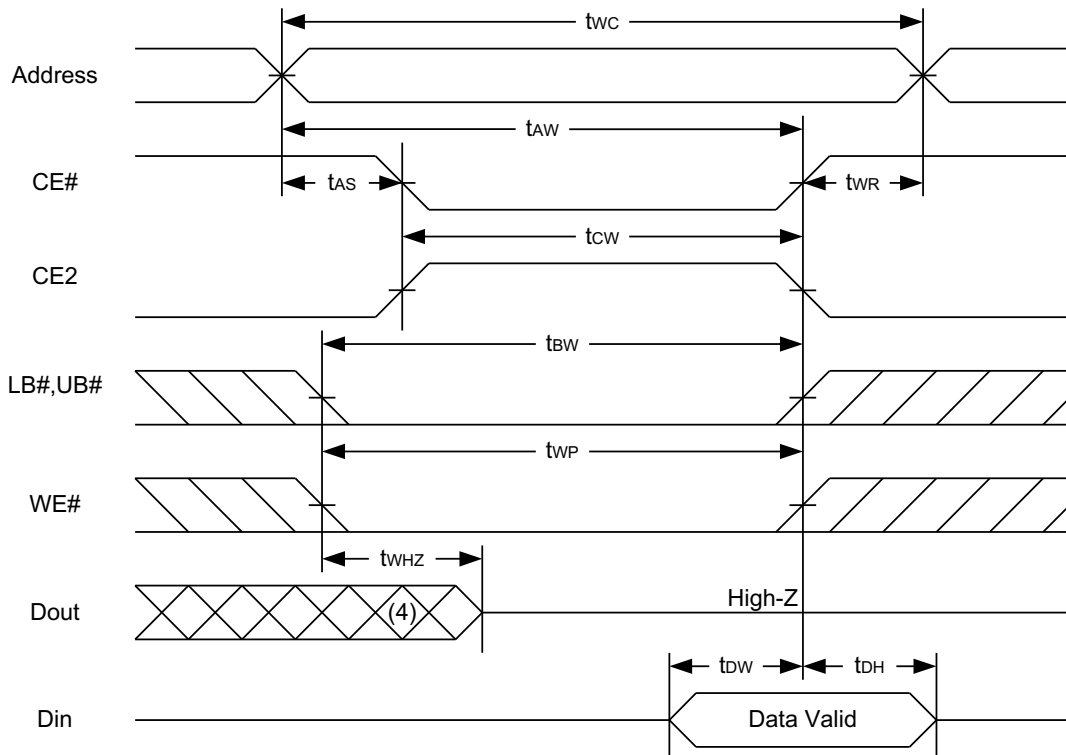
#### Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

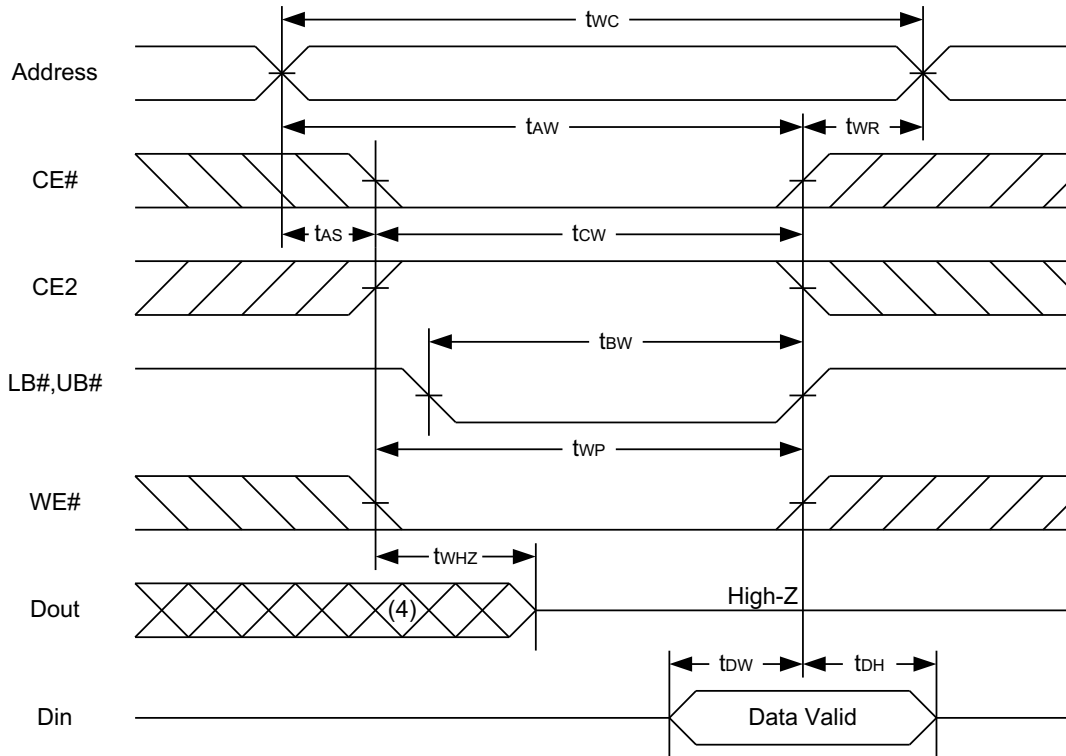
## WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



## WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



## WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



### Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.



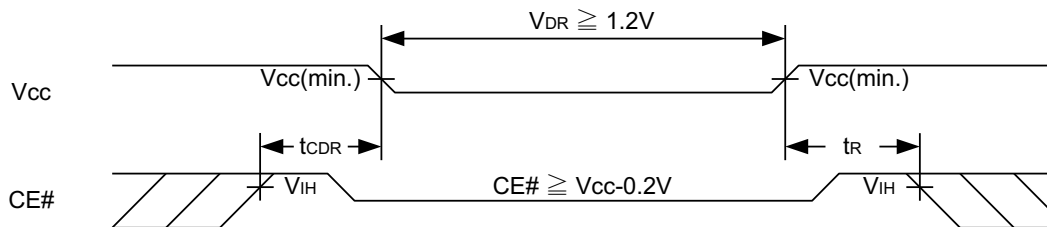
## DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥V <sub>CC</sub> - 0.2V or CE2 ≤0.2V		1.2	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.2V CE# ≥V <sub>CC</sub> -0.2V or CE2 ≤0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	40°C	-	10	36	μA
			85°C	-	-	160	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t <sub>R</sub>			t <sub>RC</sub> *	-	-	ns

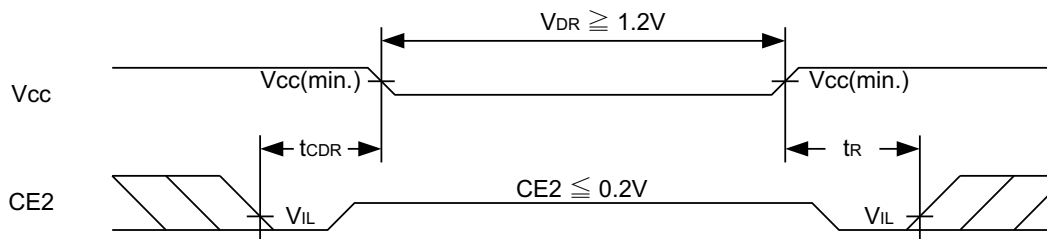
t<sub>RC</sub>\* = Read Cycle Time

## DATA RETENTION WAVEFORM

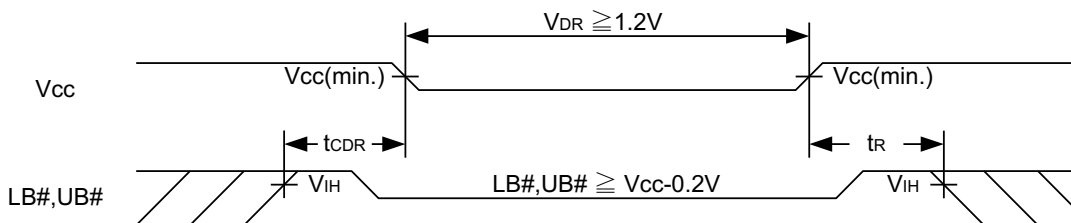
**Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)**



**Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)**

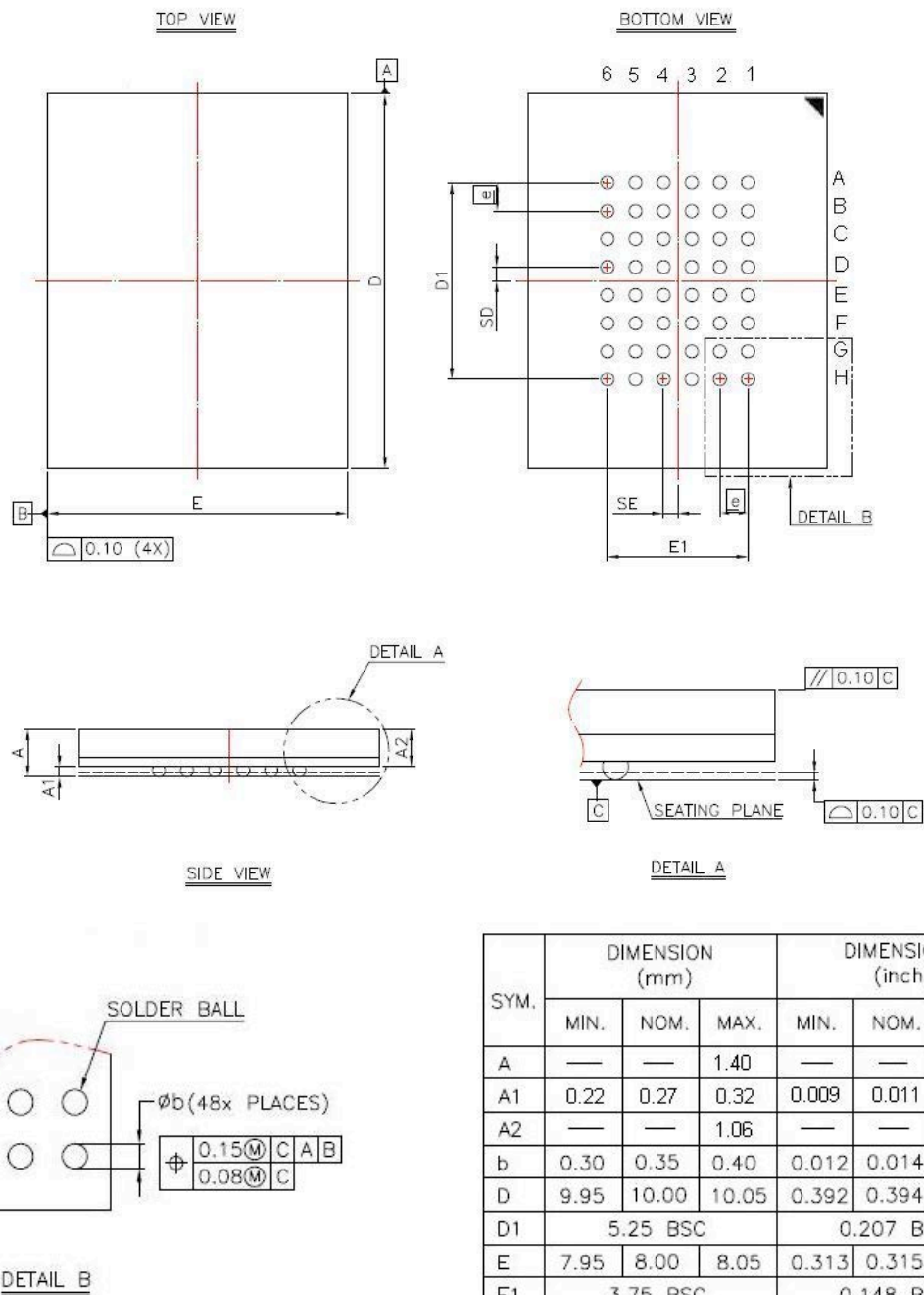


**Low V<sub>CC</sub> Data Retention Waveform (3) (LB#, UB# controlled)**



## PACKAGE OUTLINE DIMENSION

### 48-ball 8mm × 10mm TFBGA Package Outline Dimension



#### NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

## ORDERING INFORMATION

AS6C	6416	55	B	I	N	XX
SRAM	6416=4M x 16 Bit	Access Time 55=55ns	B = FBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel



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