



PMN50EPE

30 V, P-channel Trench MOSFET

16 April 2018

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Logic-level compatible
- Very fast switching
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	-	-30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t \leq 5 \text{ s}$	[1]	-	-	-6	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -4.6 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		-	35	45	$\text{m}\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	<p>TSOP6 (SOT457)</p>	<p>017aaa259</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
PMN50EPE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads		SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN50EPE	3L

8. Limiting values

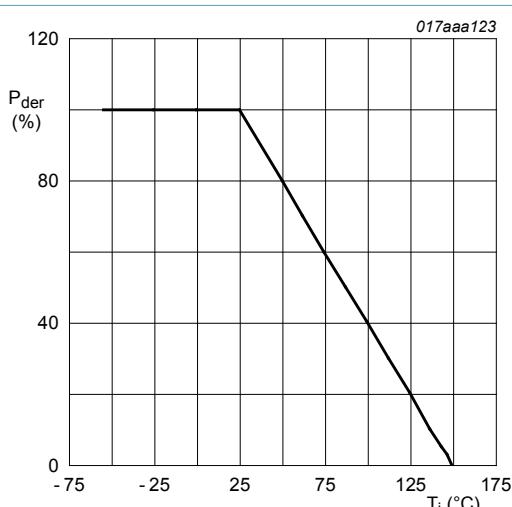
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-6	A
		V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-4.6	A
		V _{GS} = -10 V; T _{amb} = 100 °C	[1]	-	-2.9	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 µs		-	-19	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	560	mW
			[1]	-	1.4	W
		T _{sp} = 25 °C		-	6.25	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.4	A

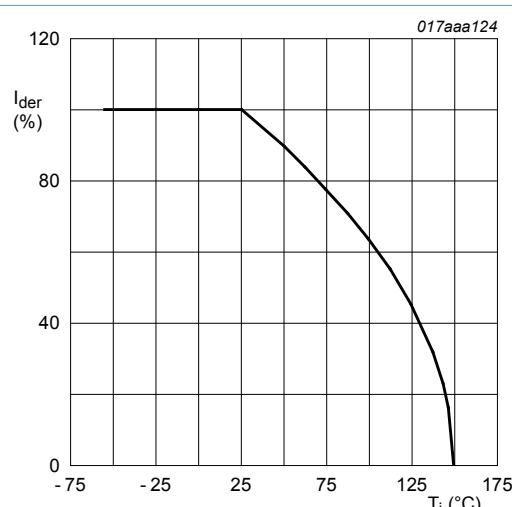
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}C)} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_D(25^{\circ}C)} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature

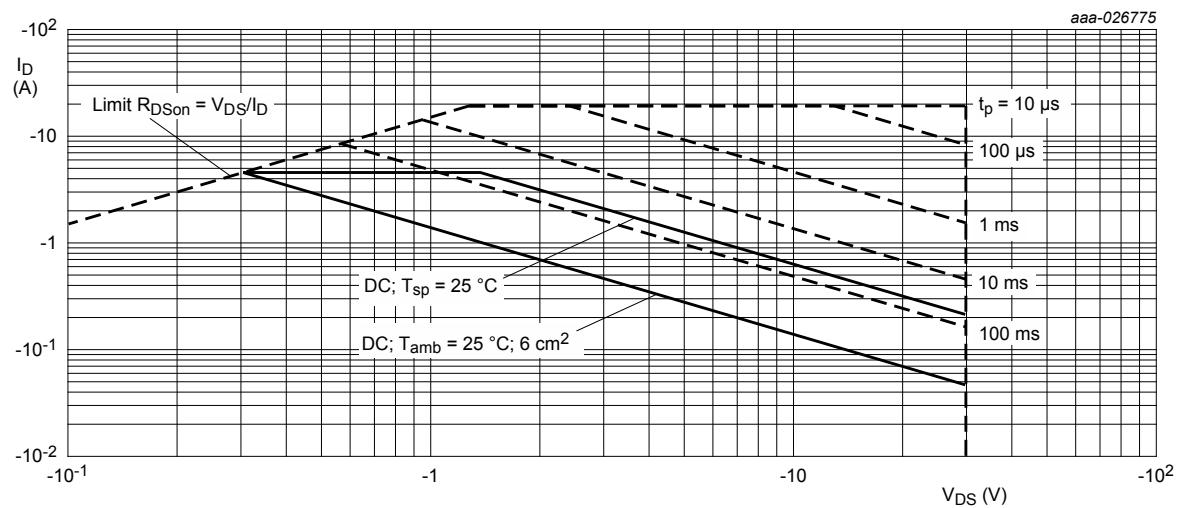


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	195	225	K/W
			[2]	-	78	90	K/W
		in free air; $t \leq 5$ s	[2]	-	55	63	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2 .

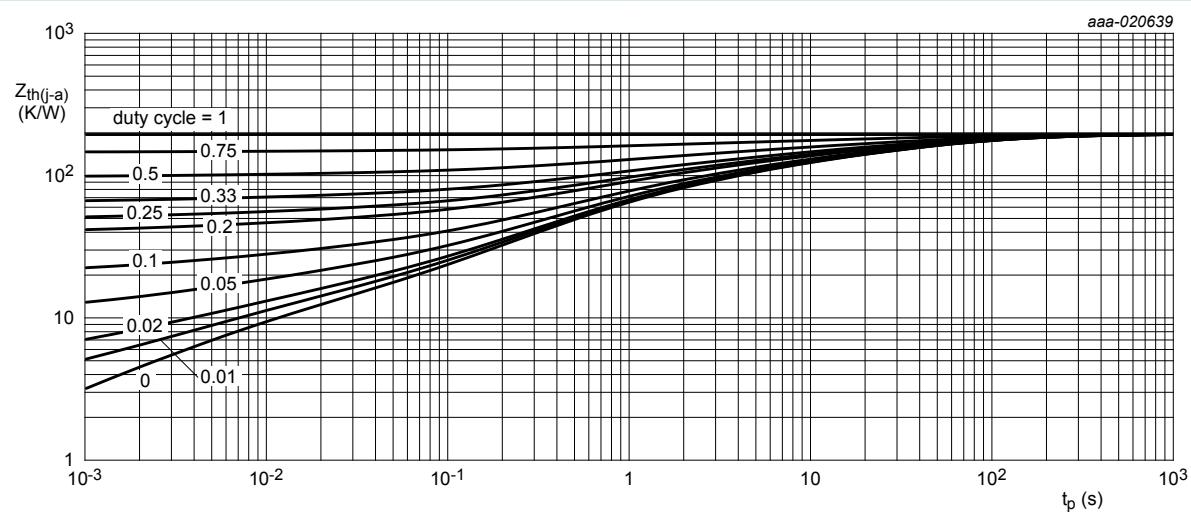


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

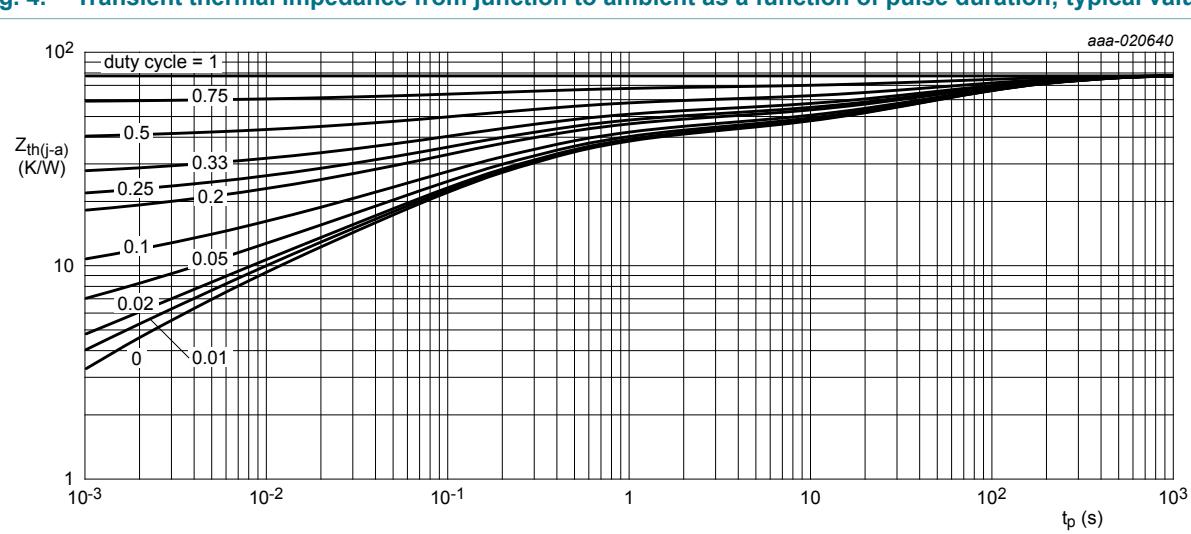


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		-30	-	-	V
V_{GSTh}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$		-1	-2	-3	V
I_{DSS}	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	10	μA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-10	μA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	2	μA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-2	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10 V; I_D = -4.6 A; T_j = 25^\circ C$		-	35	45	$m\Omega$
		$V_{GS} = -10 V; I_D = -4.6 A; T_j = 150^\circ C$		-	51	67	$m\Omega$
		$V_{GS} = -4.5 V; I_D = -3.6 A; T_j = 25^\circ C$		-	49	72	$m\Omega$
g_{fs}	forward transconductance	$V_{DS} = -10 V; I_D = -4.6 A; T_j = 25^\circ C$		-	14.2	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$		-	13	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15 V; I_D = -4.2 A; V_{GS} = -10 V; T_j = 25^\circ C$		-	12.8	20	nC
Q_{GS}	gate-source charge			-	2.2	-	nC
Q_{GD}	gate-drain charge			-	2.2	-	nC
C_{iss}	input capacitance	$V_{DS} = -15 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25^\circ C$		-	793	-	pF
C_{oss}	output capacitance			-	134	-	pF
C_{rss}	reverse transfer capacitance			-	84	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V; I_D = -4.2 A; V_{GS} = -10 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	6	-	ns
t_r	rise time			-	19	-	ns
$t_{d(off)}$	turn-off delay time			-	36	-	ns
t_f	fall time			-	19	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = -1.4 A; V_{GS} = 0 V; T_j = 25^\circ C$		-	-0.8	-1.2	V

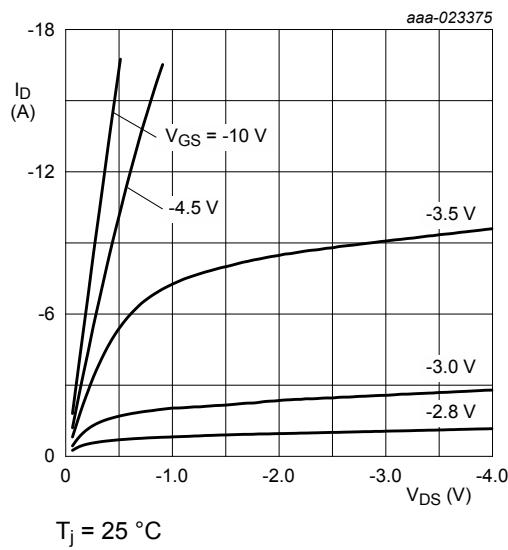


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

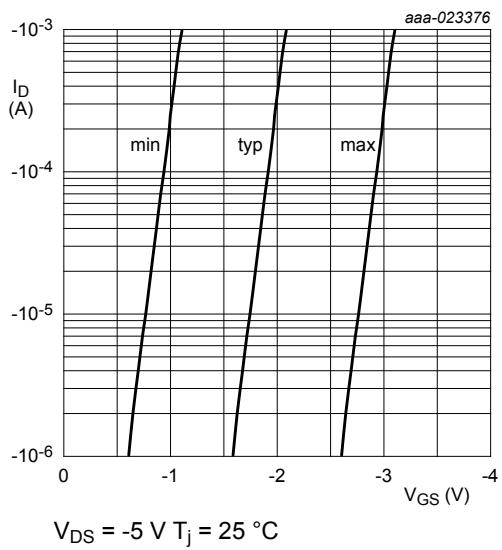


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

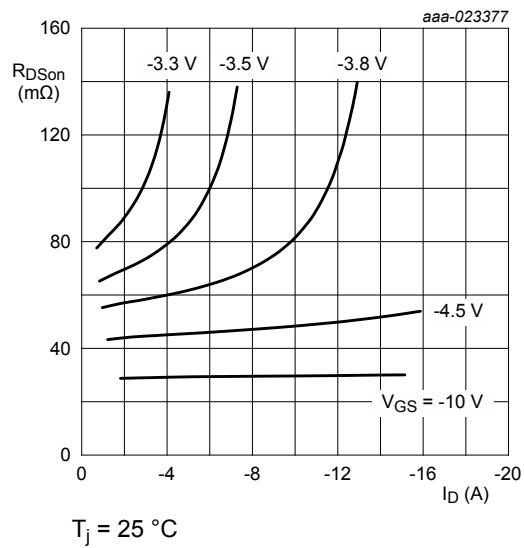


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

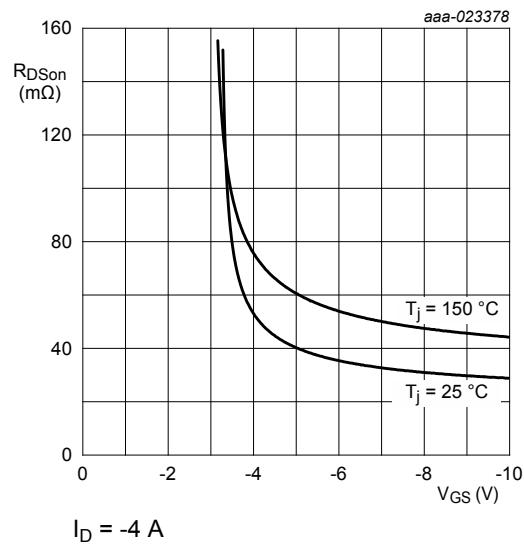


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

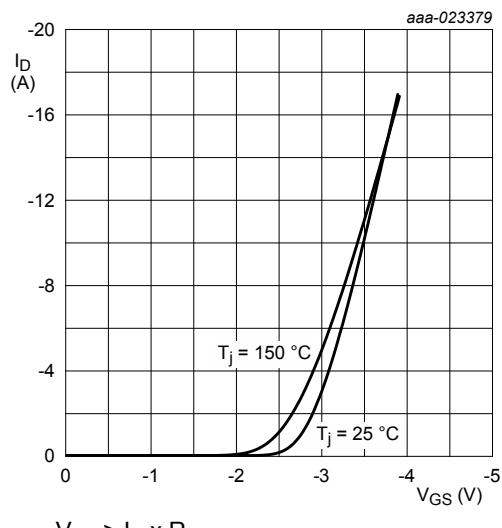


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

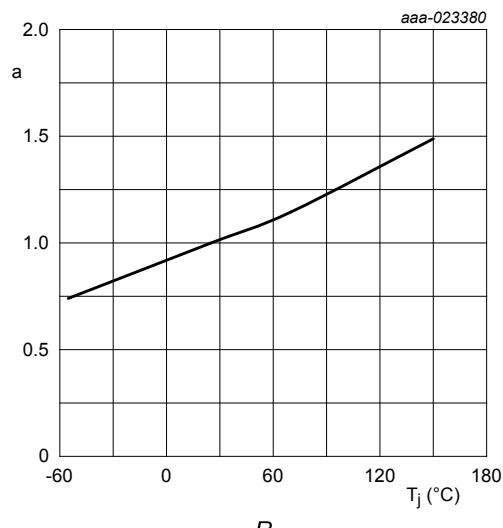


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

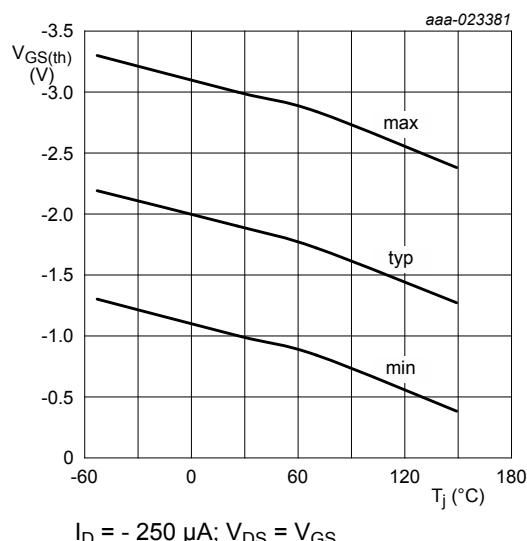


Fig. 12. Gate-source threshold voltage as a function of junction temperature

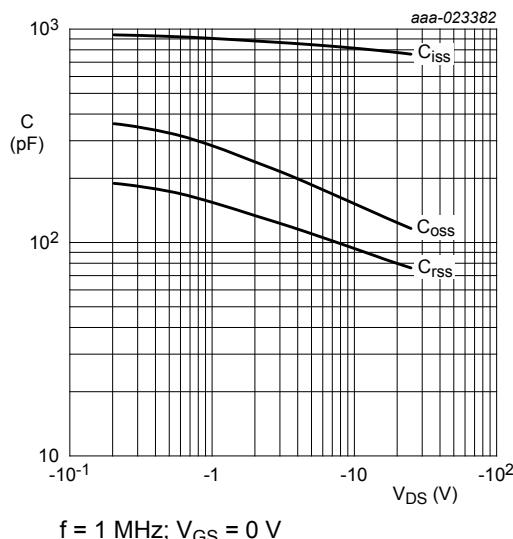
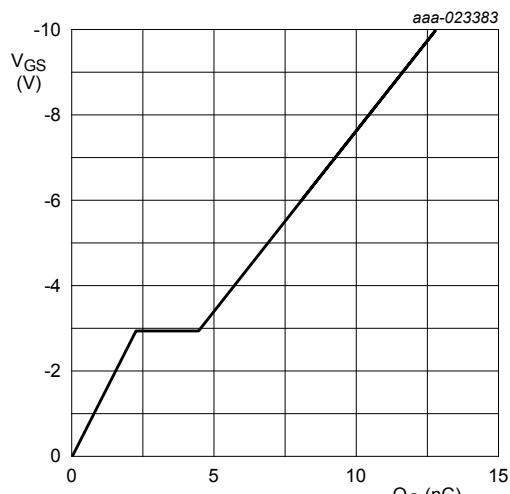


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -15$ V; $I_D = -4$ A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

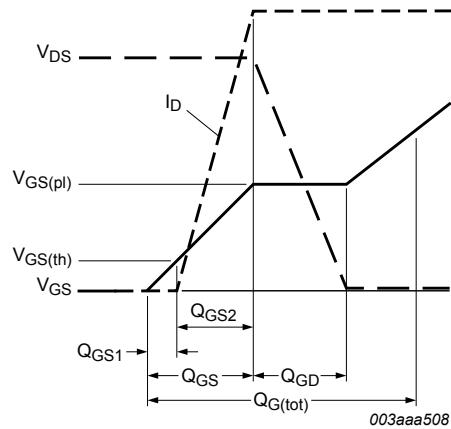
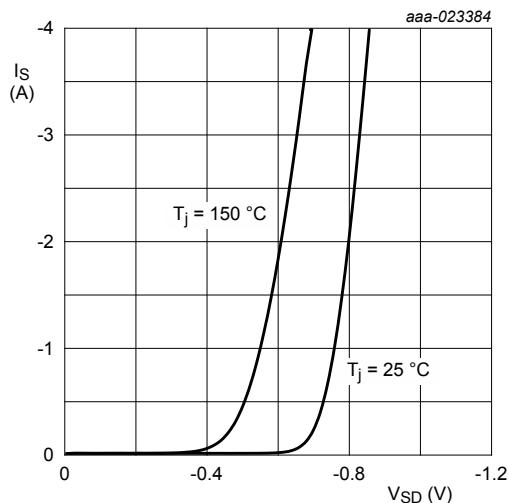


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

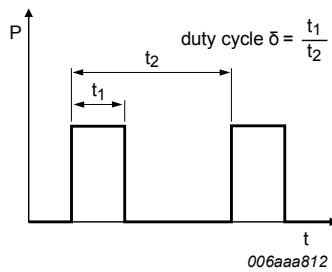


Fig. 17. Duty cycle definition

12. Package outline

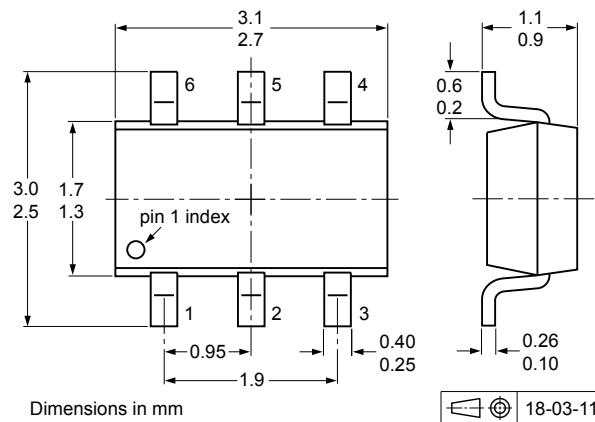


Fig. 18. Package outline TSOP6 (SOT457)

13. Soldering

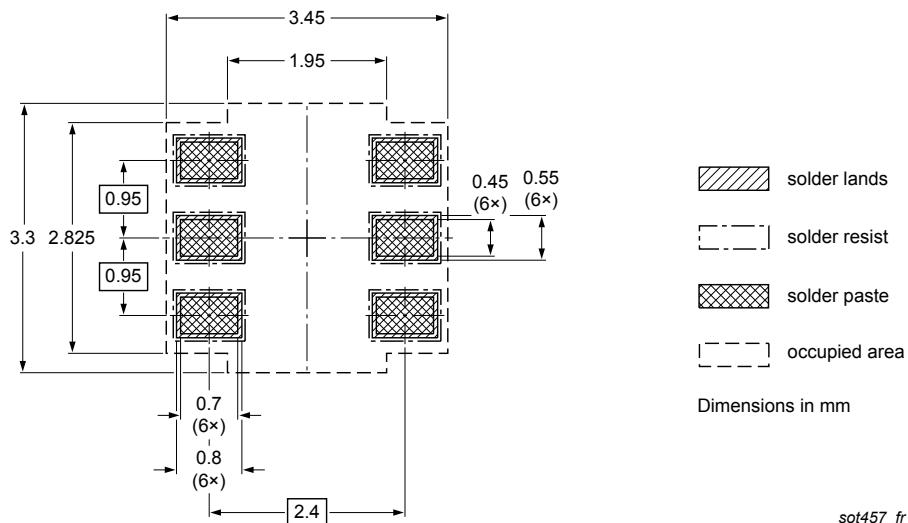


Fig. 19. Reflow soldering footprint for TSOP6 (SOT457)

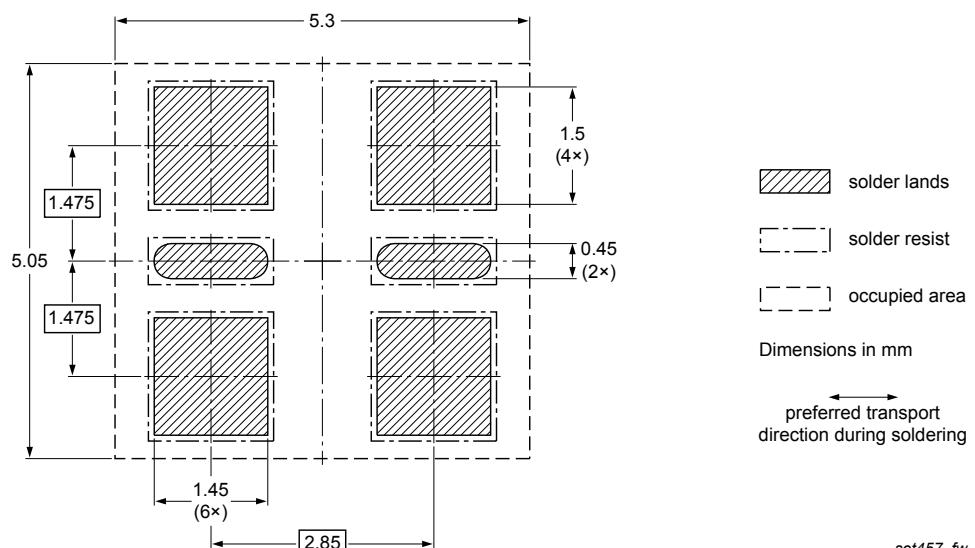


Fig. 20. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN50EPE v.1	20180416	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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