

RoHS Recast Compliant

Serial ATA Flash Drive

M.2 2242 P100-M Product Specifications (Toshiba 15nm)

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Version 1.1



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Features:

- **Compliance with SATA Interface**
 - Serial ATA Revision 3.1
 - SATA 6.0 Gbps
 - ATA-8 command set
 - Backward compatible with SATA 1.5/3.0 Gbps
- **Capacity**
 - 8, 16, 32, 64, 128, 256 GB
- **Performance***
 - Interface burst read/write: 600 MB/sec
 - Sustained read: up to 450 MB/sec
 - Sustained write: up to 165 MB/sec
- **Flash Management**
 - Built-in hardware ECC
 - Wear-leveling
 - Flash bad-block management
 - S.M.A.R.T.
 - Power Failure Management
 - ATA Secure Erase
 - TRIM
- **NAND Flash Type: MLC**
- **Endurance**
 - 8 GB: 7 TBW
 - 16 GB: 14 TBW
 - 32 GB: 28 TBW
 - 64 GB: 57 TBW
 - 128 GB: 114 TBW
 - 256 GB: 228 TBW
- **Temperature Range**
 - Operating:
 - Standard : 0°C to 70°C
 - Extended : -40°C to 85°C
 - Storage: -40°C to 100°C
- **Supply Voltage**
 - 3.3 V $\pm$ 5%
- **Power Consumption***
 - Active mode: 455 mA
 - Idle mode: 95 mA
- **Connector Type**
 - 75-pin SATA-based M.2 module pinout
- **Form Factor**
 - M.2 2242 form factor
 - Dimensions:
42mm(L)x22mm(W)x3.65mm(H)
- **Shock & Vibration****
 - Shock: 1,500 G
 - Vibration: 15 G
- **MTBF: >2,000,000 hours**
- **RoHS Recast Compliant**
- **Device Sleep Mode (optional)**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.

**Non-operating

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1. General Description

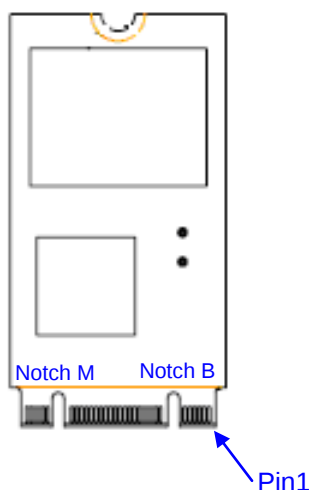
Apacer P100-M is the next generation modularized Solid State Drive (SSD) with the shape of all new M.2 form factor, with the aim to be the more suitable for mobile and compact computers with standard width at only 22.00 mm. P100-M appears in M.2 2242 mechanical dimensions and is believed to be the leading add-in storage solution for future host computing systems.

The M.2 SSD is designed with SATA-based connector pinouts, providing full compliance with the latest SATA Revision 3.2 interface specifications. Aside from SATA compliance, P100-M delivers exceptional performance and power efficiency. On the other hand, the extreme thin and light form factor makes P100-M the ideal choice for mobile computing systems, which appears to be the trend in near future.

Regarding reliability, P100-M is built with a powerful SATA controller that supports on-the-module ECC as well as efficient wear leveling scheme. Since it is operating under SATA 6.0 Gbps interface, P100-M is provided with Apacer latest S.M.A.R.T. that are primarily oriented for the latest SATA interface SSD, for drive lifetime monitoring and analyzing.

2. Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into both Key B and Key M connectors.



Pin	Type	Description
1	CONFIG_3	Ground (according to M.2 configurations for SSD-SATA definition)
2	3.3V	Supply Pin, 3.3V
3	GND	Ground
4	3.3V	Supply pin, 3.3V
5	No connect	No connect
6	Not available	No connect (used for other purposes)
7	Not available	No connect (used for other purposes)
8	Not available	No connect (used for other purposes)

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9	No connect	No connect
10	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
11	No connect	No connect (used for other purposes)
12	(removed for key)	Mechanical notch B
13	(removed for key)	Mechanical notch B
14	(removed for key)	Mechanical notch B
15	(removed for key)	Mechanical notch B
16	(removed for key)	Mechanical notch B
17	(removed for key)	Mechanical notch B
18	(removed for key)	Mechanical notch B
19	(removed for key)	Mechanical notch B
20	Not available	No connect (used for other purposes)
21	CONFIG_0	Ground (according to M.2 configurations for SSD-SATA definition)
22	Not available	No connect (used for other purposes)
23	Not available	No connect (used for other purposes)
24	Not available	No connect (used for other purposes)
25	Not available	No connect (used for other purposes)
26	Not available	No connect (used for other purposes)
27	GND	Ground
28	Not available	No connect (used for other purposes)
29	PERn1	Not used
30	Not available	No connect (used for other purposes)
31	PERp1	Not used
32	Not available	No connect (used for other purposes)
33	GND	Ground
34	Not available	No connect (used for other purposes)
35	PETn1	Not used
36	Not available	No connect (used for other purposes)
37	PETp1	Not used
38	DEVSLP	Device Sleep, input. If driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	Not available	No connect (used for other purposes)
41	SATA-Rx+	Host receiver differential signal pair
42	Not available	No connect (used for other purposes)
43	SATA-Rx-	Host receiver differential signal pair
44	Not available	No connect (used for other purposes)

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45	GND	Ground
46	Not available	No connect (used for other purposes)
47	SATA-Tx-	Host transmitter differential pair
48	Not available	No connect (used for other purposes)
49	SATA-Tx+	Host transmitter differential pair
50	PERST#	Not used
51	GND	Ground
52	CLKREQ#	Not used
53	REFCLKN	Not used
54	PEWAKE#	Not used
55	REFCLKP	Not used
56	MFG1	Manufacturing pin. Use determined by vendor (no connect on a host)
57	GND	Ground
58	MFG2	Manufacturing pin. Use determined by vendor (no connect on a host)
59	(removed for key)	Mechanical notch M
60	(removed for key)	Mechanical notch M
61	(removed for key)	Mechanical notch M
62	(removed for key)	Mechanical notch M
63	(removed for key)	Mechanical notch M
64	(removed for key)	Mechanical notch M
65	(removed for key)	Mechanical notch M
66	(removed for key)	Mechanical notch M
67	Not available	No connect (used for other purposes)
68	SUSCLK	Not used
69	CONFIG_1	Ground
70	3.3V	Supply pin, 3.3V
71	GND	Ground
72	3.3V	Supply pin, 3.3V
73	GND	Ground
74	3.3V	Supply pin, 3.3V
75	CONFIG_2	Ground

3. Product Specifications

3.1 Capacity

Capacity specification of P100-M is available as shown in Table 3-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 3-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
8 GB	8,012,390,400	15,525	16	63	15,649,200
16 GB	16,013,942,784	16,383	16	63	31,277,232
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

3.2 Performance

Performances of P100-M are listed below in Table 3-2.

Table 3-2 Performance

Capacity \ Performance	8 GB	16 GB	32 GB	64 GB	128 GB	256 GB
Sustained read (MB/s)	120	215	230	405	450	440
Sustained write (MB/s)	85	150	130	160	165	160

Note: Results may differ from various flash configurations or host system setting

3.3 Environmental Specifications

Environmental specification of P100-M series follows MIL-STD-810, as shown in Table 3-3.

Table 3-3 P100-M Environmental Specifications

Item	Specifications
Temperature	0°C to 70°C (Operating)
	-40°C to 85°C (Extended)
	-40°C to 85°C (in storage)
Humidity	RH 90% under 40°C (Operating) RH 95% under 55°C (Extended)
Shock	1500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	80cm free fall, 6 face of each
Bending	≥ 20N, hold 1min/5times
Torque	0.5N-m or 5deg, hold 5min/5times
ESD	24°C, RH 49%

3.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in P100-M. The prediction result for P100-M is more than 2,000,000 hours.

Notes about the MTBF:

The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

3.5 Certification and Compliance

P100-M complies with the following standards:

- CE
- FCC
- RoHS Recast
- MIL-STD-810
- BSMI

4. Flash Management

4.1 Error Correction/Detection

P100-M implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 72 bits error in 1K bytes.

4.2 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

4.3 Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Apacer provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

4.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

4.5 ATA Secure Erase

ATA Secure Erase is a standard ATA command and will write all “0xFF” to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

4.6 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

4.7 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 μ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption $\leq$ 5 mW; host assertion time $\leq$ 10 ms; exit timeout from this state $\leq$ 20 ms (unless specified otherwise in SATA Identify Device Log).

Note:

1. The behaviors of power management features would depend on host/device settings.
2. Device Sleep mode is optional, depending on product ordering selections.

4.8 Endurance

The endurance of a storage device is predicted by Tera Bytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Capacity	Tera Bytes Written
8 GB	7
16 GB	14
32 GB	28
64 GB	57
128 GB	114
256 GB	228

Notes:

- The measurement follows the standard metric: 1 TB (Terabyte) = 1,000 GB.
- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- The estimated values are based on JEDEC Enterprise endurance workload comprised of random data with the payload size distribution with sequential write behavior.

5. Software Interface

5.1 Command Set

This section defines the software requirements and the format of the commands the host sends to P100-M. Commands are issued to P100-M by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 5-1 Command Set

Command	Code	Command	Code
NOP	00h	Idle	97h
Data Set Management	06h	Check Power Mode	98h
Recalibrate	10h-1Fh	Sleep	99h
Read Sectors	20h	SMART	B0h
Read Sectors without Retry	21h	Device Configuration	B1h
Read Sectors EXT	24h	Read Multiple	C4h
Read DMA EXT	25h	Write Multiple	C5h
Read Native Max Address EXT	27h	Set Multiple Mode	C6h
Read Multiple EXT	29h	Read DMA	C8h
Read Log EXT	2Fh	Read DMA without Retry	C9h
Write Sectors	30h	Write DMA	CAh
Write Sectors Without Retry	31h	Write DMA without Retry	CBh
Write Sectors EXT	34h	Write Multiple FUA EXT	CEh
Write DMA EXT	35h	Standby Immediate	E0h
Set Native Max Address EXT	37h	Idle Immediate	E1h
CFA Write Sectors without erase	38h	Standby	E2h
Write Multiple EXT	39h	Idle	E3h
Write DMA FUA EXT	3Dh	Read Buffer	E4h
Write Long EXT	3Fh	Check Power Mode	E5h
Read Verify Sectors	40h	Sleep	E6h
Read Verify Sectors without Retry	41h	Flush Cache	E7h
Read Verify Sectors EXT	42h	Write Buffer	E8h
Write Uncorrectable EXT	45h	Flush Cache EXT	EAh
Read FPDMA Queued	60h	Identify Device	ECh
Write FPDMA Queued	61h	Set Features	EFh
Seek	70h-7Fh	Security Set Password	F1h
Execute Device Diagnostic	90h	Security Unlock	F2h
Initialize Device Parameters	91h	Security Erase Prepare	F3h

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Download Microcode	92h	Security Erase Unit	F4h
Download Microcode DMA	93h	Security Freeze Lock	F5h
Standby Immediate	94h	Security Disable Password	F6h
Idle Immediate	95h	Read Native Max Address	F8h
Standby	96h	Set Max Address	F9h

5.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

6. Electrical Specification

Table 6-1 Operating Range

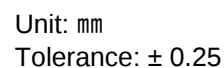
Supply Voltage	3.3V $\pm$ 5% (3.135-3.465V)
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Table 6-2 Power Consumption (typical)

Capacity Modes	8 GB	16 GB	32 GB	64 GB	128 GB	256 GB
Active (mA)	300	300	315	360	455	450
Idle (mA)	85	85	85	95	95	95

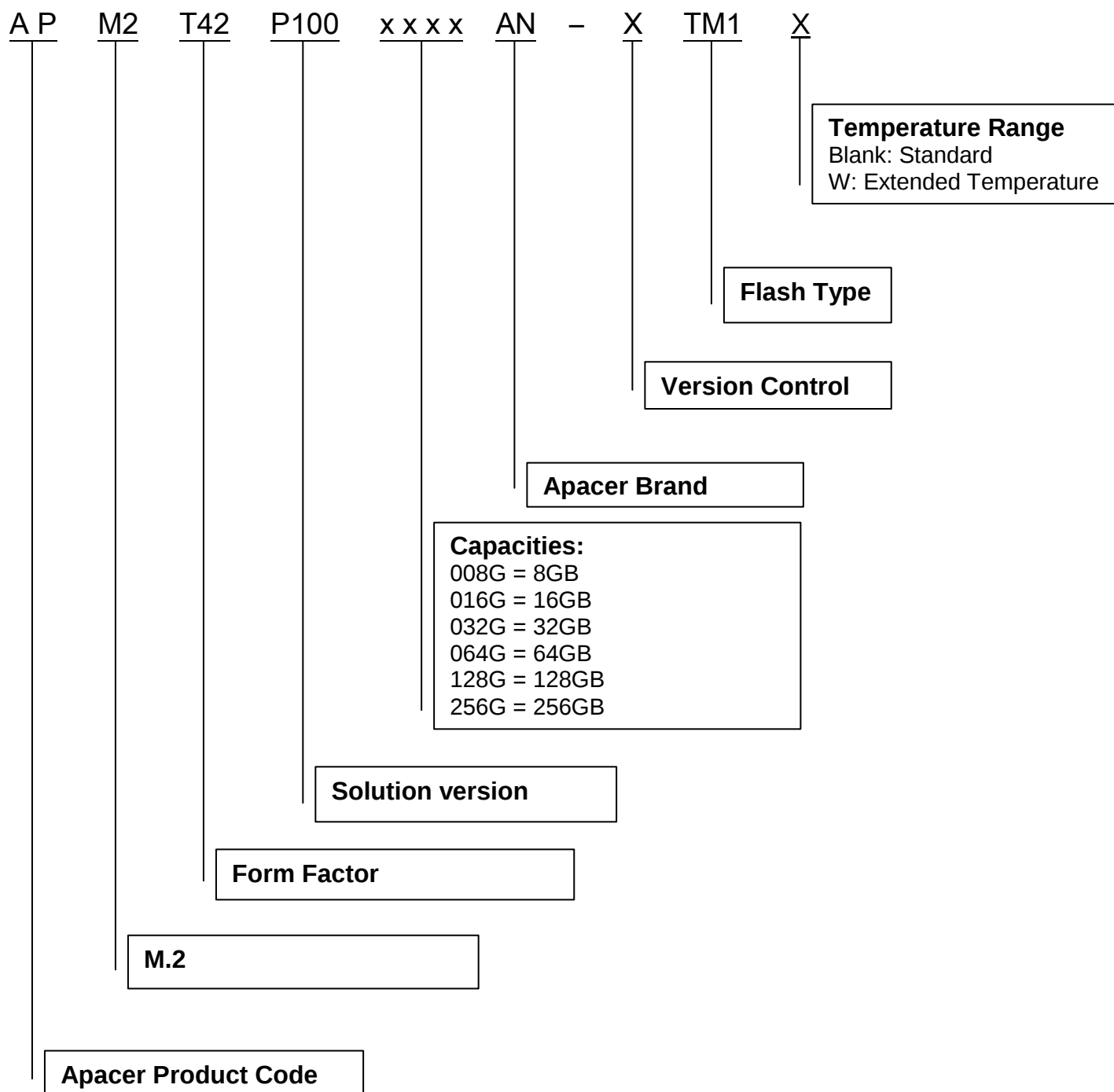
Note: Results may differ from various flash configurations or host system setting.

Dimension: 42mm(L) x 22mm(W) x 3.65mm(H)



8. Product Ordering Information

8.1 Product Code Designations



8.2 Valid Combinations

8.2.1 Standard Temperature

Capacity	No DEVSLP	DEVSLP
8GB	APM2T42P100008GAN-GTM1	APM2T42P100008GAN-HTM1
16GB	APM2T42P100016GAN-GTM1	APM2T42P100016GAN-HTM1
32GB	APM2T42P100032GAN-GTM1	APM2T42P100032GAN-HTM1
64GB	APM2T42P100064GAN-GTM1	-
128GB	APM2T42P100128GAN-GTM1	-
256GB	APM2T42P100256GAN-GTM1	-

8.2.2 Extended Temperature

Capacity	No DEVSLP	DEVSLP
8GB	APM2T42P100008GAN-GTM1W	APM2T42P100008GAN-HTM1W
16GB	APM2T42P100016GAN-GTM1W	APM2T42P100016GAN-HTM1W
32GB	APM2T42P100032GAN-GTM1W	APM2T42P100032GAN-HTM1W
64GB	APM2T42P100064GAN-GTM1W	-
128GB	APM2T42P100128GAN-GTM1W	-
256GB	APM2T42P100256GAN-GTM1W	-

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Date	Description	Remark
1.0	10/22/2015	Official release	
1.1	1/20/2016	Removed 64GB model with DEVSLP support	

Global Presence

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