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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

September 2015

FDN5632N_F085

N-Channel Logic Level PowerTrench® MOSFET

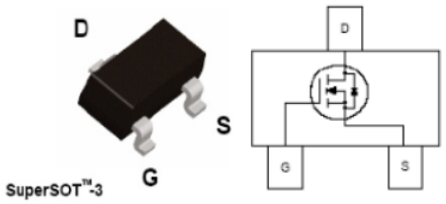
60 V, 1.6 A, 98 mΩ

Features

- $R_{DS(on)}$ = 98 mΩ at V_{GS} = 4.5 V, I_D = 1.6 A
- $R_{DS(on)}$ = 82 mΩ at V_{GS} = 10 V, I_D = 1.7 A
- Typ $Q_{g(TOT)}$ = 9.2 nC at V_{GS} = 10 V
- Low Miller Charge
- UIS Capability
- Qualified to AEC Q101
- RoHS Compliant

Applications

- DC/DC converter
- Motor Drives



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (V_{GS} = 10V)	1.7	A
	Pulsed	10	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	74	mJ
P_D	Power Dissipation	1.1	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	75	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in² copper pad area	111	°C/W

Note:

1: E_{AS} of 74mJ is 100% test at L=80mH, I_{AS}=1.4A, starting T_J = 25 °C

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
5632	FDN5632N_F085	SSOT3	7”	8mm	3000 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 48V, V_{GS} = 0V, T_A = 125°C	-	-	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1	2.0	3	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 1.7A, V_{GS}= 10V	-	57	82	mΩ
		I_D = 1.6A, V_{GS}= 6V	-	62	88	mΩ
		I_D = 1.6A, V_{GS}= 4.5V		70	98	mΩ
		I_D = 1.7A, V_{GS}= 10V, T_A = 150°C	-	107	135	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	475	-	pF
C_{oss}	Output Capacitance		-	60	-	pF
C_{rss}	Reverse Transfer Capacitance		-	30	-	pF
R_G	Gate Resistance	f = 1MHz	-	1.4	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V, V_{DD} = 20V, I_D = 1.7A	-	9.2	12	nC
Q_{gs}	Gate to Source Gate Charge		-	1.5	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	1.4	-	nC

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Switching Characteristics						
t_{on}	Turn-On Time	V_{DD} = 30V, I_D = 1.0A, V_{GS} = 10V, R_{GEN} = 6Ω	-	-	30	ns
$t_{d(on)}$	Turn-On Delay Time		-	15	-	ns
t_r	Rise Time		-	1.7	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	5.2	-	ns
t_f	Fall Time		-	1.3	-	ns
t_{off}	Turn-Off Time		-	-	12.9	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 1.7A	-	0.8	1.25	V
		I_{SD} = 0.85A	-	0.8	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 1.7A, dI_{SD}/dt = 100A/μs	-	16.0	21	ns
Q_{rr}	Reverse Recovery Charge		-	7.9	10.3	nC

Typical Characteristics

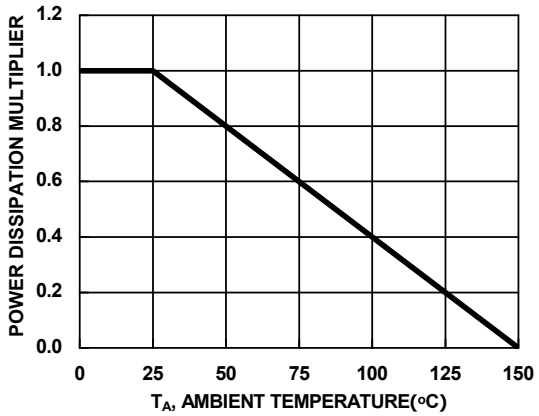


Figure 1. Normalized Power Dissipation vs. Case Temperature

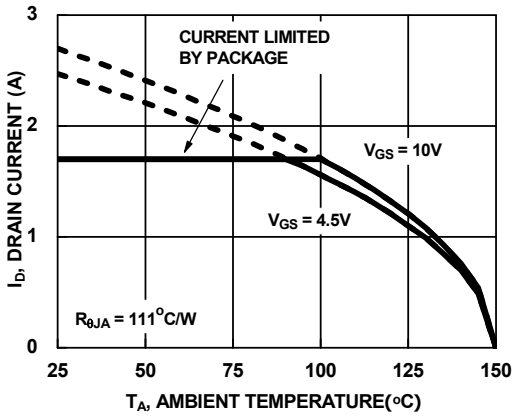


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

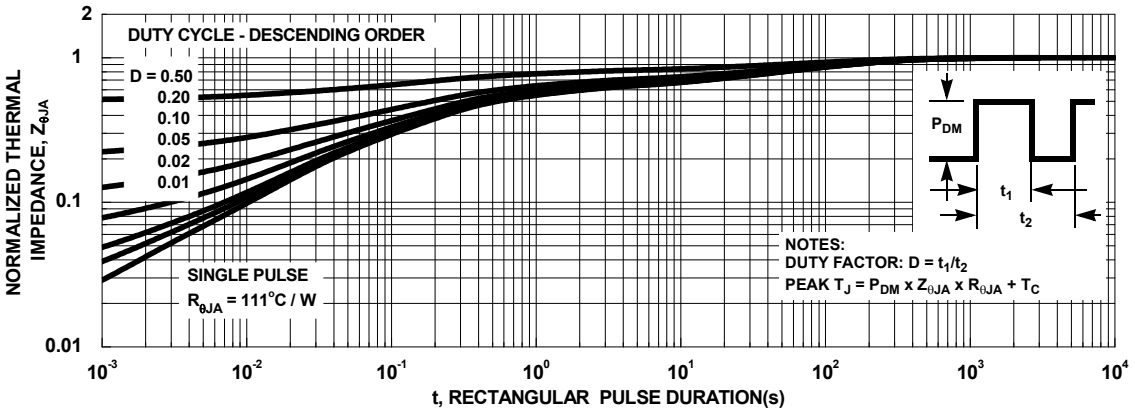


Figure 3. Normalized Maximum Transient Thermal Impedance

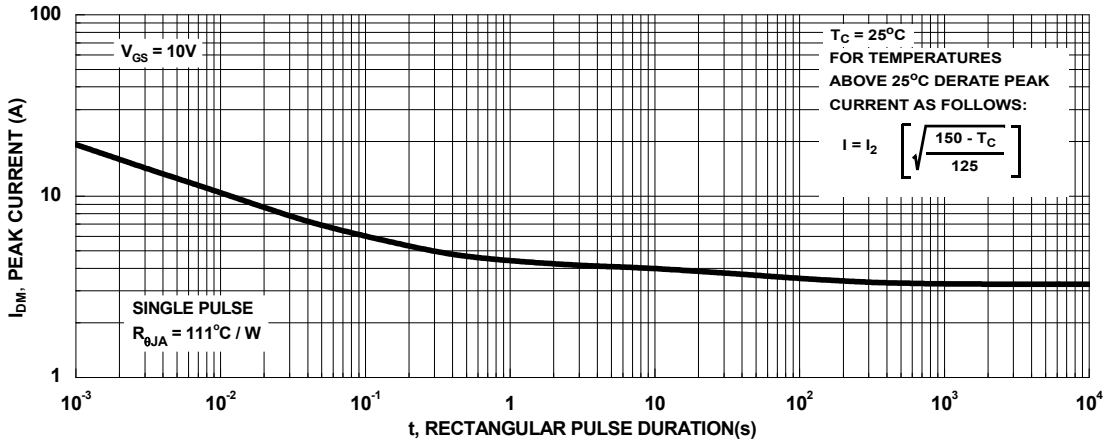


Figure 4. Peak Current Capability

Typical Characteristics

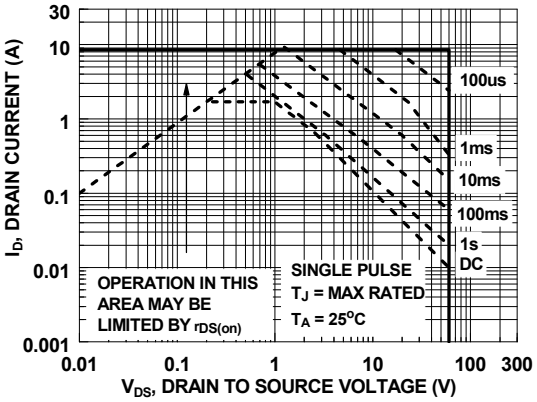


Figure 5. Forward Bias Safe Operating Area

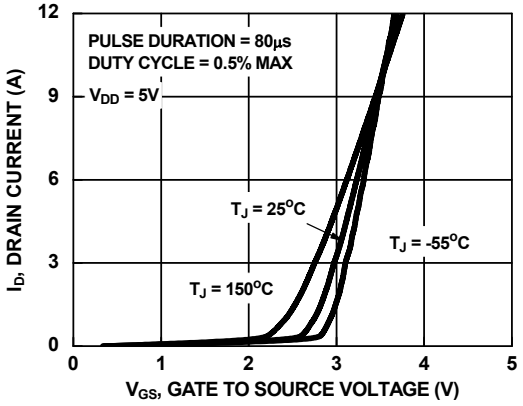


Figure 6. Transfer Characteristics

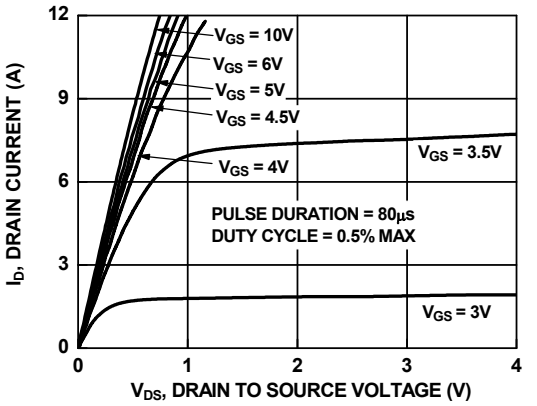


Figure 7. Saturation Characteristics

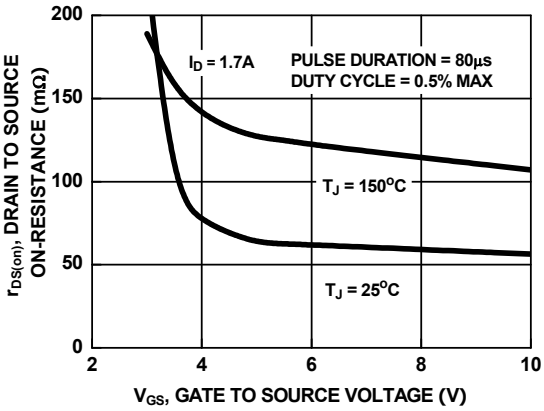


Figure 8. Drain to Source On-Resistance Variation vs Gate to Source Voltage

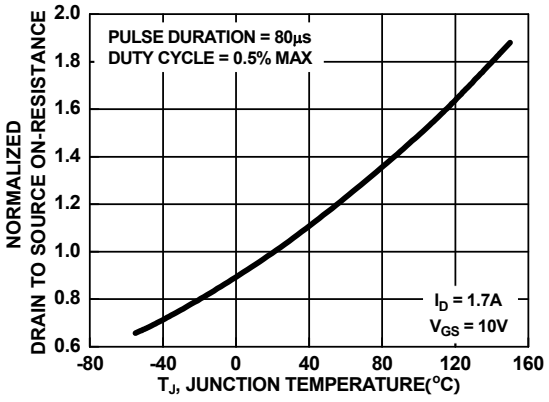


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

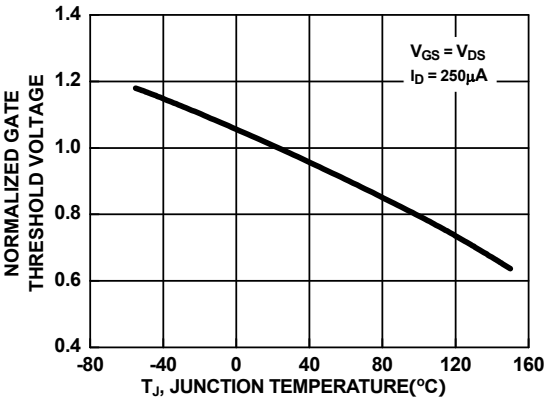


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics

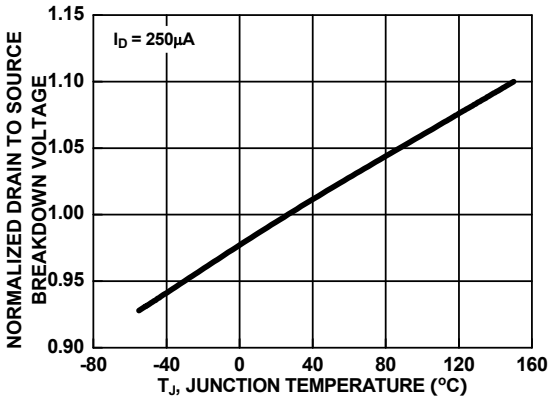


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

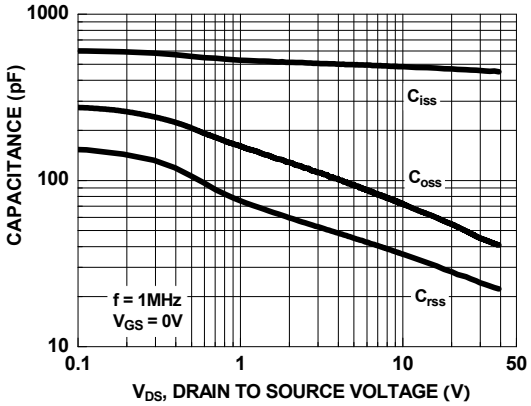


Figure 12. Capacitance vs Drain to Source Voltage

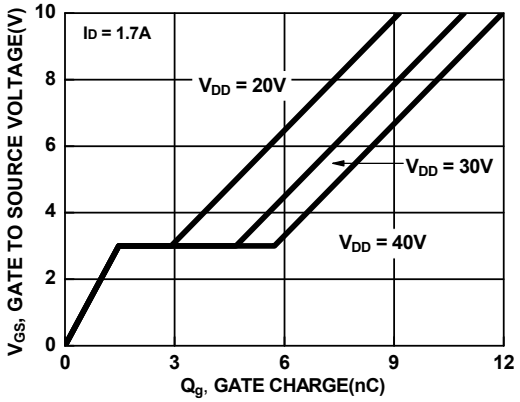
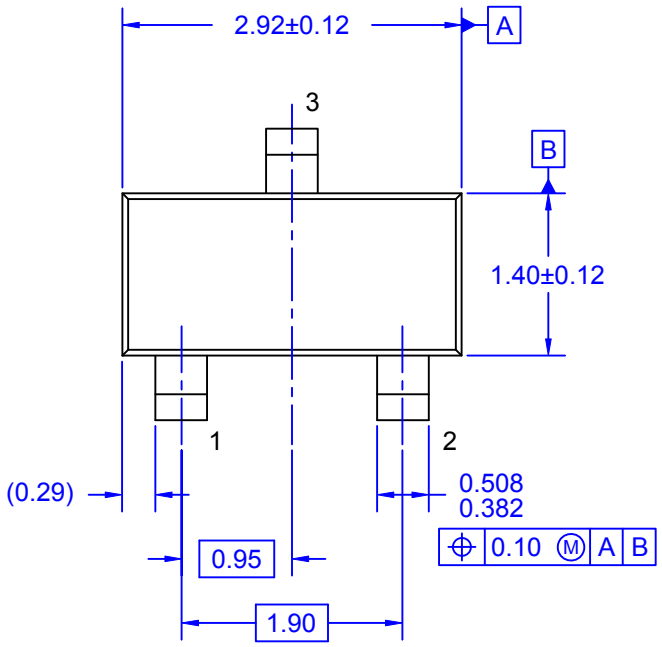
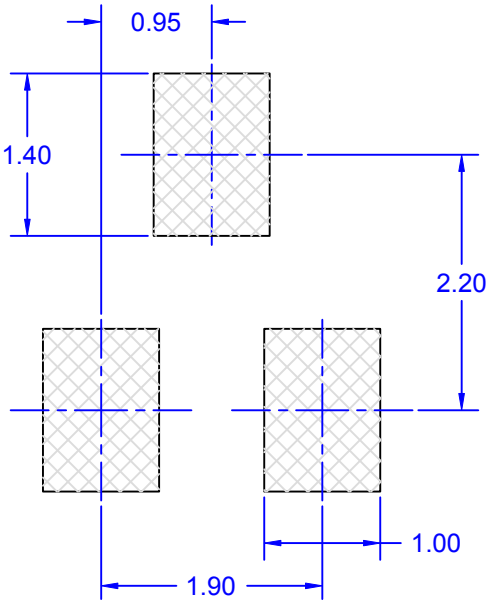
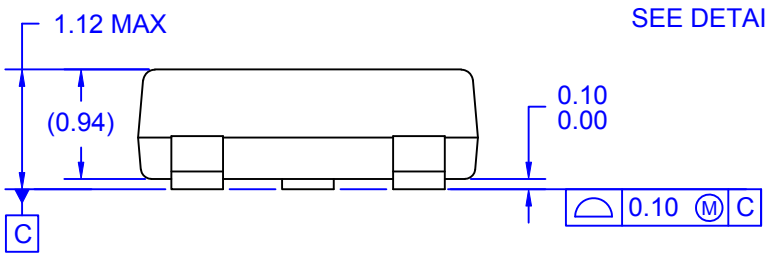


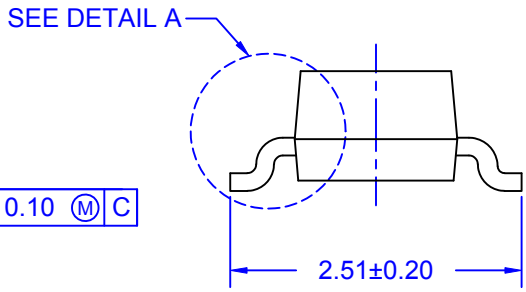
Figure 13. Gate Charge vs Gate to Source Voltage

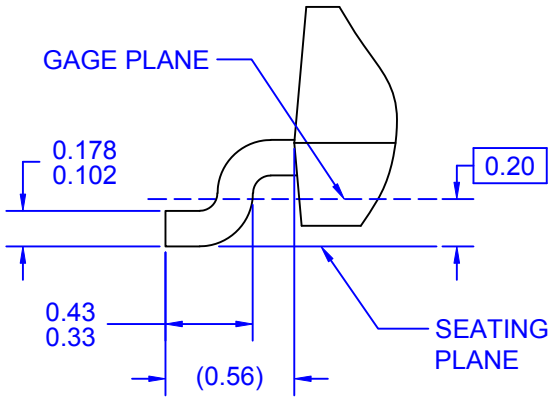




LAND PATTERN RECOMMENDATION







DETAIL A

SCALE: 50:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) NO JEDEC REFERENCE AS OF AUGUST 2003
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
E) DRAWING FILE NAME: MKT-MA03BREV3

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