41 dB Range, 1 dB Step Size, Programmable Dual VGA

Data Sheet

AD8372

FEATURES

- Dual independent digitally controlled VGA
- Differential input and output
  - 150 Ω differential input
  - Open-collector differential output
- 7.8 dB noise figure to 100 MHz @ maximum gain
- HD2/HD3 better than 77 dBc for 1 V p-p differential output
- −3 dB bandwidth of 130 MHz
- 41 dB gain range
- 1 dB step size ± 0.2 dB
- Serial 8-bit bidirectional SPI control interface
- Wide input dynamic range
- Pin-programmable output stage
- Power-down feature
- Single 5 V supply: 106 mA per channel
- 32-lead LFCSP, 5 mm × 5 mm package

APPLICATIONS

- Differential ADC drivers
- CMTS upstream direct sampling receivers
- CATV modem signal scaling
- Generic RF/IF gain stages
- Single-ended-to-differential conversion

FUNCTIONAL BLOCK DIAGRAM

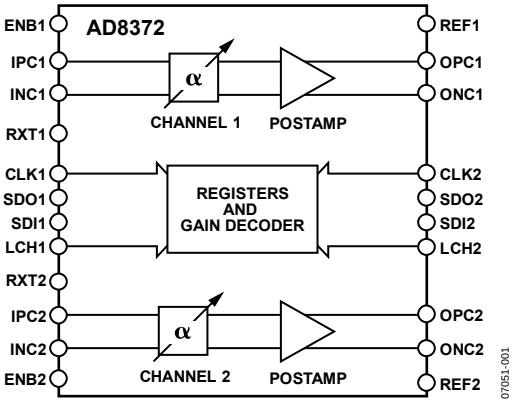

Figure 1.

GENERAL DESCRIPTION

The AD8372 is a dual, digitally controlled, variable gain amplifier (VGA) that provides precise gain control, high IP3, and low noise figure. The excellent distortion performance and moderate signal bandwidth make the AD8372 a suitable gain control device for a variety of multichannel receiver applications.

For wide input dynamic range applications, the AD8372 provides a broad 41 dB gain range. The gain is programmed through a bidirectional 4-pin serial interface. The serial interface consists of a clock, latch, data input, and data output lines for each channel.

The AD8372 provides the ability to set the transconductance of the output stage using a single external resistor. The RXT1 and RXT2 pins provide a band gap derived stable reference voltage of 1.56 V. Typically 2.0 kΩ shunt resistors to ground are used to set the maximum gain to a nominal value of 31 dB. The current setting resistors can be adjusted to manipulate the gain and distortion performance of each channel. This is a flexible feature in applications where it is desirable to trade off distortion performance for lower power consumption.

The AD8372 is powered on by applying the appropriate logic level to the ENB1, ENB2 pins. When powered down, the AD8372 consumes less than 2.6 mA and offers excellent input-to-output isolation. The gain setting is preserved when powered down.

Fabricated on an Analog Devices, Inc., high frequency BiCMOS process, the AD8372 provides precise gain adjustment capabilities with good distortion performance. The quiescent current of the AD8372 is typically 106 mA per channel. The AD8372 amplifier comes in a compact, thermally enhanced 5 mm × 5 mm 32-lead LFCSP package and operates over the temperature range of −40°C to +85°C.

Rev. C

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5/2008—Rev. 0 to Rev. A

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11/2007—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T = 25°C, Z_S = 150 Ω, Z_L = 250 Ω at 35 MHz, 1 V p-p differential output, RXT1 = RXT2 = 2.0 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 1 V p-p, C_{LOAD} < 3pF		130		MHz
INPUT STAGE	Pin IPC1, Pin INC1, Pin IPC2, and Pin INC2				
Maximum Input Swing at Each Input Pin			5		V p-p
Input Resistance	Differential		150		Ω
Common-Mode Input Voltage			2.4		V
CMRR	Gain code = 1x101010 (max gain)		55		dB
GAIN					
Maximum Voltage Gain	Gain code = 1x101010		32		dB
Minimum Voltage Gain	Gain code = 1x000001		−9		dB
Gain Step Size	From gain code 1x000001 to 1x101010		1.0		dB
Gain Step Accuracy	From gain code 1x000001 to 1x101010		±0.3		dB
Gain Flatness	Gain code = 1x101010, from 5 MHz to 65MHz		0.7		dB
Gain Temperature Sensitivity	Gain code = 1x101010		7.5		mdB/°C
Step Response	For 6 dB gain step, 10% settling		20		ns
OUTPUT STAGE	Pin OPC1, Pin ONC1, Pin OPC2, and Pin ONC2				
Output Voltage Swing	At P1dB, gain code = 1x101010		9		V p-p
Output Resistance	Differential		3.5		kΩ
Channel Isolation	Measured at differential output for differential input applied to alternate channel		55		dB
NOISE/HARMONIC PERFORMANCE					
5 MHz	Gain code = 1x101010 (max gain)				
Noise Figure			7.8		dB
Second Harmonic			79		dBc
Third Harmonic			91		dBc
Output IP3			32		dBm
Output 1 dB Compression Point			18.2		dBm
35 MHz	Gain code = 1x101010 (max gain)				
Noise Figure			7.8		dB
Second Harmonic			79		dBc
Third Harmonic			87		dBc
Output IP3			35		dBm
Output 1 dB Compression Point			18.1		dBm
65 MHz	Gain code = 1x101010 (max gain)				
Noise Figure			7.9		dB
Second Harmonic			78		dBc
Third Harmonic			85		dBc
Output IP3			35		dBm
Output 1 dB Compression Point			17.9		dBm
85 MHz	Gain code = 1x101010				
Noise Figure			8.1		dB
Second Harmonic			77		dBc
Third Harmonic			85		dBc
Output IP3			35		dBm
Output 1 dB Compression Point			17.7		dBm

Parameter	Conditions	Min	Typ	Max	Unit
POWER INTERFACE					
Supply Voltage		4.5		5.5	V
Quiescent Current per Channel	Thermal connection made to exposed paddle under device		106		mA
vs. Temperature	$-40°C \le T_A \le +85°C$			135	mA
Power-Down Current, Both Channels	ENB1 and ENB2 low		1.2		mA
vs. Temperature	$-40°C \le T_A \le +85°C$			1.3	mA
ENABLE INTERFACE	Pin ENB1 and Pin ENB2				
Enable Threshold	Minimum voltage to enable the device			0.8	V
ENB1, ENB2 Input Bias Current	ENB1, ENB2 = 0 V		400		nA
GAIN CONTROL INTERFACE	Pin CLK1, Pin CLK2, Pin SDI1, Pin SDI2, Pin SDO1, Pin SDO2, Pin LCH1, and Pin LCH2				
V_{IH}	Minimum voltage for a logic high	2.4			V
Input Bias Current			400		nA
Serial Port Output Feedthrough	Worse-case feedthrough from CLK1, CLK2, SDI1, SDI2, SDO1, SDO2, LCH1, LCH2 to OPC1 and ONC2, or OPC2 and ONC2		−60		dB

Table 2. Gain Code vs. Voltage Gain Look-Up Table

8-Bit Binary Gain Code[1]	Voltage Gain (dB)
RW DC 000000	< −60
RW DC 000001	−9
RW DC 000010	−8
RW DC 000011	−7
RW DC 000100	−6
RW DC 000101	−5
RW DC 000110	−4
RW DC 000111	−3
RW DC 001000	−2
RW DC 001001	−1
RW DC 001010	0
RW DC 001011	+1
RW DC 001100	+2
RW DC 001101	+3
RW DC 001110	+4
RW DC 001111	+5
RW DC 010000	+6
RW DC 010001	+7
RW DC 010010	+8
RW DC 010011	+9
RW DC 010100	+10
RW DC 010101	+11
RW DC 010110	+12
RW DC 010111	+13
RW DC 011000	+14
RW DC 011001	+15
RW DC 011010	+16
RW DC 011011	+17
RW DC 011100	+18
RW DC 011101	+19
RW DC 011110	+20
RW DC 011111	+21
RW DC 100000	+22
RW DC 100001	+23
RW DC 100010	+24
RW DC 100011	+25
RW DC 100100	+26
RW DC 100101	+27
RW DC 100110	+28
RW DC 100111	+29
RW DC 101000	+30
RW DC 101001	+31
RW DC 101010	+32
RW DC 101011	< −60

[1] RW is the read/write bit. RW = 0 for read mode; RW = 1 for write mode. DC is the don't care bit.

SERIAL CONTROL INTERFACE TIMING

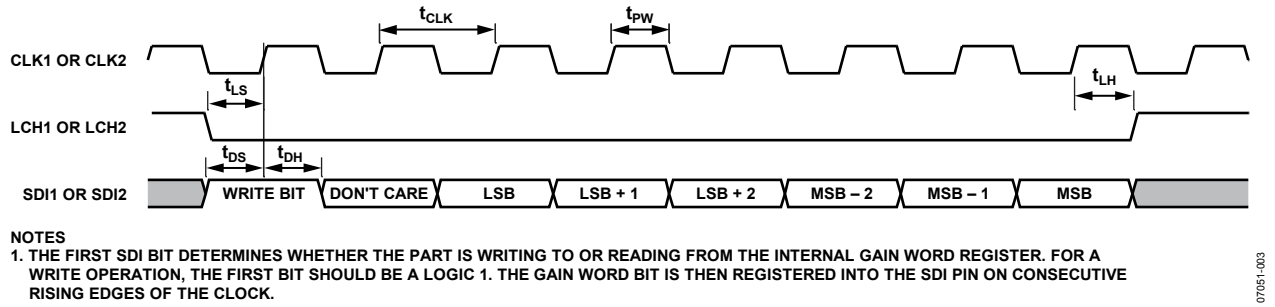

Figure 2. Write Mode Timing Diagram

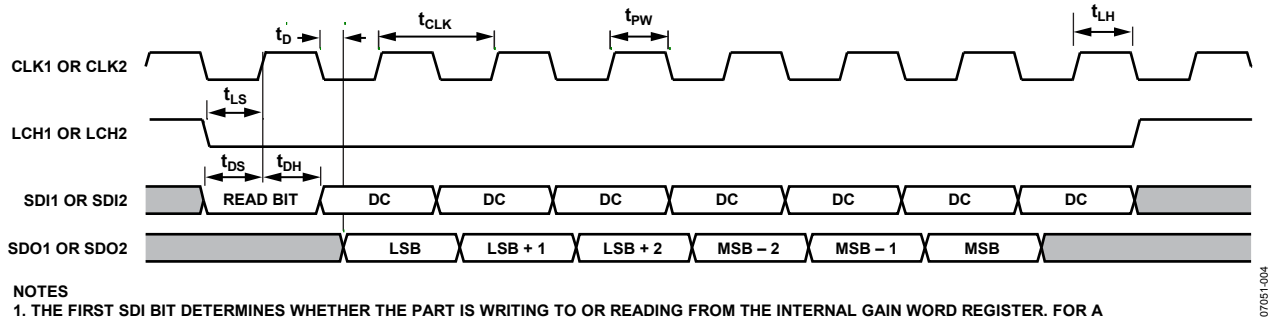

Figure 3. Read Mode Timing Diagram

Table 3. Serial Programming Timing Parameters

Parameter	Min	Unit
Clock Pulse Width (t_{PW})	10	ns
Clock Period (t_{CK})	20	ns
Write Mode		
Setup Time Data vs. Clock (t_{DS})	0.0	ns
Hold Time Data vs. Clock (t_{DH})	1.6	ns
Setup Time Latch vs. Clock (t_{LS})	−1.8	ns
Hold Time Latch vs. Clock (t_{LH})	2.0	ns
Read Mode		
Clock to Data Out (t_D)	4.5	ns

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, V_S	5.5 V
ENB1, ENB2, SDI1, SDI2, SDO1, SDO2, CLK1, CLK2, LCH1, LCH2	DGDx − 0.5 V to V_S + 500 mV
Input Voltage, V_{IPC1}, V_{INC1}, V_{IPC2}, V_{INC2}	AGDx − 0.5 V to V_S + 500 mV
Internal Power Dissipation	1.4 W
θ_{JA} (Exposed Paddle Soldered Down)	34.6°C/W[1, 2]
θ_{JC} (At Exposed Paddle)	3.6°C/W[2]
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Still air.
[2] All values are modeled using a standard 4-layer JEDEC test board with the pad soldered to the board and thermal vias in the board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

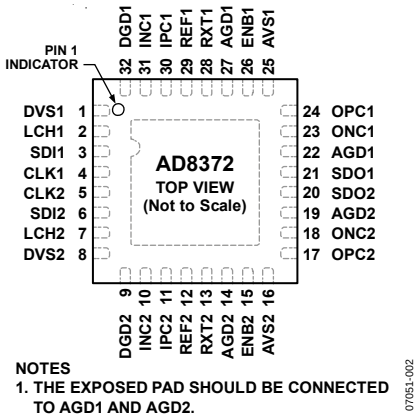

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DVS1	Digital Supply Pin for Channel 1
2	LCH1	Latch Input for Channel 1
3	SDI1	Serial Data Input for Channel 1
4	CLK1	Clock Input for Channel 1
5	CLK2	Clock Input for Channel 2
6	SDI2	Serial Data Input for Channel 2
7	LCH2	Serial Data Input for Channel 2 Latch Input for Channel 2
8	DVS2	Digital Supply Pin for Channel 2
9	DGD2	Digital Ground for Channel 2
10	INC2	Negative Input for Channel 2
11	IPC2	Positive Input for Channel 2
12	REF2	Reference Voltage for Channel 2
13	RXT2	External Bias Setting Resistor Connection for Channel 2
14	AGD2	Analog Ground for Channel 2
15	ENB2	Chip Enable Pin for Channel 2
16	AVS2	Analog Supply Pin for Channel 2
17	OPC2	Positive Output for Channel 2
18	ONC2	Negative Output for Channel 2
19	AGD2	Analog Ground for Channel 2
20	SDO2	Serial Data Output for Channel 2
21	SDO1	Serial Data Output for Channel 1
22	AGD1	Analog Ground for Channel 1
23	ONC1	Negative Output for Channel 1
24	OPC1	Positive Output for Channel 1
25	AVS1	Analog Supply Pin for Channel 1
26	ENB1	Chip Enable Pin for Channel 1
27	AGD1	Analog Ground for Channel 1
28	RXT1	External Bias Setting Resistor Connection for Channel 1
29	REF1	Reference Voltage for Channel 1
30	IPC1	Positive Input for Channel 1
31	INC1	Negative Input for Channel 1
32	DGD1	Digital Ground for Channel 1
	EPAD	Exposed Pad. The exposed pad should be connected to AGD1 and AGD2.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, Z_S = 150 Ω, Z_L = 250 Ω, 1 V p-p differential output, both channels enabled, unless otherwise noted.

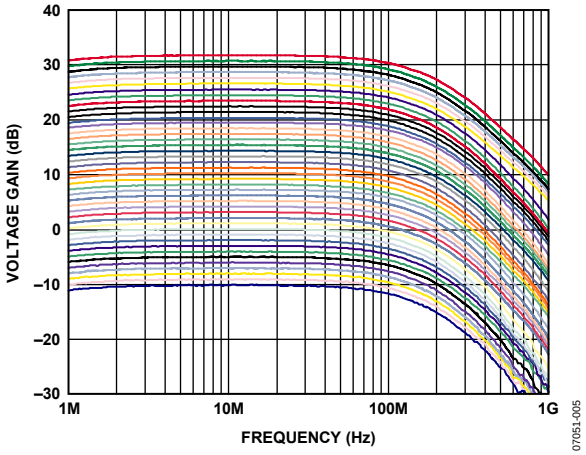

Figure 5. Gain vs. Frequency by Gain Code (All Codes), Differential In, Differential Out

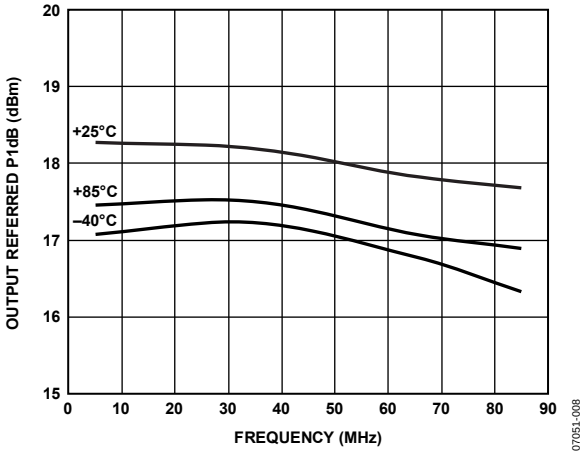

Figure 8. P1dB, Maximum Gain

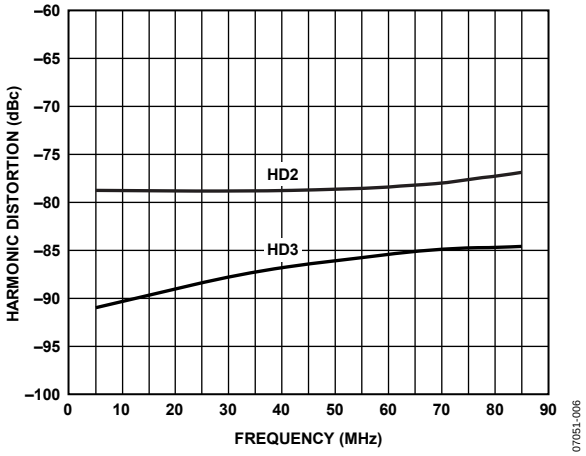

Figure 6. 2nd and 3rd Harmonic Distortion

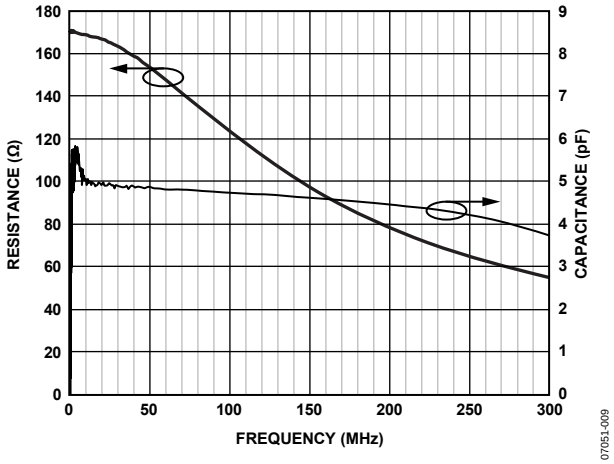

Figure 9. Input Equivalent Parallel Impedance

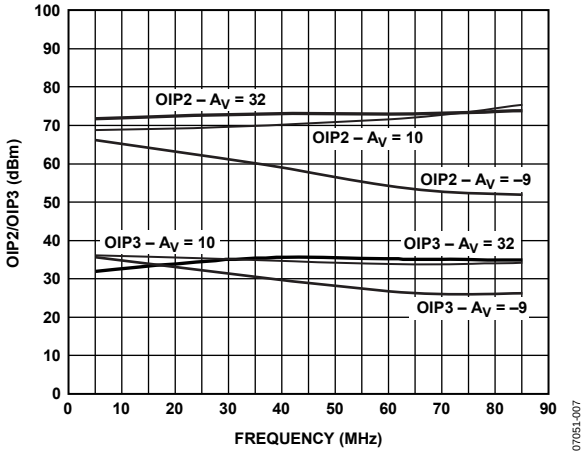

Figure 7. OIP2 and OIP3

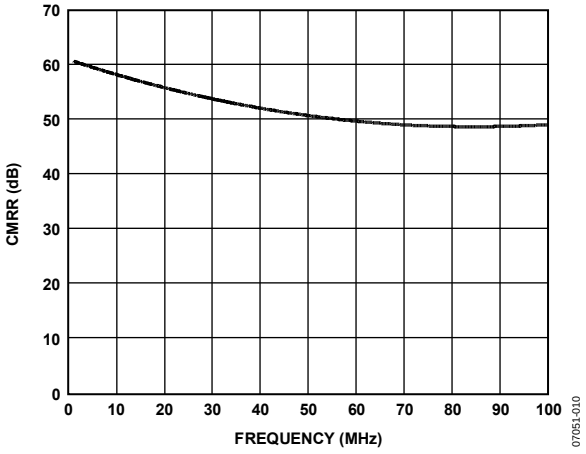

Figure 10. CMRR vs. Frequency

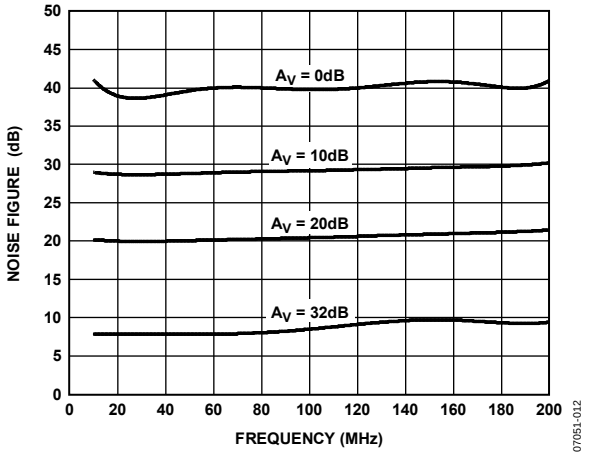

Figure 11. Noise Figure vs. Frequency

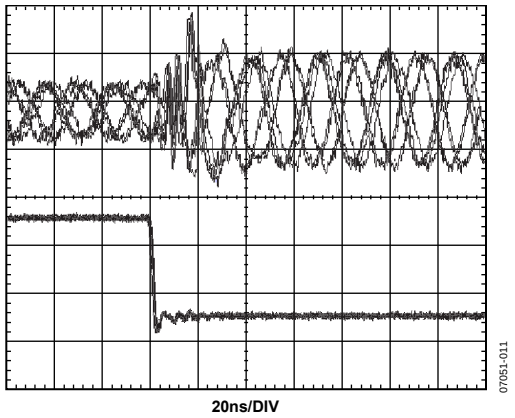

Figure 13. AD8372 Response to 6 dB Step Change in Gain (Gain Register Setting 36 to Setting 42); Falling Edge Shown is Serial Clock Input Edge

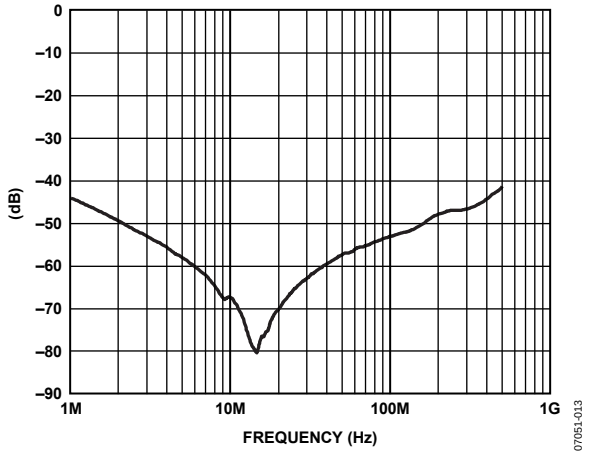

Figure 12. Isolation, Input to Opposite Output at Maximum Gain (To calculate output to output gain, subtract 29 dB from this plot)

THEORY OF OPERATION

The AD8372 is a dual differential variable gain amplifier. Each amplifier consists of a 150 Ω digitally controlled 6 dB attenuator followed by a 1 dB vernier and a fixed gain transconductance amplifier.

The differential output on each amplifier consists of a pair of open-collector transistors. It is recommended that each open-collector output be biased to +5 V with a high value inductor. A 33 µH inductor, such as the Coilcraft® 1812LS-333XJL, is an excellent choice for this component. A 250 Ω resistor should be placed across the differential outputs to provide a current-to-voltage conversion and as a source impedance for passive filtering, post AD8372.

The gain for each side is based on a 250 Ω differential load and varies as the R_{LOAD} changes per the following equations:

$$Gain = 20\log(R_{LOAD}/250), \text{ for voltage gain}$$

$$Gain = 10\log(R_{LOAD}/250), \text{ for power gain}$$

The dependency of the gain on the load is due to the open-collector output stage that is biased using external chokes. The inductance of the chokes and the resistance of the load determine the low frequency pole of the amplifier. The high frequency pole is set by the parasitic capacitance of the chokes and outputs in parallel with the output resistance.

The total supply current of 106 mA per side consists of 70 mA for the combined outputs and about 36 mA through the power supply pins. Each side has an external resistor (R_{EXT}) to ground to set the transconductance of the output stage. For optimum distortion, 106 mA total current per side is recommended, making the R_{EXT} value about 2.0 kΩ. Each side has a 2.4 V reference pin and that same common-mode voltage appears on the inputs. This reference should be decoupled using a 0.1 µF capacitor. The part can be powered down to less than 2.6 mA by setting the ENB pin low for the appropriate side.

The noise figure of the AD8372 is 7.8 dB at maximum gain and increases as the gain is reduced. The increase in noise figure is equal to the reduction in gain.

The linearity of the part measured at the output is first-order independent of the gain setting.

Layout considerations should include minimizing capacitance on the outputs by avoiding ground planes under the chokes, and equalizing the output line lengths for phase balance.

SINGLE-ENDED AND DIFFERENTIAL SIGNALS

The AD8372 is designed to be used by applying differential signals to the inputs and using the differential output drive of the device to drive the next device in the signal chain. The excellent distortion performance of the AD8372 is due primarily to the use of differential signaling techniques to cancel various distortion components in the device. In addition, all ac characterization is done using differential signal paths. Using this device with either the input or the output in a single-ended circuit significantly degrades the overall performance of the AD8372.

PASSIVE FILTER TECHNIQUES

The AD8372 has a 100 Ω differential input impedance. For optimal performance, the differential output load should be 250 Ω. When designing passive filters around the AD8372, these impedances must be taken into account.

DIGITAL GAIN CONTROL

The digital gain control interface consists of the following pins: SDI, SDO, CLK, and LATCH. The interface is active when the LATCH pin is shifted low. Gain words are written into the AD8372 via the SDI pin, and read back from the SDO pin. The first bit clocked into the data input pin determines whether the interface is in write or read mode. The second bit is a don't care bit, while the remaining six bits program the gain. In read mode, the SDO pin clocks out the 6-bit gain word, LSB to MSB. The gain can be programmed between −9 dB and 32 dB in 1 dB steps. Timing details are given in Figure 2 and Figure 3. The gain code is given in Table 2.

DRIVING ANALOG-TO-DIGITAL CONVERTERS

The AD8372 is designed with the intention of driving high speed, high dynamic range ADCs. The circuit in Figure 14 represents a simplified front end of one-half of the AD8372 dual VGA driving an AD9445 14-bit, 125 MHz analog-to-digital converter (ADC). The input of the AD8372 is driven differentially using a 1:3 impedance ratio transformer, which also matches the 150 Ω input resistance to a 50 Ω source. The open-collector outputs are biased through the 33 µH inductors and are ac-coupled from the 142 Ω load resistors that, in parallel with the 2 kΩ input resistance of the ADC, provide a 250 Ω load for gain accuracy.

The ADC is ac-coupled from the 142 Ω resistors to negate a dc effect on the input common-mode voltage of the AD9445. Including the series 33 Ω resistors improves the isolation of the AD8372 from the switching currents caused by the ADC input sample and hold. The AD9445 represents a 2 kΩ differential load and requires a 2 V p-p signal when VREF = 1 V for a full-scale output. This circuit provides variable gain, isolation, and source matching for the AD9445. Using this circuit with the AD8372 in a gain of 32 dB (maximum gain), an SFDR performance of 74.5 dBc is achieved at 85 MHz (see Figure 15).

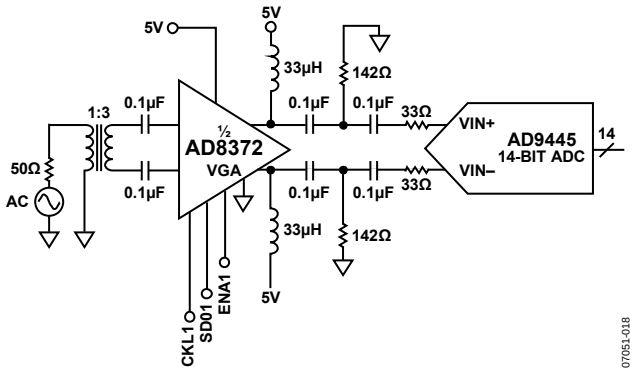

Figure 14. AD8372 Driving an AD9445 ADC

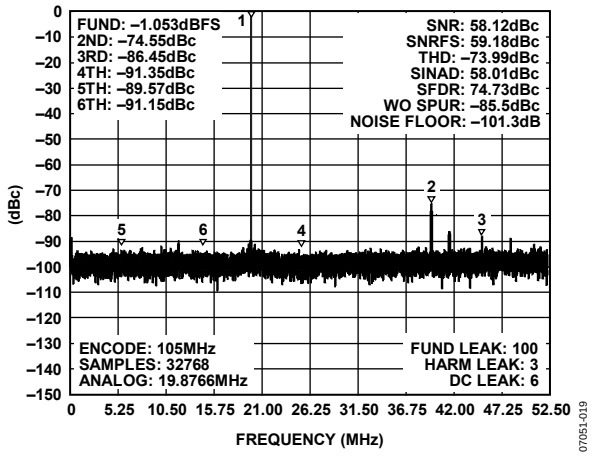

Figure 15. 74.5 dBc SFDR Performance of the AD8372 Driving the AD9445 ADC

EVALUATION BOARD SCHEMATIC

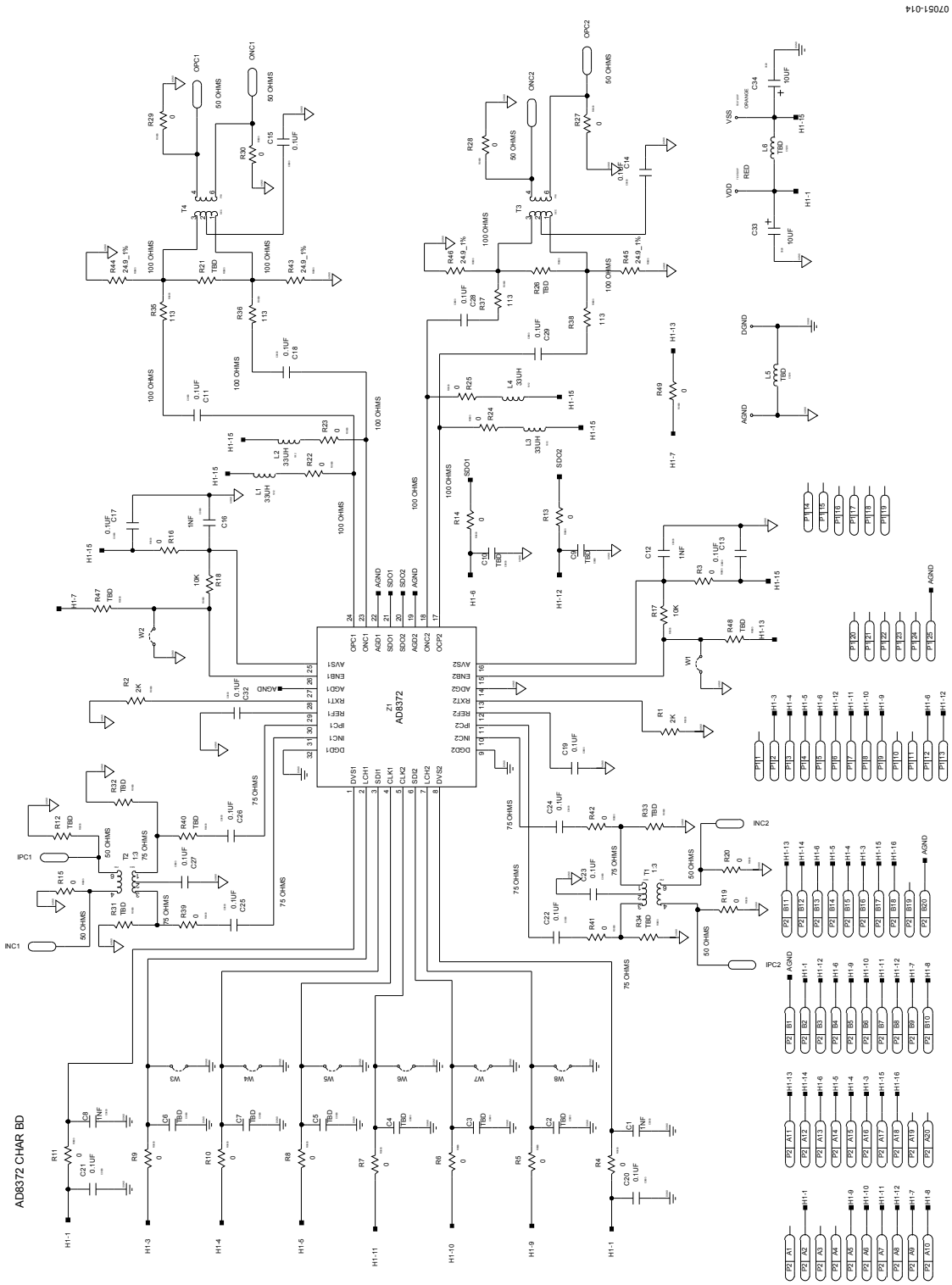

Figure 16. AD8372 Evaluation Board Schematic

OUTLINE DIMENSIONS

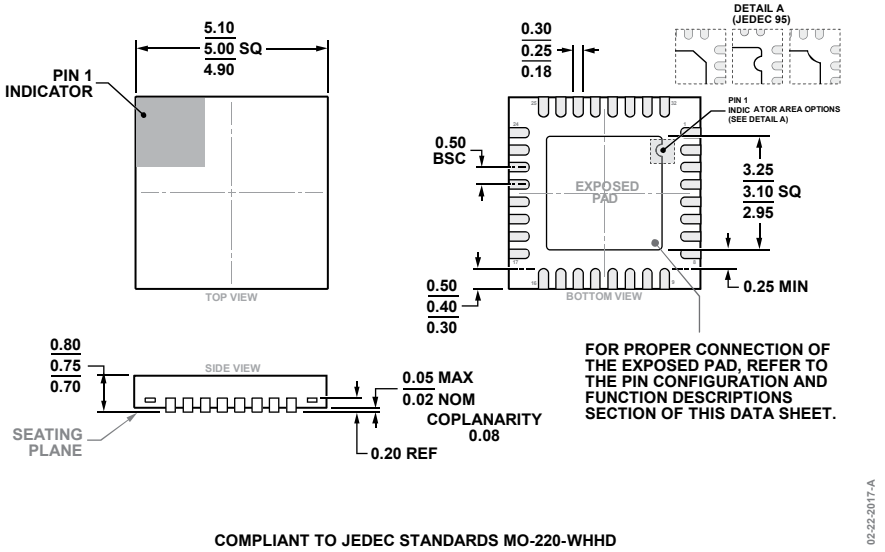

Figure 17. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8372ACPZ-WP	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP], Waffle Pack	CP-32-7	36
AD8372ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP], 7″ Tape and Reel	CP-32-7	1,500
AD8372-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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