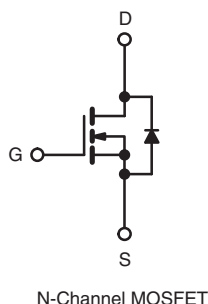
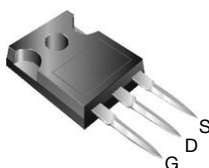


## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.60
$Q_g$ (Max.) (nC)	84	
$Q_{gs}$ (nC)	18	
$Q_{gd}$ (nC)	36	
Configuration	Single	

TO-247AC



### FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V  $V_{GS}$  Rating
- Reduced  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$
- Isolated Central Mounting Hole
- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS\*  
COMPLIANT

### DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Power MOSFET technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because its isolated mounting hole.

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFPC50LCPbF SiHFPC50LC-E3
SnPb	IRFPC50LC SiHFPC50LC

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	44	
Linear Derating Factor		1.5	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	920	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	11	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	19	mJ
Maximum Power Dissipation	$P_D$	190	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	3.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25^\circ\text{C}$ ,  $L = 13$  mH,  $R_g = 25\ \Omega$ ,  $I_{AS} = 11$  A (see fig. 12).
- $I_{SD} \leq 11$  A,  $dI/dt \leq 100$  A/ $\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.65	

**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.59	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6.6 A <sup>b</sup>	-	-	0.60	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 6.6 A <sup>b</sup>		7.0	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	2300	-	pF
Output Capacitance	C <sub>oss</sub>			-	270	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	28	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A, V <sub>DS</sub> = 360 V, see fig. 6 and 13 <sup>b</sup>	-	-	84	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	18	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	36	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 11 A , R <sub>g</sub> = 6.2 Ω, R <sub>D</sub> = 30 Ω, see fig. 10 <sup>b</sup>		-	17	-	ns
Rise Time	t <sub>r</sub>			-	32	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	41	-	
Fall Time	t <sub>f</sub>			-	26	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	11	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	44	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 11 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.4	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 11 A, dI/dt = 100 A/μs <sup>b</sup>		-	590	890	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	4.5	6.8	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

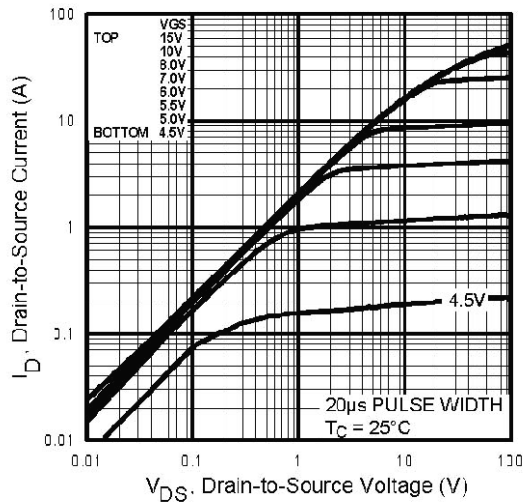


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

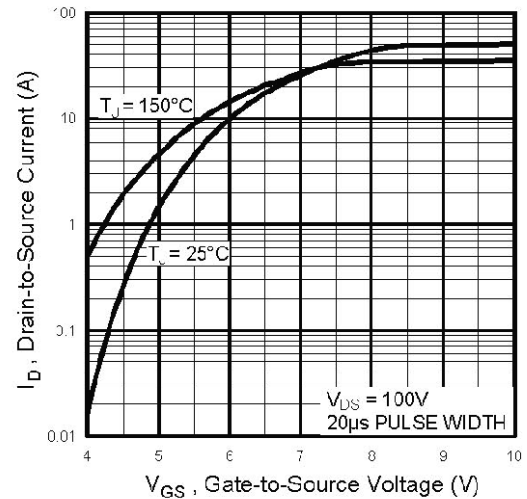


Fig. 3 - Typical Transfer Characteristics

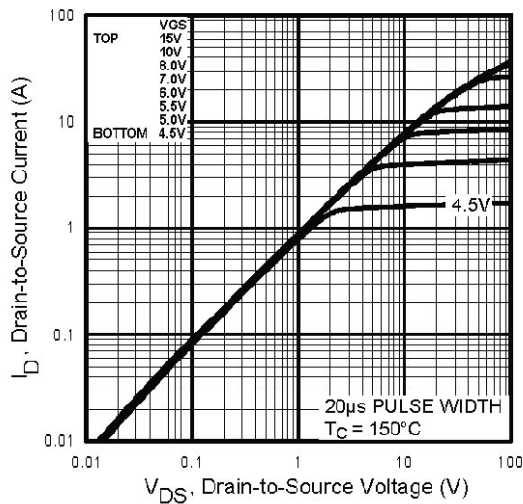


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

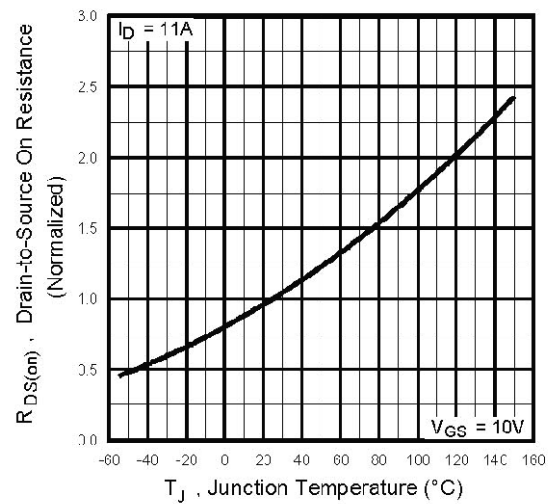
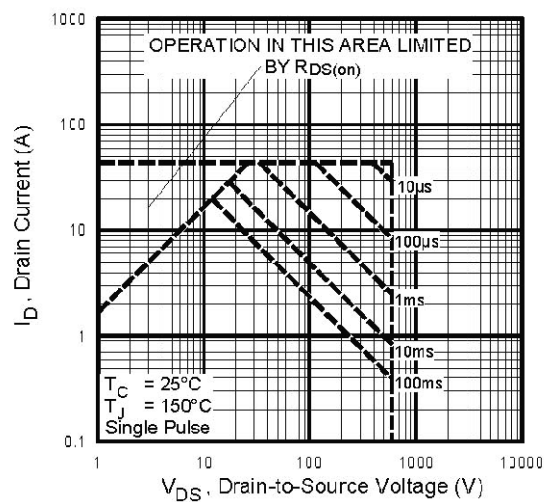
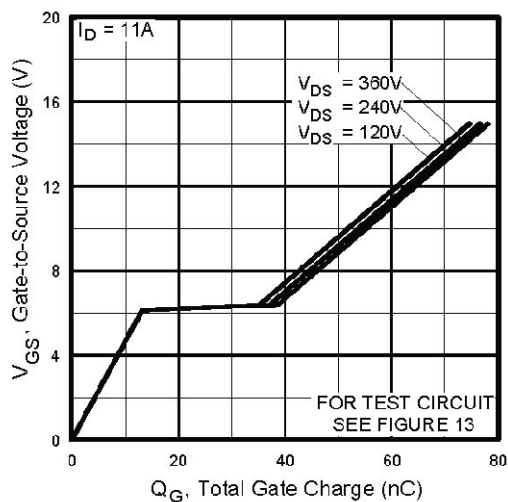
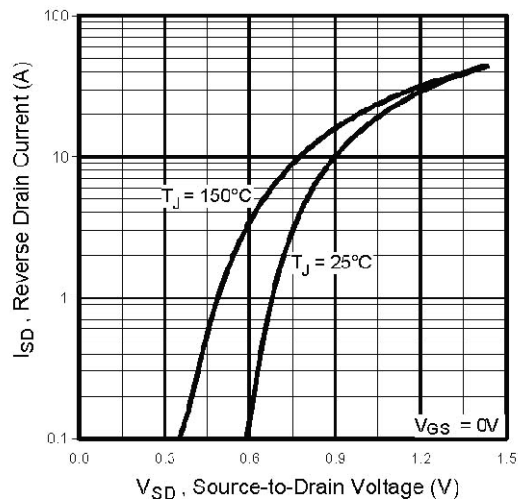
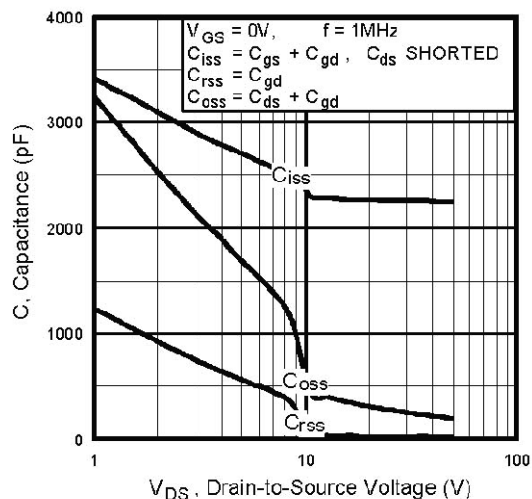


Fig. 4 - Normalized On-Resistance vs. Temperature



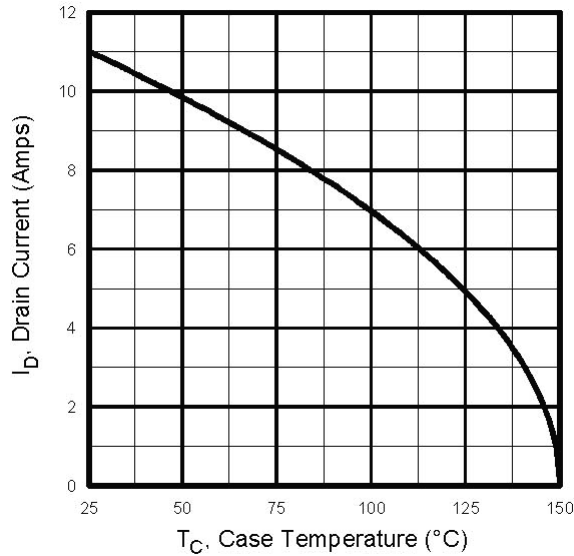


Fig. 9 - Maximum Drain Current vs. Case Temperature

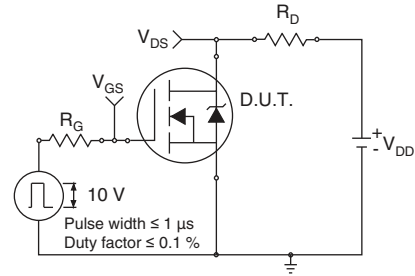


Fig. 10a - Switching Time Test Circuit

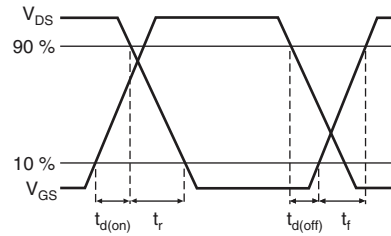


Fig. 10b - Switching Time Waveforms

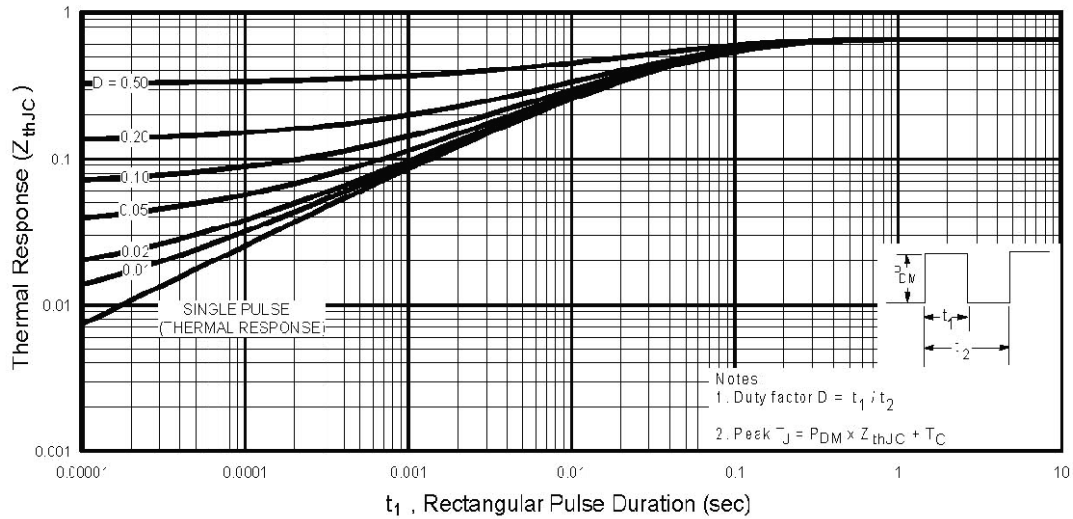


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

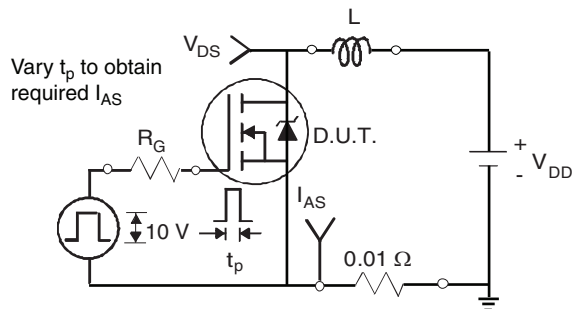


Fig. 12a - Unclamped Inductive Test Circuit

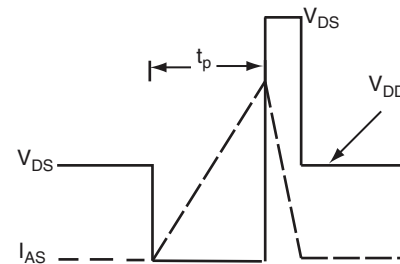


Fig. 12b - Unclamped Inductive Waveforms

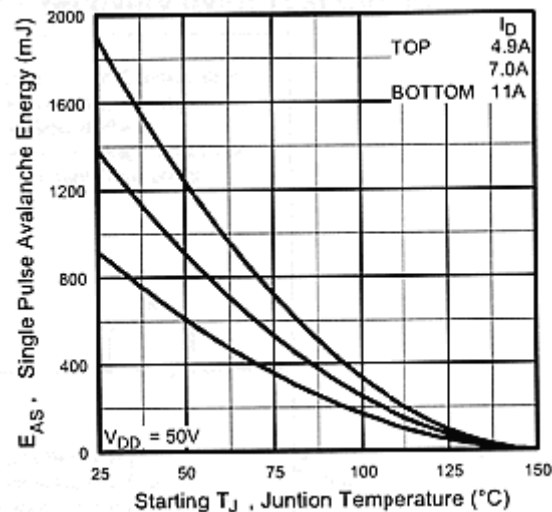


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

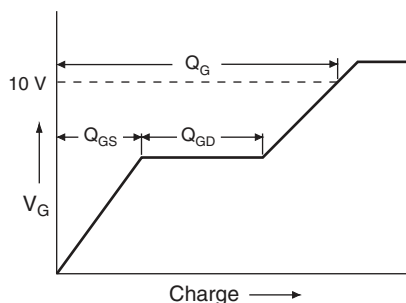


Fig. 13a - Basic Gate Charge Waveform

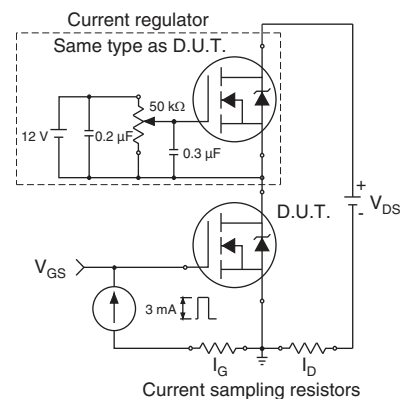
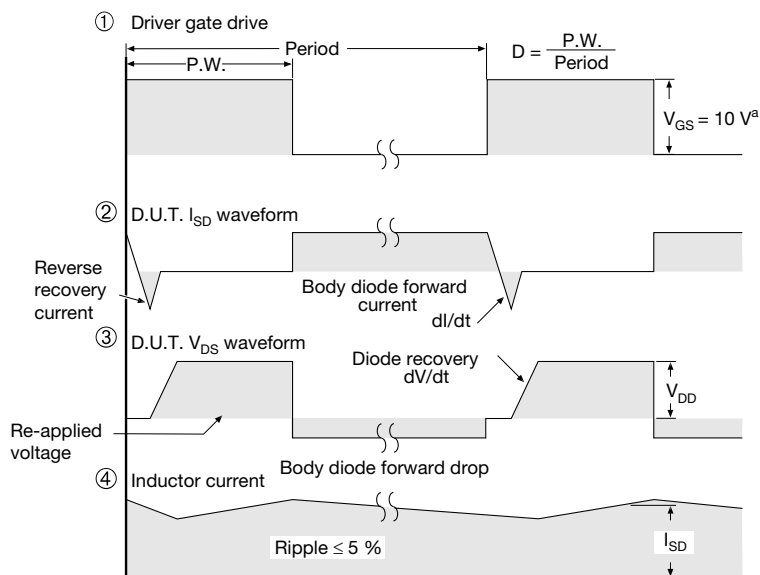
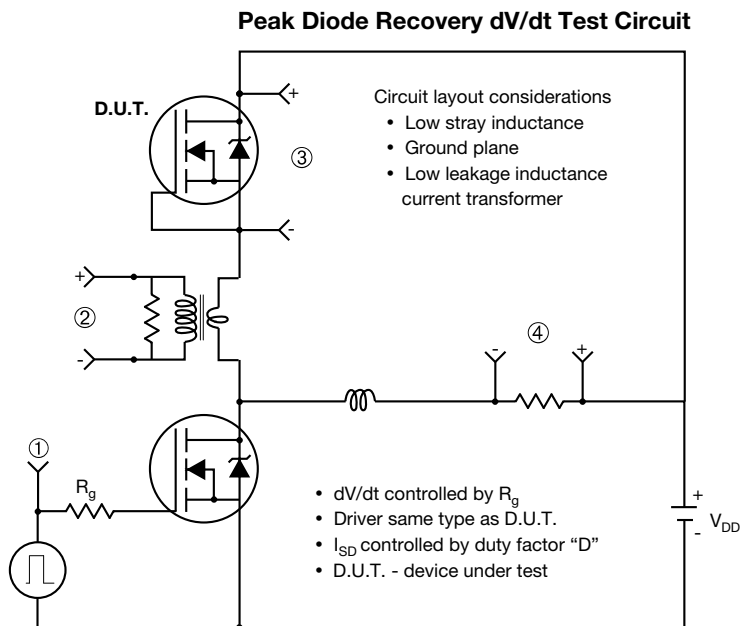


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5$  V for logic level devices

**Fig. 14 - For N-Channel**

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