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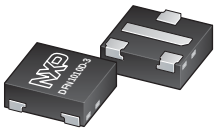


# PDTD113/123/143/114EQA series

## 50 V, 500 mA NPN resistor-equipped transistors

Rev. 1 — 4 February 2016 Product data sheet

## 1. Product profile

### 1.1 General description

NPN Resistor-Equipped Transistor (RET) family in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

**Table 1. Product overview**

| Type number | R1 | R2 | Package NXP | PNP complement |
|---|---|---|---|---|
| PDTD113EQA | 1 kΩ | 1 kΩ | DFN1010D-3 (SOT1215) | PDTB113EQA |
| PDTD123EQA | 2.2 kΩ | 2.2 kΩ | | PDTB123EQA |
| PDTD143EQA | 4.7 kΩ | 4.7 kΩ | | PDTB143EQA |
| PDTD114EQA | 10 kΩ | 10 kΩ | | PDTB114EQA |

### 1.2 Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- ± 10% resistor ratio tolerance
- Simplifies circuit design
- Reduces component count
- Reduced pick and place costs
- Low package height of 0.37 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint
- AEC-Q101 qualified

### 1.3 Applications

- Digital applications
- Cost saving alternative for BC807/BC817 series in digital applications
- Controlling IC inputs
- Switching loads

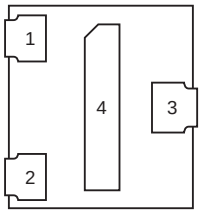
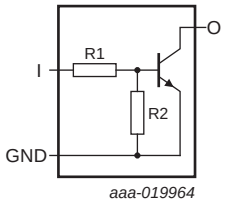
### 1.4 Quick reference data

**Table 2. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | 50 | V |
| $I_O$ | output current | | - | - | 500 | mA |

## 2. Pinning information

**Table 3. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | I | input (base) |   Transparent top view |   aaa-019964 |
| 2 | GND | GND (emitter) | | |
| 3 | O | output (collector) | | |
| 4 | O | output (collector) | | |

## 3. Ordering information

**Table 4. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PDTD113EQA | DFN1010D-3 | plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 × 1.0 × 0.37 mm | SOT1215 |
| PDTD123EQA | | | |
| PDTD143EQA | | | |
| PDTD114EQA | | | |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# 4. Marking

**Table 5. Marking codes**

| Type number | Marking code |
|---|---|
| PDTD113EQA | 01 00 11 |
| PDTD123EQA | 01 01 10 |
| PDTD143EQA | 01 10 01 |
| PDTD114EQA | 01 11 01 |

## 4.1 Binary marking code description

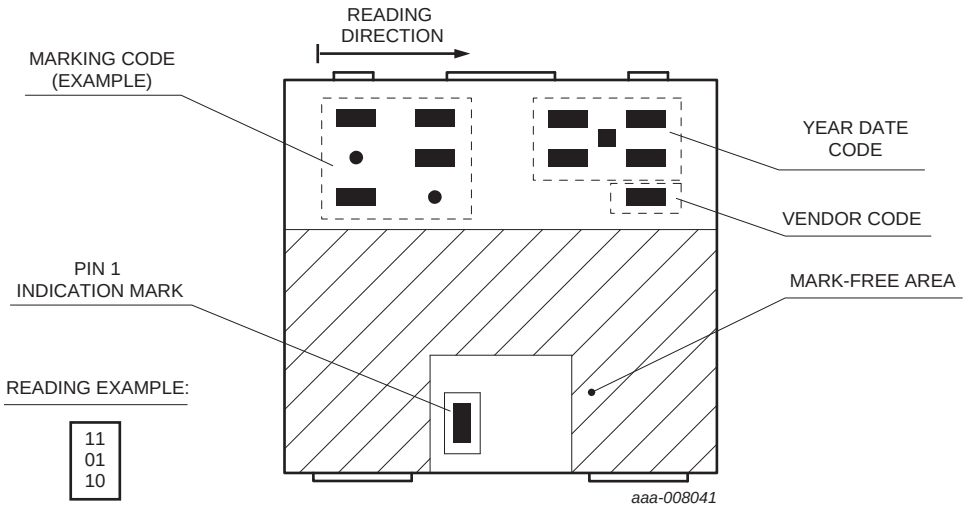


**Fig 1. SOT1215 binary marking code description**

# 5. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CBO}$ | collector-base voltage | open emitter | - | 50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | - | 50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | - | 10 | V |


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**Table 6. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

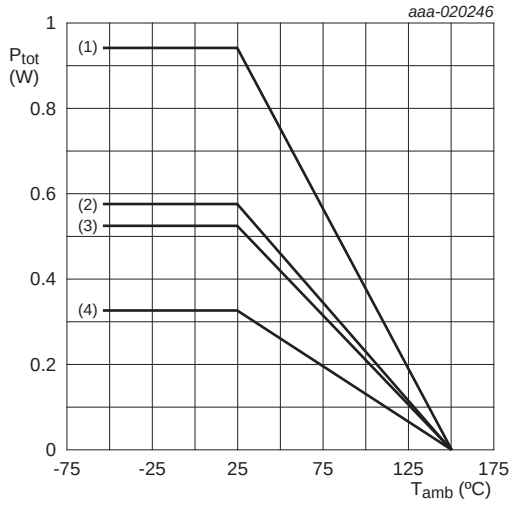
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_I$ | input voltage | | | | | |
| | PDTD113EQA | | | −10 | +10 | V |
| | PDTD123EQA | | | −10 | +12 | V |
| | PDTD143EQA | | | −10 | +30 | V |
| | PDTD114EQA | | | −10 | +50 | V |
| $I_O$ | output current | | | - | 500 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 325 | mW |
| | | | [2] | - | 575 | mW |
| | | | [3] | - | 525 | mW |
| | | | [4] | - | 940 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | −55 | +150 | °C |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated; mounting pad for collector 1 $cm^2$.

[3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 $cm^2$.




(1) FR4 PCB, 4-layer copper, 1 $cm^2$

(2) FR4 PCB, single-sided copper, 1 $cm^2$

(3) FR4 PCB, 4-layer copper, standard footprint

(4) FR4 PCB, single sided copper, standard footprint

**Fig 2. Power derating curves**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# 6. Thermal characteristics

**Table 7. Thermal characteristics**

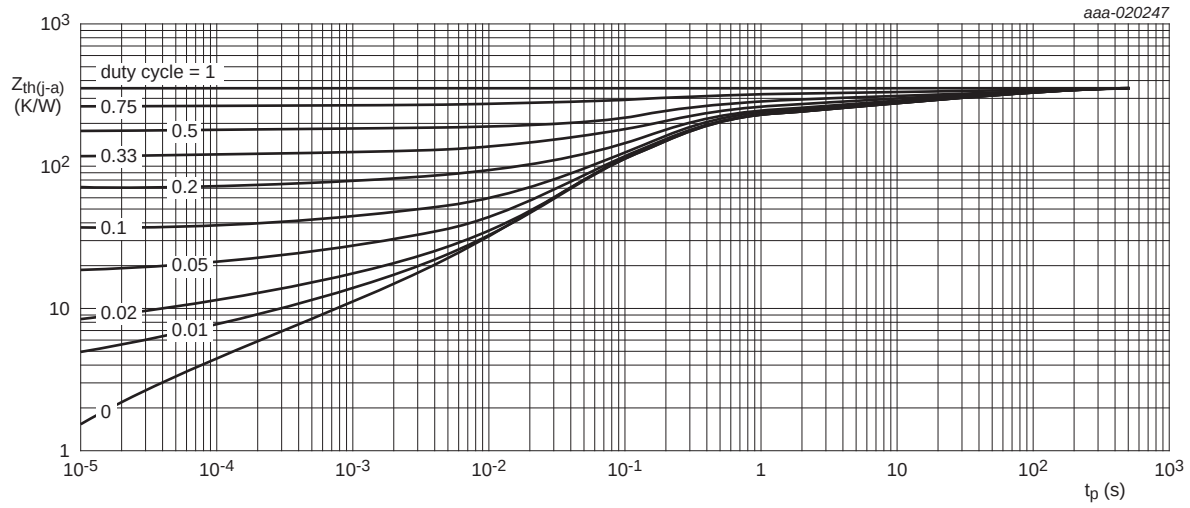
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 385 | K/W |
| | | | [2] | - | - | 218 | K/W |
| | | | [3] | - | - | 239 | K/W |
| | | | [4] | - | - | 133 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | - | 40 | K/W |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated; mounting pad for collector 1 $cm^2$.

[3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 $cm^2$.




FR4 PCB, single-sided copper, tin-plated and standard footprint

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**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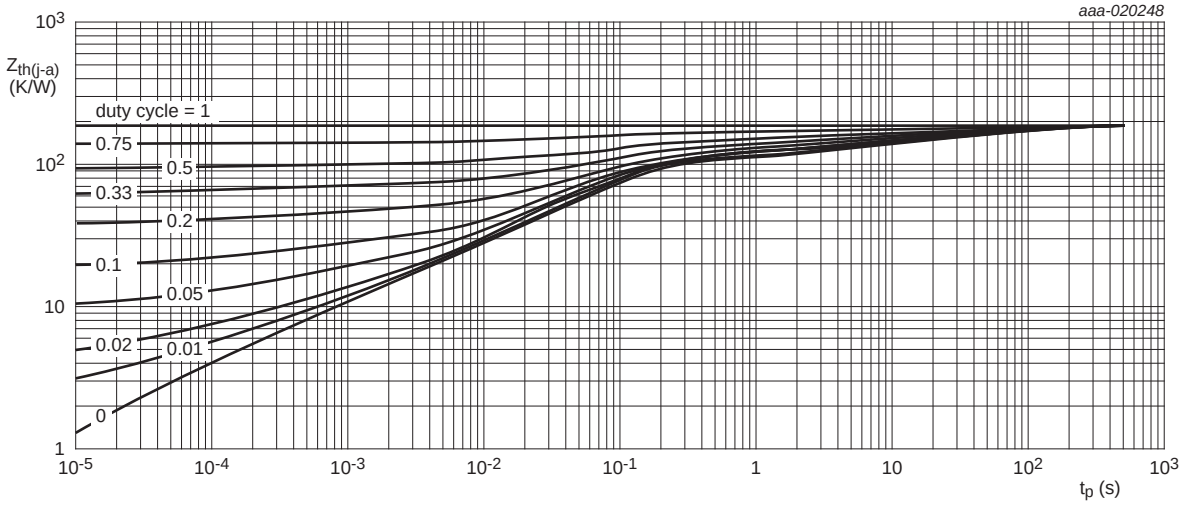
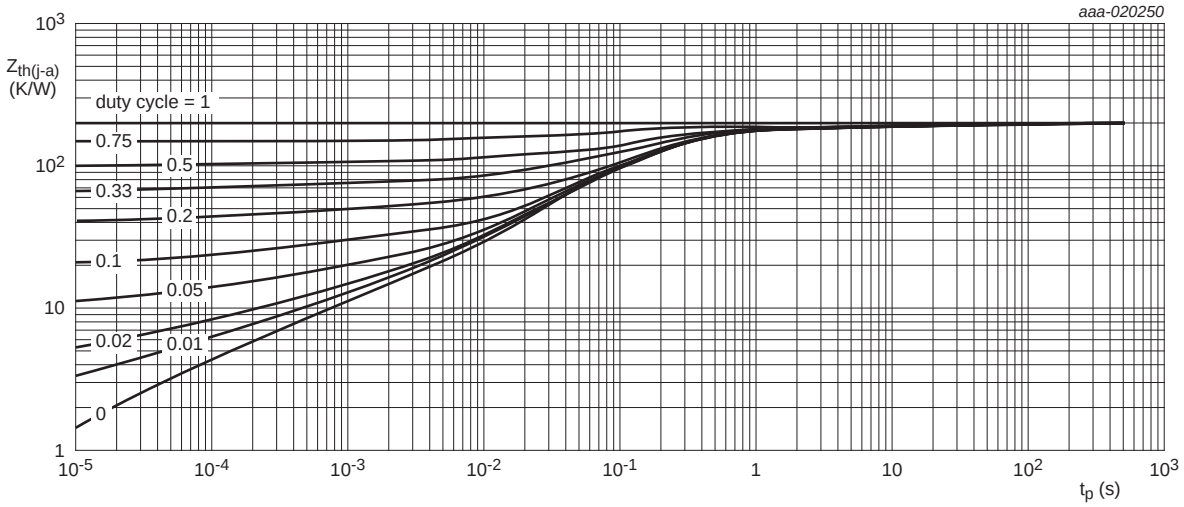



FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 $cm^2$

**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**




FR4 PCB, 4-layer copper, tin-plated and standard footprint

**Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**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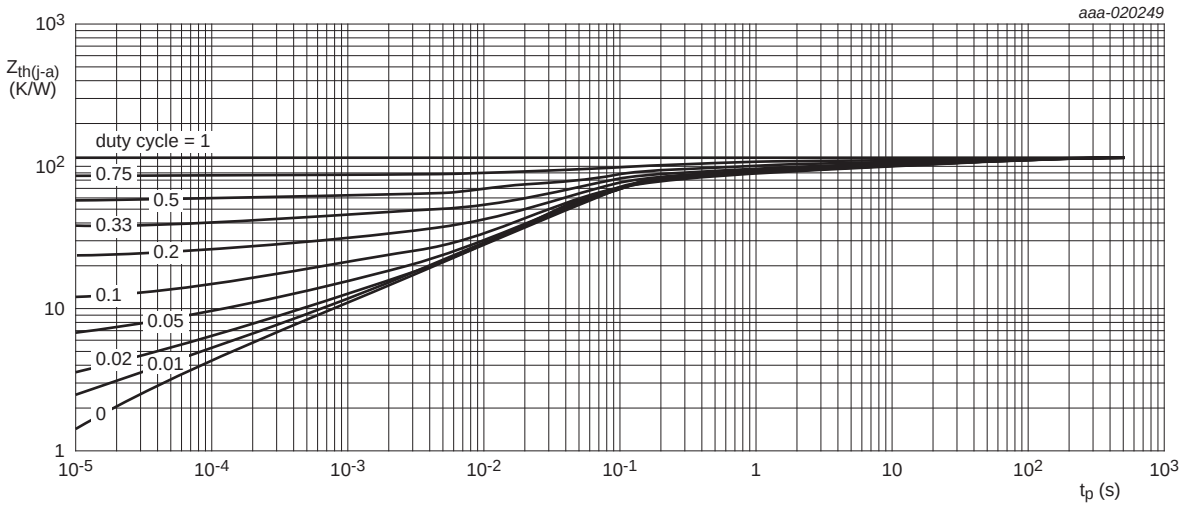


FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 $cm^2$

**Fig 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**


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# 7. Characteristics

**Table 8. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 50 V; $I_E$ = 0 A | - | - | 100 | nA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = 50 V; $I_B$ = 0 A | - | - | 0.5 | µA |
| $I_{EBO}$ | emitter-base cut-off current | | | | | |
| | PDTD113EQA | $V_{EB}$ = 5 V; $I_C$ = 0 A | - | - | 4 | mA |
| | PDTD123EQA | | - | - | 2 | mA |
| | PDTD143EQA | | - | - | 0.9 | mA |
| | PDTD114EQA | | | | 0.4 | mA |
| $h_{FE}$ | DC current gain | | | | | |
| | PDTD113EQA | $V_{CE}$ = 5 V; $I_C$ = 50 mA | 33 | - | - | |
| | PDTD123EQA | | 40 | - | - | |
| | PDTD143EQA | | 60 | - | - | |
| | PDTD114EQA | | 70 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 50 mA; $I_B$ = 2.5 mA | - | - | 100 | mV |
| $V_{I(off)}$ | off-state input voltage | | | | | |
| | PDTD113EQA | $V_{CE}$ = 5 V; $I_C$ = 100 µA | 0.6 | 1.05 | 1.5 | V |
| | PDTD123EQA | | 0.6 | 1.05 | 1.8 | V |
| | PDTD143EQA | | 0.6 | 1.05 | 1.5 | V |
| | PDTD114EQA | | 0.6 | 1.05 | 1.5 | V |
| $V_{I(on)}$ | on-state input voltage | | | | | |
| | PDTD113EQA | $V_{CE}$ = 0.3 V; $I_C$ = 20 mA | 1 | 1.45 | 1.8 | V |
| | PDTD123EQA | | 1 | 1.5 | 2 | V |
| | PDTD143EQA | | 1 | 1.7 | 2.2 | V |
| | PDTD114EQA | | 1 | 2.2 | 3 | V |
| R1 | bias resistor 1 (input) | [1] | | | | |
| | PDTD113EQA | | 0.7 | 1 | 1.3 | kΩ |
| | PDTD123EQA | | 1.54 | 2.2 | 2.86 | kΩ |
| | PDTD143EQA | | 3.3 | 4.7 | 6.1 | kΩ |
| | PDTD114EQA | | 7 | 10 | 13 | kΩ |
| R2/R1 | bias resistor ratio | [1] | 0.9 | 1 | 1.1 | |
| $C_c$ | collector capacitance | $V_{CB}$ = 10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | - | 5 | - | pF |
| $f_T$ | transition frequency | $V_{CE}$ = 5 V; $I_C$ = 50 mA; f = 100 MHz [2] | - | 210 | - | MHz |

[1] See section test information for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.


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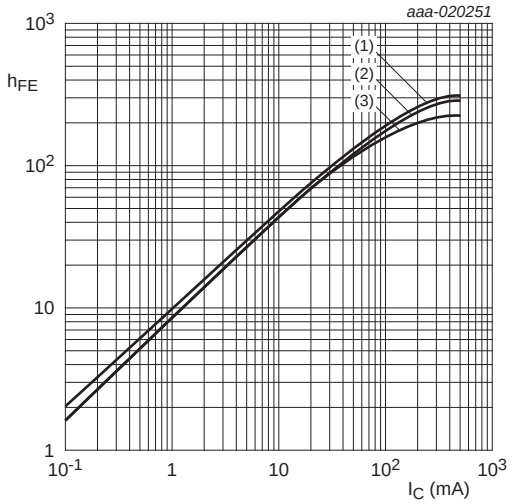


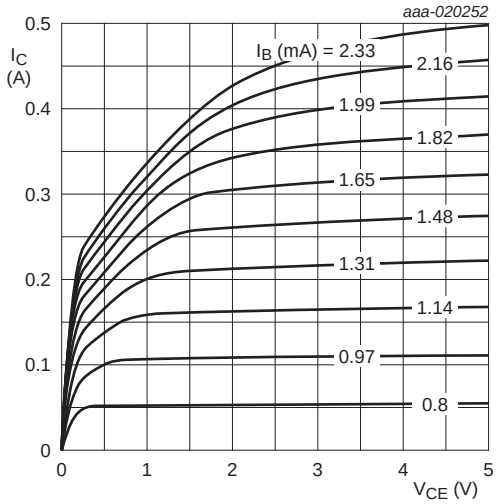

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

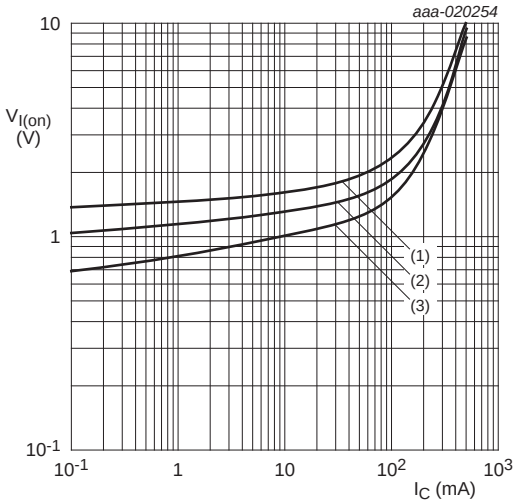
(3) $T_{amb}$ = −40 °C

**Fig 7. PDTD113EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 8. PDTD113EQA: Collector current as a function of collector-emitter voltage; typical values**



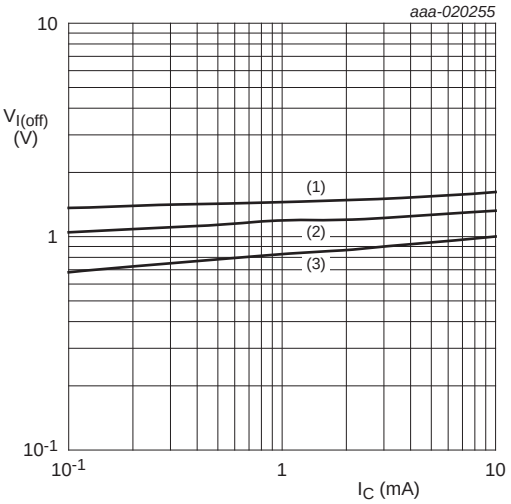

$V_{CE}$ = 0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 9. PDTD113EQA: On-state input voltage as a function of collector current; typical values**




$V_{CE}$ = 5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 10. PDTD113EQA: Off-state input voltage as a function of collector current; typical values**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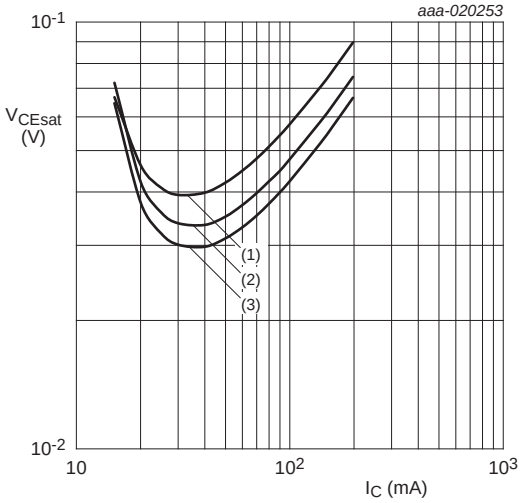


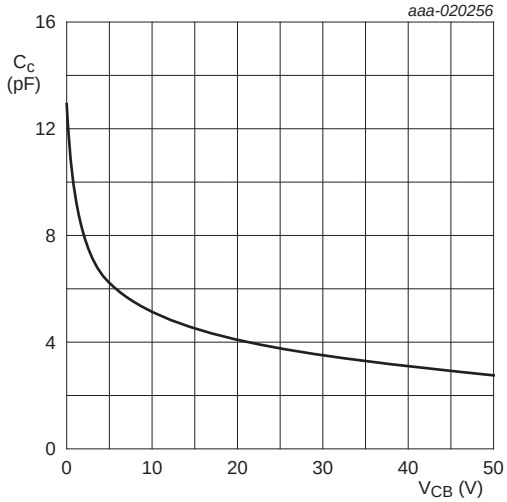

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 11. PDTD113EQA: Collector-emitter saturation voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 12. PDTD113EQA: Collector capacitance as a function of collector-base voltage; typical values**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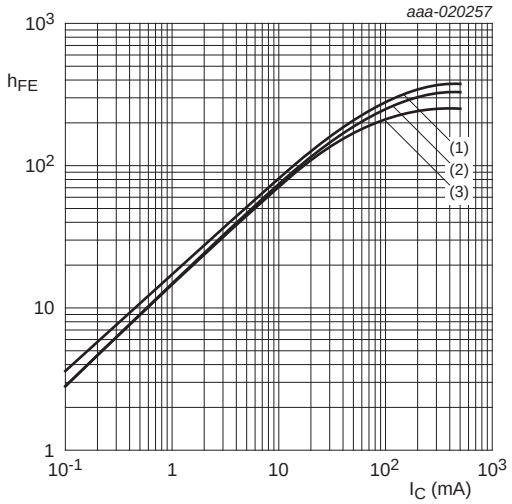


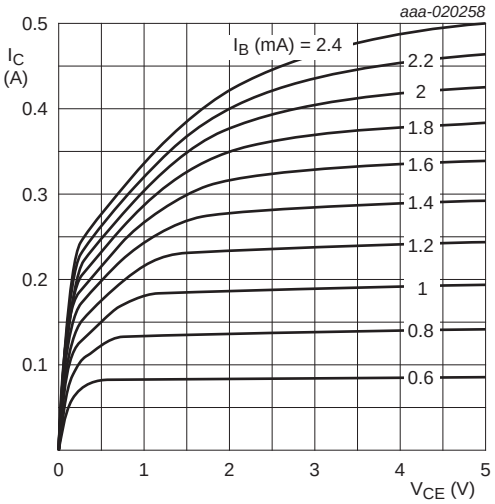

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

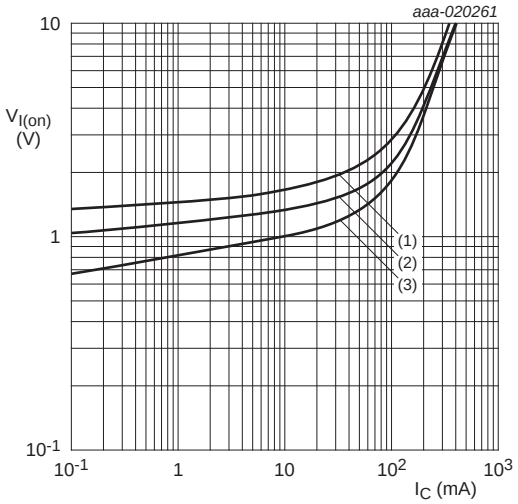
(3) $T_{amb}$ = −40 °C

**Fig 13. PDTD123EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 14. PDTD123EQA: Collector current as a function of collector-emitter voltage; typical values**



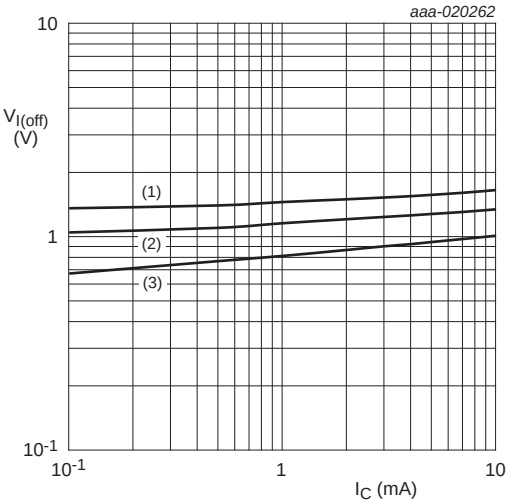

$V_{CE}$ = 0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 15. PDTD123EQA: On-state input voltage as a function of collector current; typical values**




$V_{CE}$ = 5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 16. PDTD123EQA: Off-state input voltage as a function of collector current; typical values**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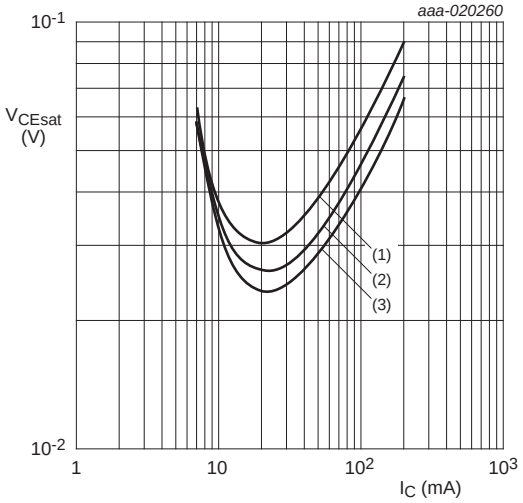


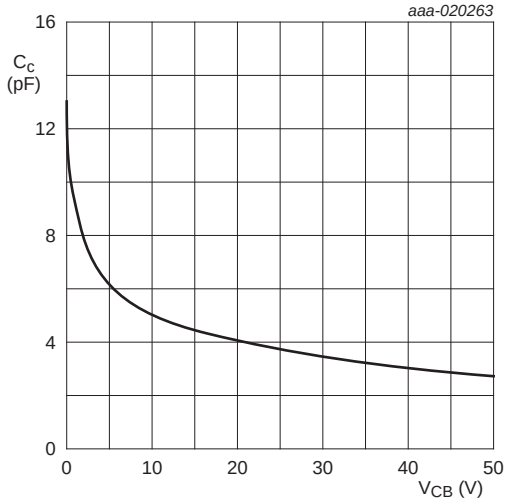

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 17. PDTD123EQA: Collector-emitter saturation voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 18. PDTD123EQA: Collector capacitance as a function of collector-base voltage; typical values**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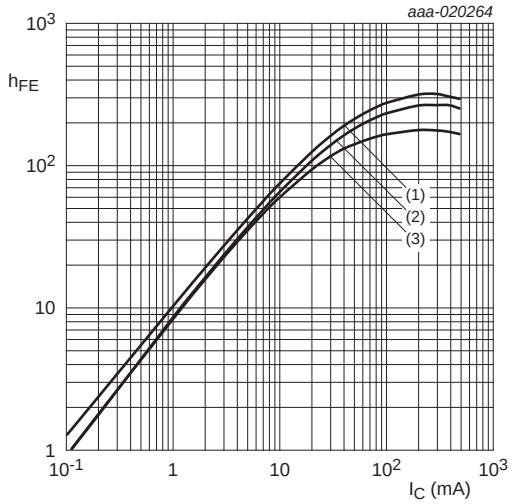


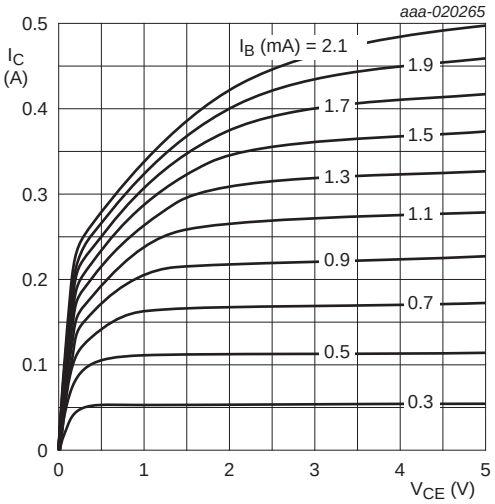

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

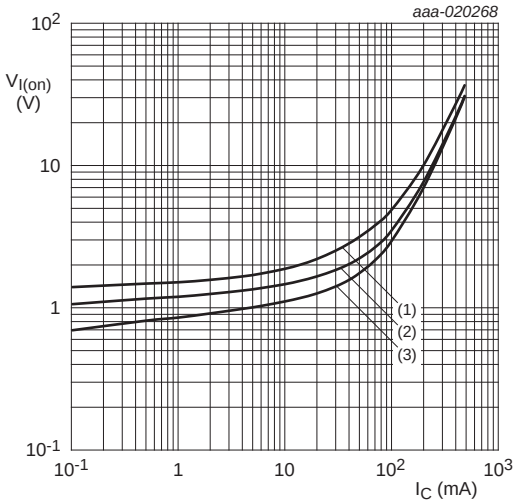
(3) $T_{amb}$ = −40 °C

**Fig 19. PDTD143EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 20. PDTD143EQA: Collector current as a function of collector-emitter voltage; typical values**



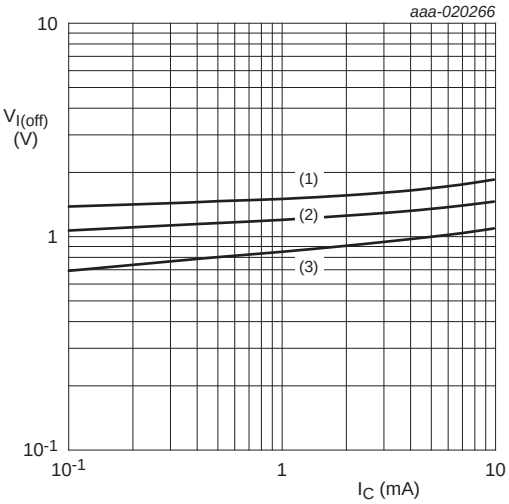

$V_{CE}$ = 0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 21. PDTD143EQA: On-state input voltage as a function of collector current; typical values**




$V_{CE}$ = 5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 22. PDTD143EQA: Off-state input voltage as a function of collector current; typical values**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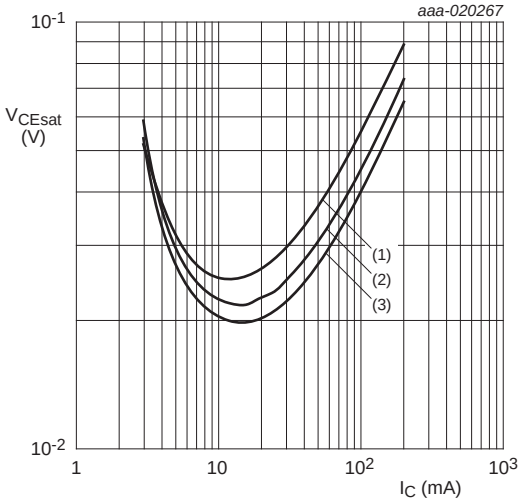


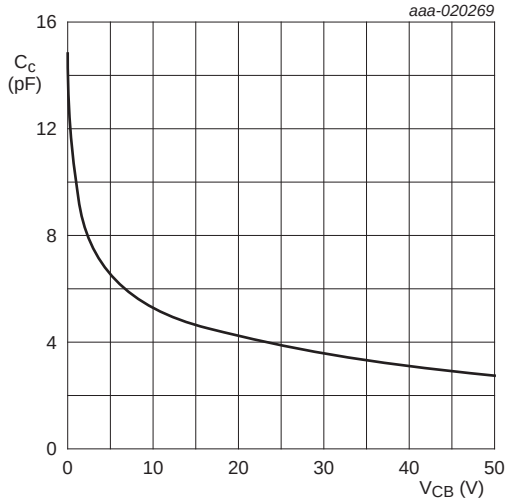

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 23. PDTD143EQA: Collector-emitter saturation voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 24. PDTD143EQA: Collector capacitance as a function of collector-base voltage; typical values**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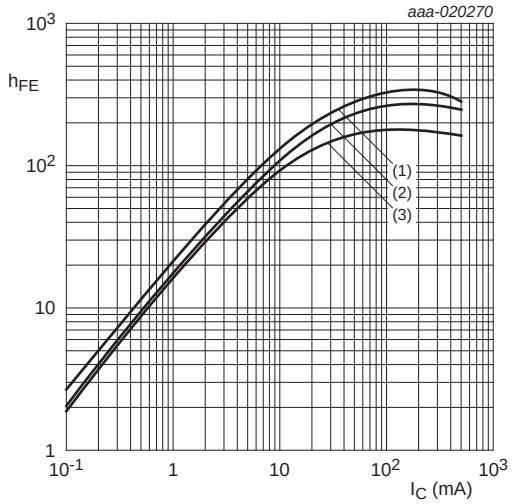


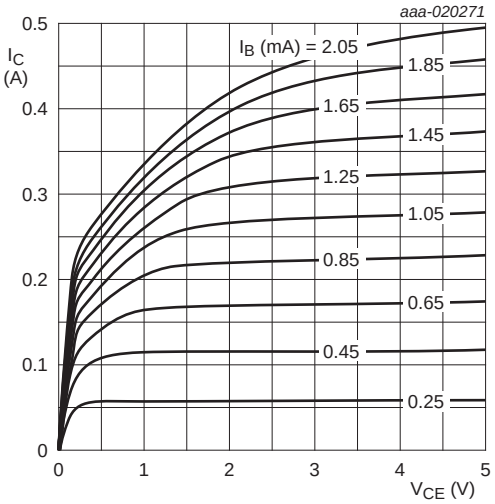

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

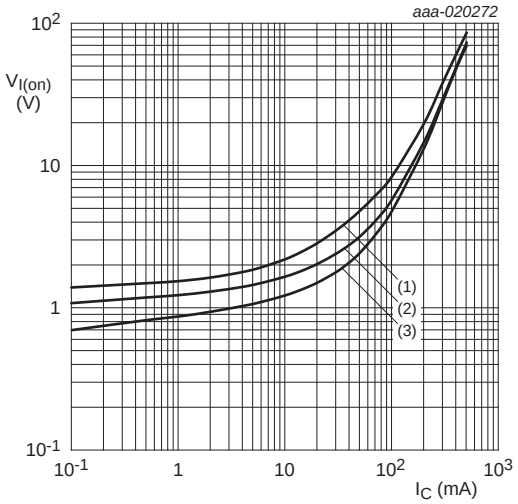
(3) $T_{amb}$ = −40 °C

**Fig 25. PDTD114EQA: DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 26. PDTD114EQA: Collector current as a function of collector-emitter voltage; typical values**



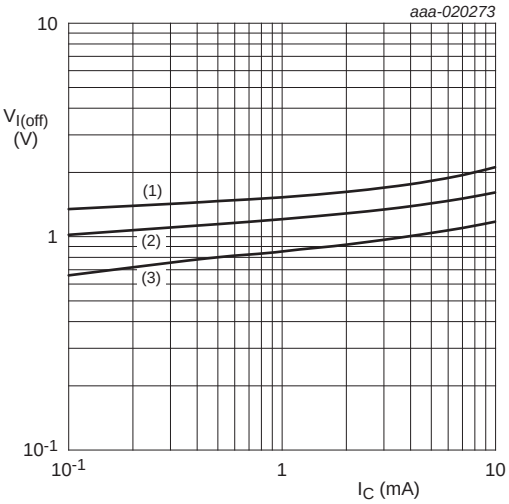

$V_{CE}$ = 0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 27. PDTD114EQA: On-state input voltage as a function of collector current; typical values**




$V_{CE}$ = 5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 28. PDTD114EQA: Off-state input voltage as a function of collector current; typical values**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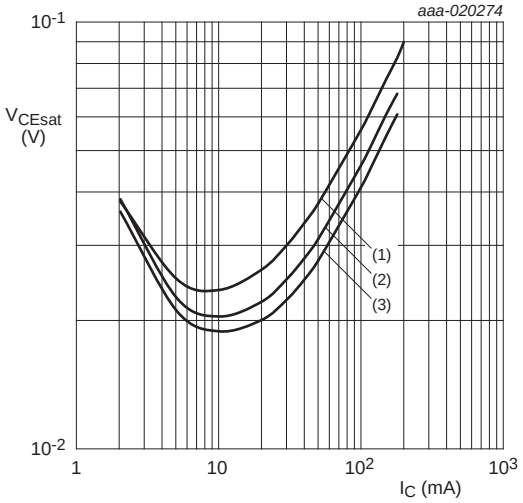


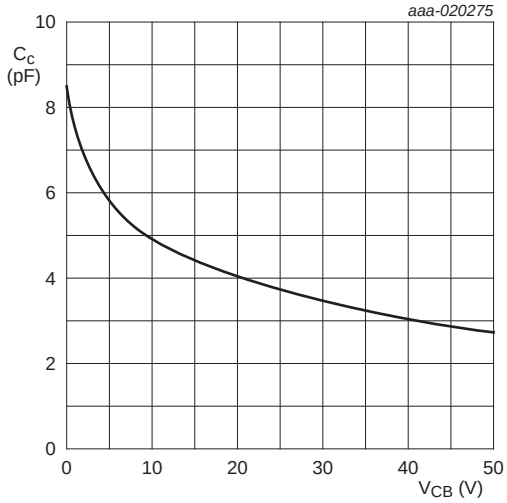

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

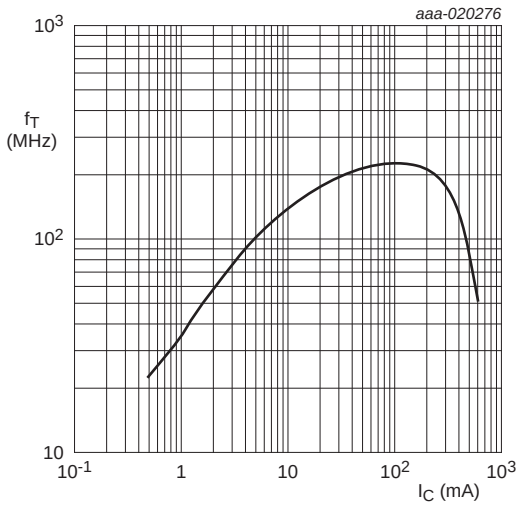
(3) $T_{amb}$ = −40 °C

**Fig 29. PDTD114EQA: Collector-emitter saturation voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 30. PDTD114EQA: Collector capacitance as a function of collector-base voltage; typical values**




$V_{CE}$ = 5 V; f = 100 MHz; $T_{amb}$ = 25 °C

**Fig 31. Transition frequency as a function of collector current; typical values of built-in transistor**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# 8. Test information

## 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 8.2 Resistor calculation

- Calculation of bias resistor 1 (R1):

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation method A of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_{I3})}{R1 \cdot I_{I3}} - 1$$

- Calculation method B of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

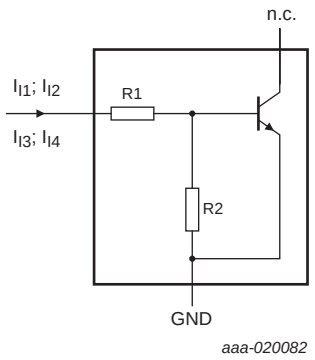


**Fig 32. Resistor test circuit**


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### 8.3 Resistor test conditions

**Table 9. Resistor test conditions**

| Type number | R1 | R2 | Test conditions | | | |
|---|---|---|---|---|---|---|
| | kΩ | kΩ | $I_{I1}$ | $I_{I2}$ | $I_{I3}$ | $I_{I4}$ |
| PDTD113EQA [1] | 1 | 1 | 1.5 mA | 1.9 mA | –2.2 mA | - |
| PDTD123EQA [1] | 2.2 | 2.2 | 0.7 mA | 0.8 mA | –0.75 mA | - |
| PDTD143EQA [2] | 4.7 | 4.7 | 1.3 mA | 1.5 mA | –1.05 mA | –1.25 mA |
| PDTD114EQA [2] | 10 | 10 | 0.7 mA | 0.8 mA | –0.45 mA | –0.55 mA |

[1] Uses calculation method A of bias resistor ratio R2/R1

[2] Uses calculation method B of bias resistor ratio R2/R1

## 9. Package outline

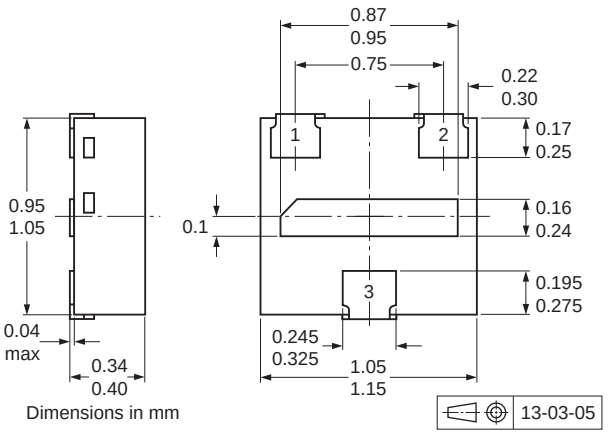


**Fig 33. Package outline DFN1010D-3 (SOT1215)**


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## 10. Soldering

**Footprint information for reflow soldering of DFN1010D-3 package** **SOT1215**

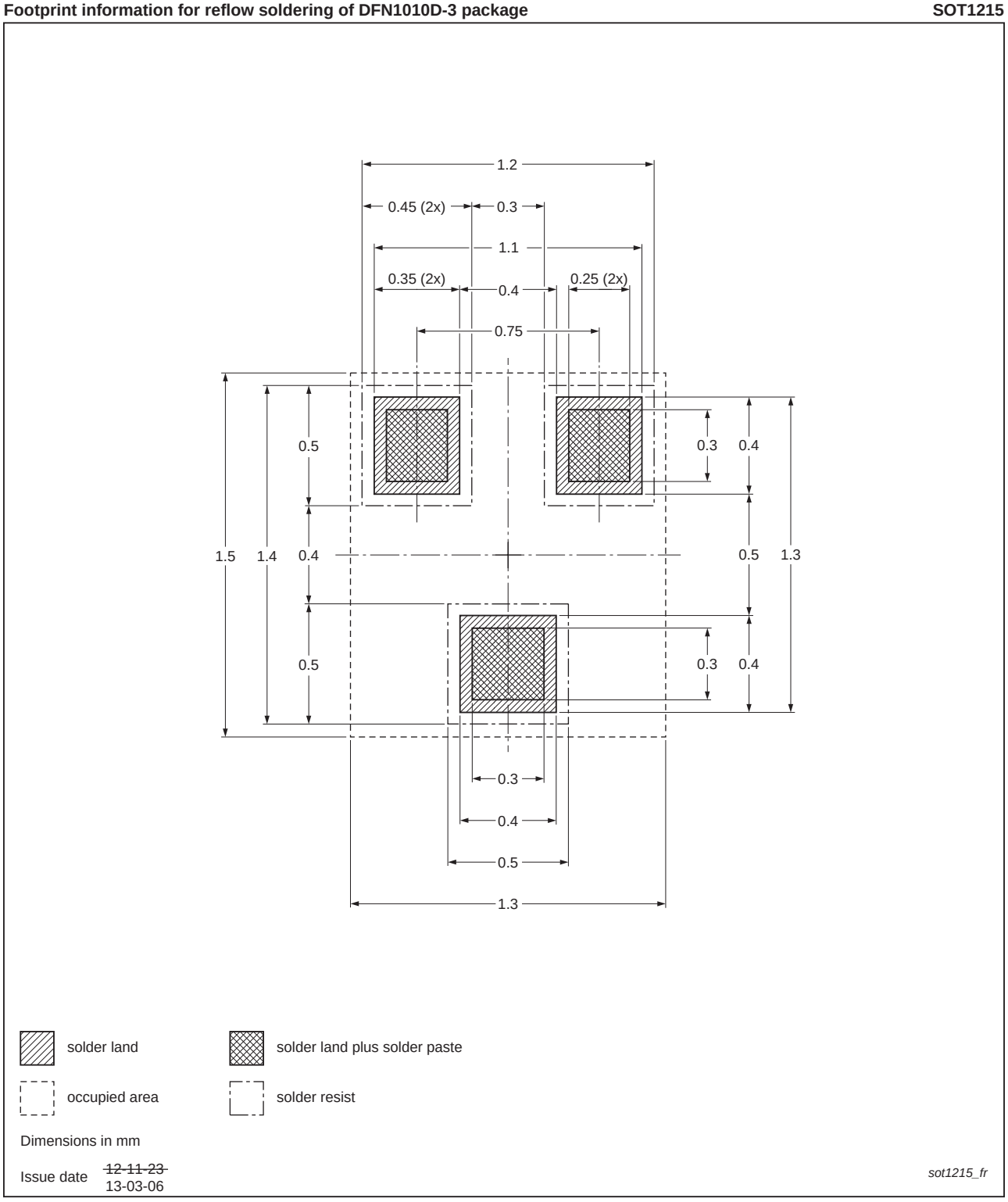


**Fig 34. Reflow soldering footprint DFN1010D-3 (SOT1215)**


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## 11. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PDTD113_123_143_114EQA_SER v.1 | 20160104 | Product data sheet | - | - |


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# 12. Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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