

# 74ALVT162823

18-bit bus-interface D-type flip-flop with reset and enable with 30  $\Omega$  termination resistors; 3-state

Rev. 3 — 23 January 2018

Product data sheet

## 1 General description

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The 74ALVT162823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data or address paths of buses carrying parity.

The 74ALVT162823 has two 9-bit wide buffered registers with clock enable ( $\overline{nCE}$ ) and master reset ( $\overline{nMR}$ ) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding Q output of the flip-flop.

The 74ALVT162823 is designed with 30  $\Omega$  series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers or transmitters.

## 2 Features and benefits

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- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5 V I/O compatible
- Ideal where high speed, light loading or increased fan-in are required with MOS microprocessors
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- Output capability: +12 mA to -12 mA
- Outputs include series resistance of 30  $\Omega$  making external termination resistors unnecessary
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883, method 3015: exceeds 2000 V
  - MM: exceeds 200 V



18-bit bus-interface D-type flip-flop with reset and enable with 30 Ω termination resistors; 3-state

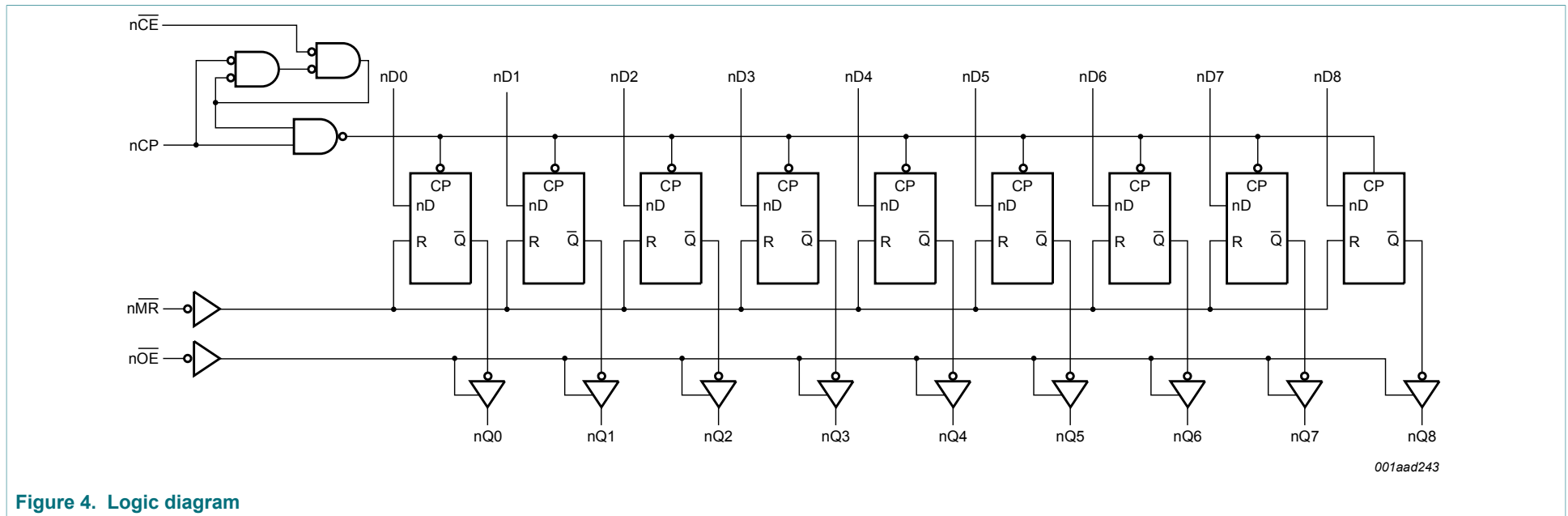


Figure 4. Logic diagram

## 5 Pinning information

### 5.1 Pinning

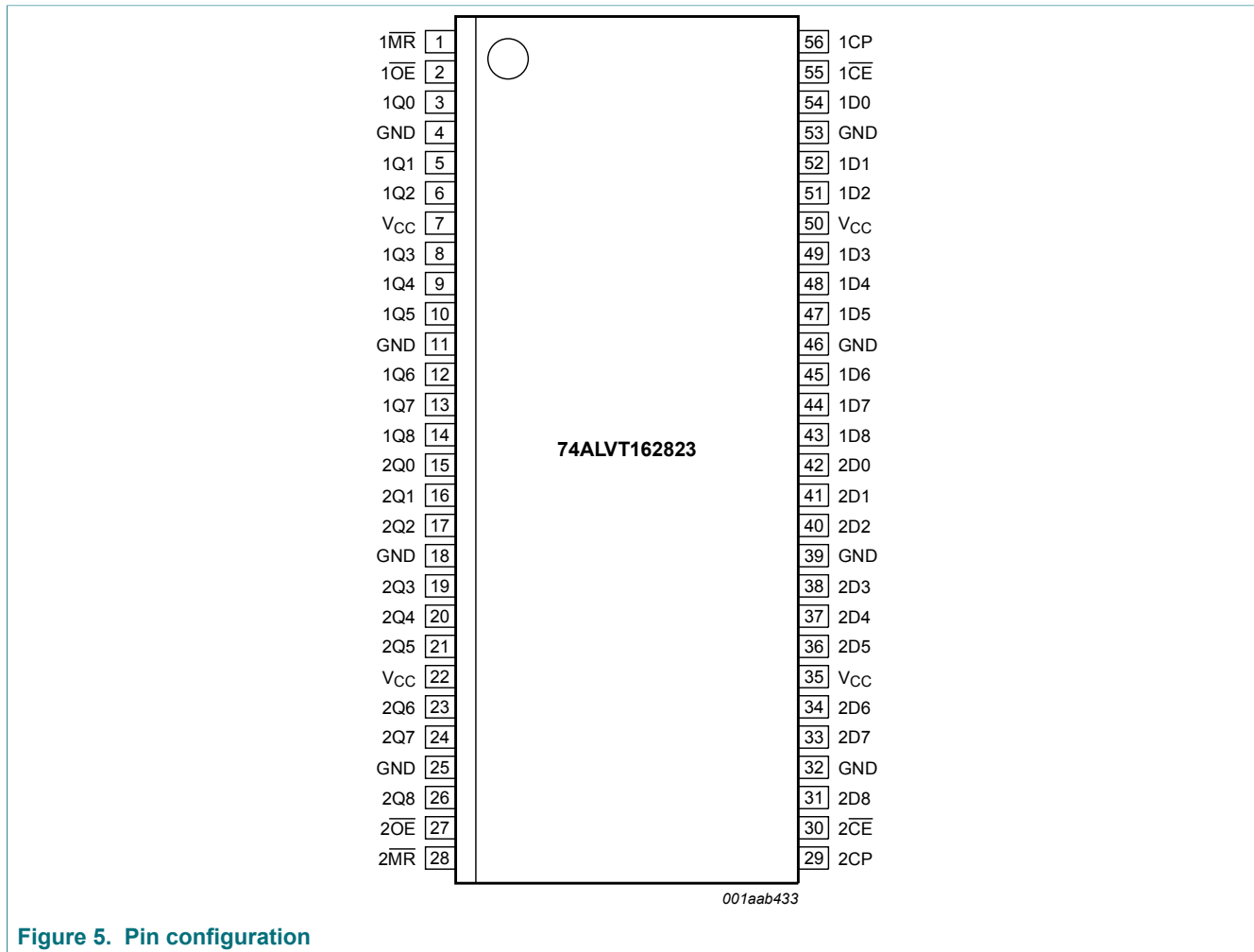


Figure 5. Pin configuration

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8	54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8	3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8	42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8	15, 16, 17, 19, 20, 21, 23, 24, 26	data outputs
$1\overline{MR}$ , $2\overline{MR}$	1, 28	master reset input (active-LOW)
$1\overline{OE}$ , $2\overline{OE}$	2, 27	output enable inputs (active LOW)
1CP, 2CP	56, 29	clock pulse inputs (active rising edge)
$1\overline{CE}$ , $2\overline{CE}$	55, 30	clock enable input (active-LOW)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V <sub>CC</sub>	7, 22, 35, 50	supply voltage

## 6 Functional description

Table 3. Function table <sup>[1]</sup>

Operating mode	Input					Output
	n $\overline{OE}$	n $\overline{MR}$	n $\overline{CE}$	nCP	nDn	nQn
Clear	L	L	X	X	X	L
Load and read data	L	H	L	$\uparrow$	h	H
					l	L
Hold	L	H	H	NC	X	NC
High-impedance	H	X	X	X	X	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
 NC = no change;  
 X = don't care;  
 Z = high-impedance OFF-state;  
 $\uparrow$  = LOW-to-HIGH clock transition;

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-	-50	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$T_j$	junction temperature		[2] -	150	$^{\circ}$ C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC} = 2.5</math> V</b>						
$V_{CC}$	supply voltage		2.3	-	2.7	V
$V_I$	input voltage		0	-	5.5	V
$I_{OH}$	HIGH-level output current		-	-	-8	mA
$I_{OL}$	LOW-level output current		-	-	12	mA
$\Delta t/\Delta v$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	$^{\circ}$ C
<b><math>V_{CC} = 3.3</math> V</b>						
$V_{CC}$	supply voltage		3.0	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$I_{OH}$	HIGH-level output current		-	-	-12	mA
$I_{OL}$	LOW-level output current		-	-	12	mA
$\Delta t/\Delta v$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	$^{\circ}$ C

## 9 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b><math>V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>						
$V_{IK}$	input clamping voltage	$V_{CC} = 2.3\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
$V_{IH}$	HIGH-level input voltage		1.7	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.7	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.3\text{ V}$ ; $I_O = -8\text{ mA}$	1.7	2.5	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.3\text{ V}$ ; $I_O = 12\text{ mA}$	-	0.3	0.5	V
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_O = 1\text{ mA}$ ; $V_I = V_{CC}$ or GND <sup>[2]</sup>	-	0.2	0.55	V
$I_I$	input leakage current	control pins				
		$V_{CC} = 2.7\text{ V}$ ; $V_I = \text{GND}$	-	0.1	±1	µA
		$V_{CC} = 2.7\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	µA
		I/O data pins <sup>[3]</sup>				
		$V_{CC} = 2.7\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	µA
		$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$	-	0.5	1	µA
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V to }4.5\text{ V}$	-	0.1	±100	µA
		$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$				
$I_{BHL}$	bus hold LOW current	data inputs; $V_{CC} = 2.5\text{ V}$ ; $V_I = 0.7\text{ V}$ <sup>[4]</sup>	-	100	-	µA
$I_{BHH}$	bus hold HIGH current	data inputs; $V_{CC} = 2.5\text{ V}$ ; $V_I = 1.7\text{ V}$ <sup>[4]</sup>	-	-70	-	µA
$I_{EX}$	external current	output HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 2.5\text{ V}$	-	10	125	µA
$I_{O(pu\text{p}d)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V to }V_{CC}$ ; $V_I = \text{GND or }V_{CC}$ <sup>[5]</sup>	-	1	±100	µA
$I_{OZ}$	OFF-state output current	$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$				
		output HIGH state; $V_O = 2.3\text{ V}$	-	0.5	5	µA
		output LOW-state; $V_O = 0.5\text{ V}$	-	0.5	-5	µA
$I_{CC}$	supply current	$V_{CC} = 2.7\text{ V}$ ; $V_I = \text{GND or }V_{CC}$ ; $I_O = 0\text{ A}$				
		outputs HIGH-state	-	0.04	0.1	mA
		outputs LOW-state	-	2.7	4.5	mA
		outputs disabled <sup>[6]</sup>	-	0.04	0.1	mA

## 18-bit bus-interface D-type flip-flop with reset and enable with 30 Ω termination resistors; 3-state

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ ; one input at $V_{CC} - 0.6 \text{ V}$ , other inputs at $V_{CC}$ or GND <sup>[7]</sup>	-	0.04	0.4	mA
$C_I$	input capacitance	$V_I = 0 \text{ V or } V_{CC}$	-	3	-	pF
$C_O$	output capacitance	$V_{IO} = 0 \text{ V or } 3.0 \text{ V}$	-	9	-	pF
<b><math>V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}</math></b>						
$V_{IK}$	input clamping voltage	$V_{CC} = 3.0 \text{ V}$ ; $I_{IK} = -18 \text{ mA}$	-	-0.85	-1.2	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 3.0 \text{ V}$ ; $I_O = -12 \text{ mA}$	2.0	2.3	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 3.0 \text{ V}$ ; $I_O = 12 \text{ mA}$	-	0.5	0.8	V
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 3.6 \text{ V}$ ; $I_O = 1 \text{ mA}$ ; $V_I = V_{CC}$ or GND <sup>[2]</sup>	-	-	0.55	V
$I_I$	input leakage current	control pins				
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{CC}$ or GND	-	0.1	±1	μA
		$V_{CC} = 0 \text{ V or } 3.6 \text{ V}$ ; $V_I = 5.5 \text{ V}$	-	0.1	10	μA
		I/O data pins <sup>[3]</sup>				
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = 5.5 \text{ V}$	-	0.1	10	μA
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{CC}$	-	0.5	1	μA
		$V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V}$	-	0.1	-5	μA
$I_{OFF}$	power-off leakage current	$V_{CC} = 0 \text{ V}$ ; $V_I$ or $V_O = 0 \text{ V to } 4.5 \text{ V}$	-	0.1	±100	μA
$I_{BHL}$	bus hold LOW current	data inputs; $V_{CC} = 3 \text{ V}$ ; $V_I = 0.8 \text{ V}$	75	130	-	μA
$I_{BHH}$	bus hold HIGH current	data inputs; $V_{CC} = 3 \text{ V}$ ; $V_I = 2.0 \text{ V}$	-75	-140	-	μA
$I_{BHLO}$	bus hold LOW overdrive current	data inputs; $V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V to } 3.6 \text{ V}$ <sup>[8]</sup>	500	-	-	μA
$I_{BHHO}$	bus hold HIGH overdrive current	data inputs; $V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V to } 3.6 \text{ V}$ <sup>[8]</sup>	-500	-	-	μA
$I_{EX}$	external current	output HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5 \text{ V}$ ; $V_{CC} = 3.0 \text{ V}$	-	10	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2 \text{ V}$ ; $V_O = 0.5 \text{ V to } V_{CC}$ ; $V_I = \text{GND or } V_{CC}$ <sup>[9]</sup>	-	1	±100	μA
$I_{OZ}$	OFF-state output current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$				
		output HIGH state; $V_O = 3.0 \text{ V}$	-	0.5	5	μA
		output LOW-state; $V_O = 0.5 \text{ V}$	-	0.5	-5	μA
$I_{CC}$	supply current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = \text{GND or } V_{CC}$ ; $I_O = 0 \text{ A}$				
		outputs HIGH-state	-	0.05	0.1	mA
		outputs LOW-state	-	3.9	5.5	mA
		outputs disabled <sup>[6]</sup>	-	0.06	0.1	mA



18-bit bus-interface D-type flip-flop with reset and enable with 30 Ω termination resistors; 3-state

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3\text{ V to }3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND	-	0.04	0.4	mA
$C_I$	input capacitance	$V_I = 0\text{ V or }V_{CC}$	-	3	-	pF
$C_O$	output capacitance	$V_{IO} = 0\text{ V or }3.0\text{ V}$	-	9	-	pF

- [1] All typical values for  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  are measured at  $V_{CC} = 2.5\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .  
All typical values for  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .
- [2] For valid test results, data must not be loaded into the flip-flops after applying power.
- [3] Unused pins at  $V_{CC}$  or GND.
- [4] Not guaranteed.
- [5] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  a transition time of 100 μs is permitted. This parameter is valid for  $T_{amb} = 25\text{ }^\circ\text{C}$  only.
- [6]  $I_{CC}$  is measured with outputs pulled up to  $V_{CC}$  or pulled down to ground.
- [7] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.
- [8] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [9] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of 100 μs is permitted. This parameter is valid for  $T_{amb} = 25\text{ }^\circ\text{C}$  only.

## 10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ ; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b><math>V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>						
$t_{PLH}$	LOW to HIGH propagation delay	nCP to nQn; see Figure 6	2.1	3.7	5.8	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	nCP to nQn; see Figure 6	2.0	2.8	4.6	ns
		nMR to nQn; see Figure 8	2.0	3.0	4.6	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	nOE to nQn; see Figure 9	2.8	4.4	6.6	ns
$t_{PZL}$	OFF-state to LOW propagation delay	nOE to nQn; see Figure 9	2.0	3.4	5.2	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	nOE to nQn; see Figure 9	2.3	3.2	4.6	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	nOE to nQn; see Figure 9	2.0	2.5	3.5	ns
$t_{su(H)}$	set-up time HIGH	nDn to nCP; see Figure 7	1.0	0.5	-	ns
		nCE to nCP; see Figure 7	1.0	0.2	-	ns
$t_{su(L)}$	set-up time LOW	nDn to nCP; see Figure 7	2.0	1.3	-	ns
		nCE to nCP; see Figure 7	0.5	-0.1	-	ns
$t_{h(H)}$	hold time HIGH	nDn to nCP; see Figure 7	0.1	-1.4	-	ns
		nCE to nCP; see Figure 7	1.0	0.2	-	ns
$t_{h(L)}$	hold time LOW	nDn to nCP; see Figure 7	0.1	-0.5	-	ns
		nCE to nCP; see Figure 7	1.0	-0.1	-	ns
$t_W$	pulse width	nCP HIGH; see Figure 6	2.0	0.8	-	ns
		nCP LOW	3.0	2.1	-	ns
		nMR LOW; see Figure 8	2.0	0.8	-	ns
$t_{rec}$	recovery time	nMR to nCP; see Figure 8	2.3	1.3	-	ns

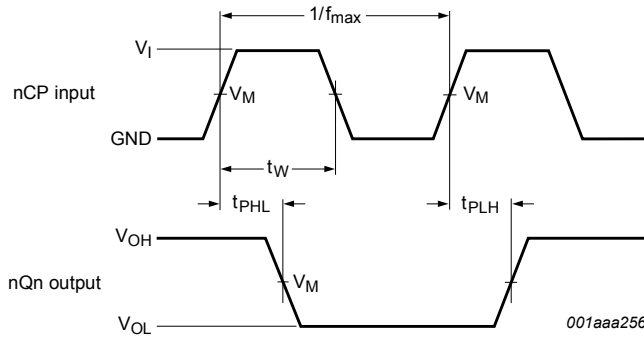
18-bit bus-interface D-type flip-flop with reset and enable with 30  $\Omega$  termination resistors; 3-state

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>V<sub>CC</sub> = 3.3 V <math>\pm</math> 0.3 V</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay	nCP to nQn; see <a href="#">Figure 6</a>	1.8	2.9	4.4	ns
t <sub>PHL</sub>	HIGH-to-LOW propagation delay	nCP to nQn; see <a href="#">Figure 6</a>	1.6	2.3	3.6	ns
		nMR to nQn; see <a href="#">Figure 8</a>	1.8	2.5	3.7	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	nOE to nQn; see <a href="#">Figure 9</a>	2.0	3.5	5.2	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nOE to nQn; see <a href="#">Figure 9</a>	1.7	2.8	3.8	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	nOE to nQn; see <a href="#">Figure 9</a>	2.4	3.5	4.7	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nOE to nQn; see <a href="#">Figure 9</a>	1.9	2.8	3.8	ns
t <sub>su(H)</sub>	set-up time HIGH	nDn to nCP; see <a href="#">Figure 7</a>	1.0	0.5	-	ns
		nCE to nCP; see <a href="#">Figure 7</a>	1.0	0.1	-	ns
t <sub>su(L)</sub>	set-up time LOW	nDn to nCP; see <a href="#">Figure 7</a>	1.6	1.1	-	ns
		nCE to nCP; see <a href="#">Figure 7</a>	0.5	-0.5	-	ns
t <sub>h(H)</sub>	hold time HIGH	nDn to nCP; see <a href="#">Figure 7</a>	0.1	-0.5	-	ns
		nCE to nCP; see <a href="#">Figure 7</a>	1.0	-0.1	-	ns
t <sub>h(L)</sub>	hold time LOW	nDn to nCP; see <a href="#">Figure 7</a>	0.1	-0.7	-	ns
		nCE to nCP; see <a href="#">Figure 7</a>	1.0	0.5	-	ns
t <sub>w</sub>	pulse width	nCP HIGH; see <a href="#">Figure 6</a>	1.5	0.7	-	ns
		nCP LOW	2.5	1.4	-	ns
		nMR LOW; see <a href="#">Figure 8</a>	2.0	1.5	-	ns
t <sub>rec</sub>	recovery time	nMR to nCP; see <a href="#">Figure 8</a>	2.0	1.1	-	ns

[1] All typical values for V<sub>CC</sub> = 2.5 V  $\pm$  0.2 V are measured at V<sub>CC</sub> = 2.5 V and T<sub>amb</sub> = 25 °C.

All typical values for V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

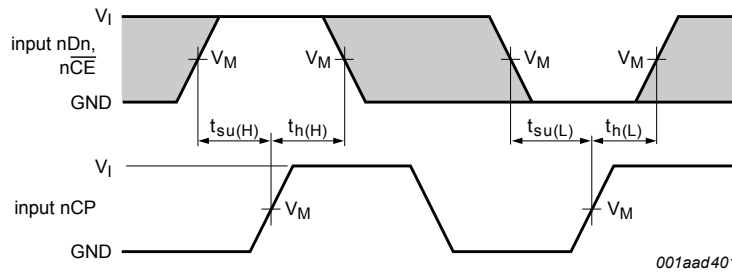
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

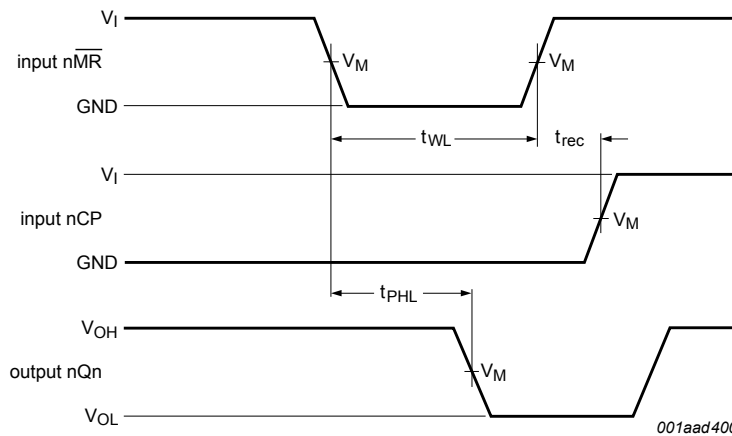
**Figure 6. Propagation delay clock input (nCP) to output (nQn), clock pulse (nCP) width HIGH and maximum clock frequency**



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 7. Data set-up and hold times**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Figure 8. Master reset (nMR) pulse width, master reset (nMR) to output (nQn) propagation delay and master reset (nMR) to clock (nCP) recovery time**

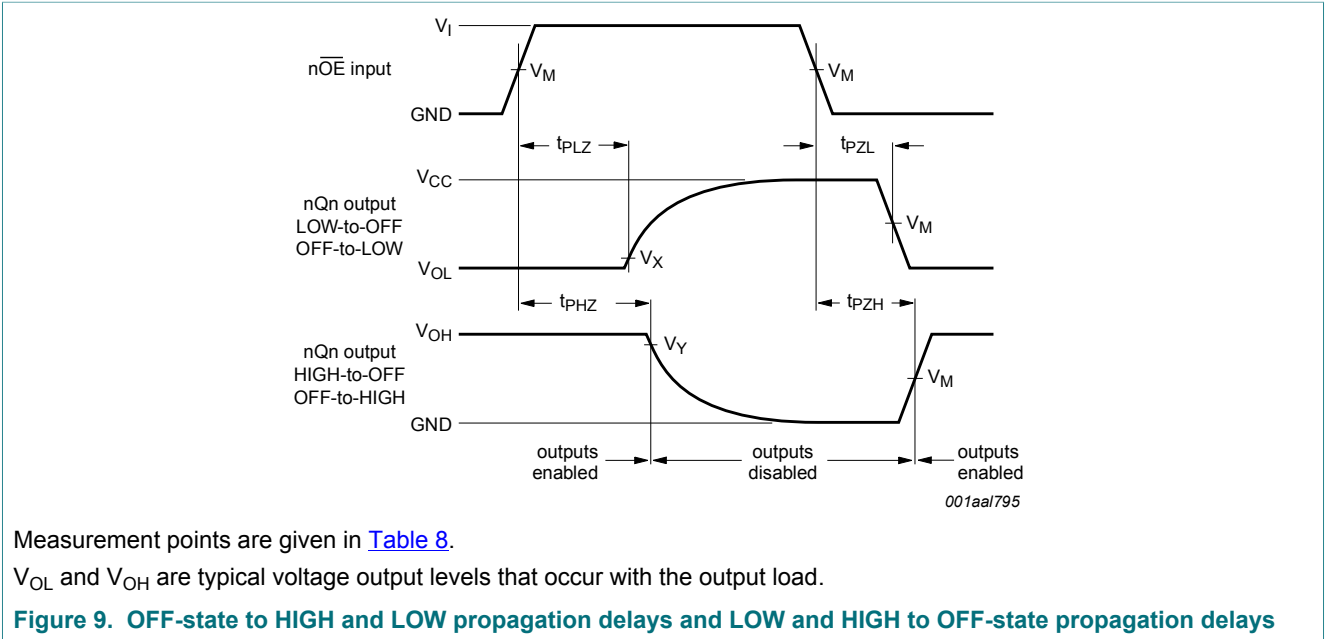


Table 8. Measurement points

$V_{CC}$	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
$\leq 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
$\geq 3.0\text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

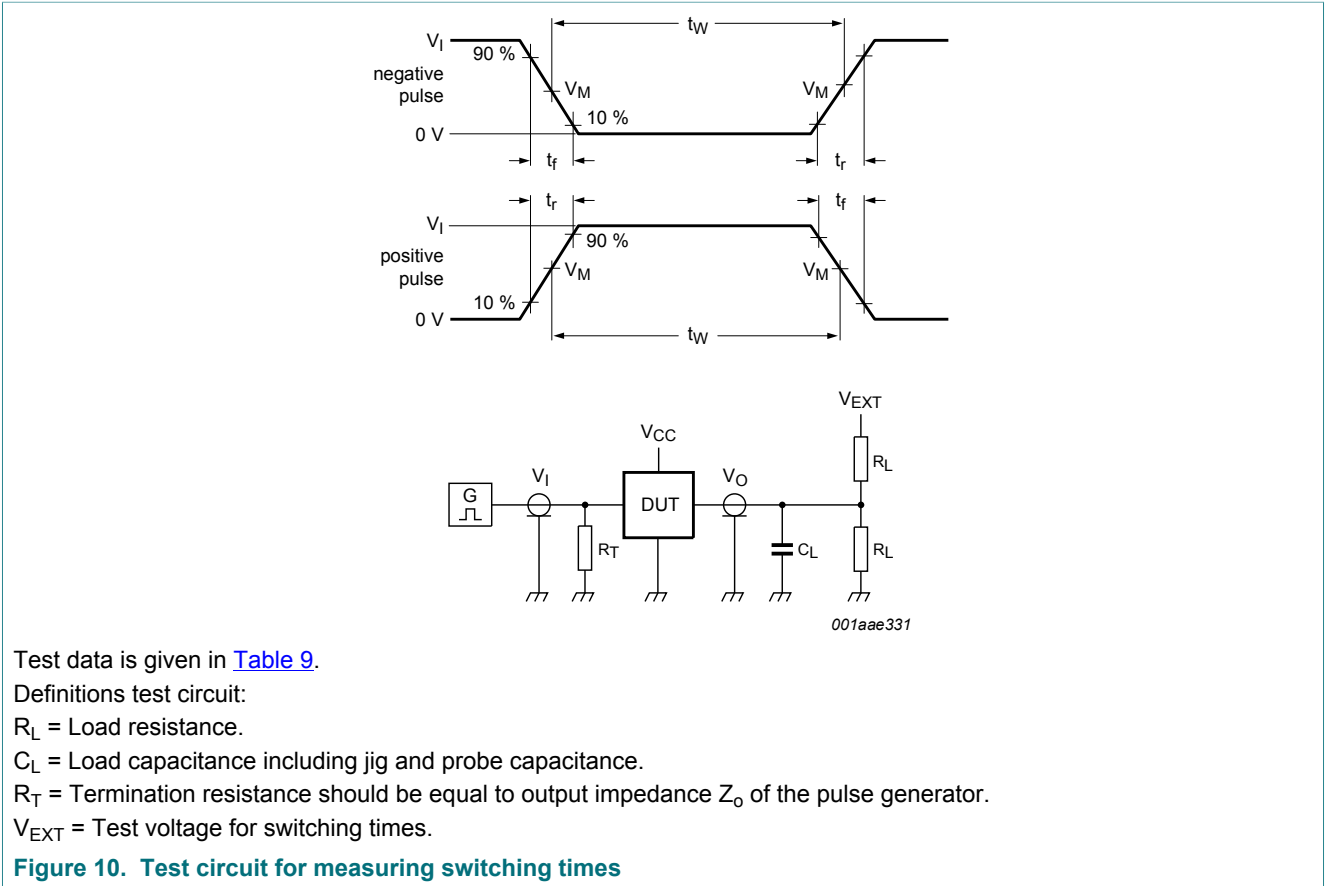


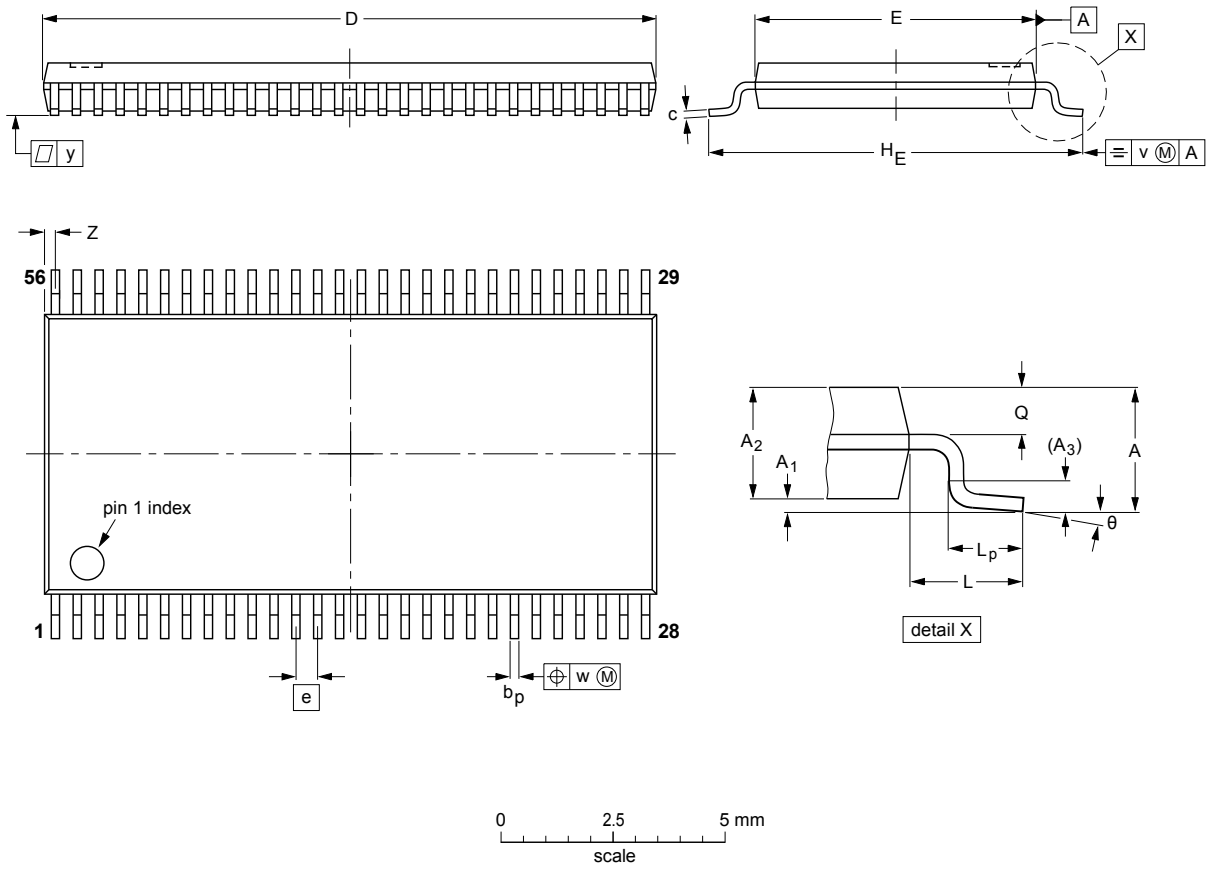
Table 9. Test data

Input		Load				$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V or $V_{CC}$ whichever is less	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 Ω	GND	6 V or $V_{CC} \times 2$	open

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				99-12-27 03-02-19

Figure 11. Package outline SOT364-1 (TSSOP56)

## 12 Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
MOS	Metal-Oxide Semiconductor

## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVT162823 v.3	20180123	Product data sheet	-	74ALVT162823 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ALVT162823DL (SOT371-1 / SSOP56) removed.</li> </ul>			
74ALVT162823 v.2	20050811	Product data sheet	-	74ALVT162823 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 2</a>: modified 'Jedec Std 17' into 'JESD78'</li> <li><a href="#">Section 10</a>: changed propagation delays.</li> </ul>			
74ALVT162823 v.1	19980827	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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**18-bit bus-interface D-type flip-flop with reset and enable with 30  $\Omega$  termination resistors; 3-state**

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