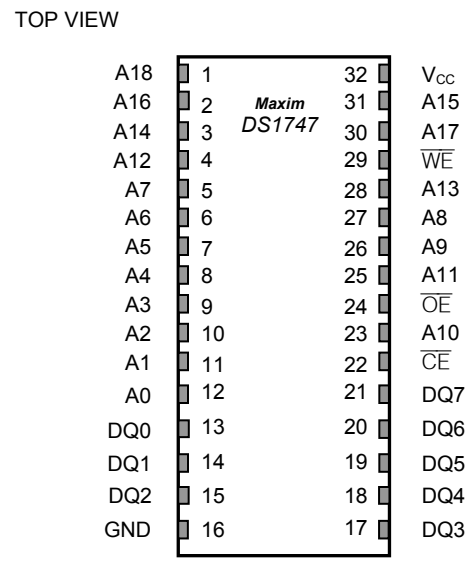
DS1747/DS1747P
Y2K-Compliant, Nonvolatile Timekeeping RAMs

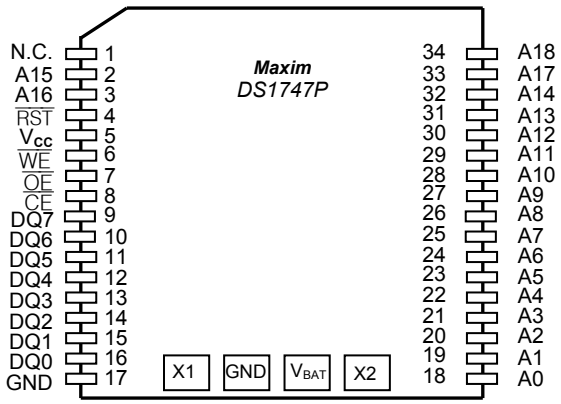
FEATURES

- **Integrated NV SRAM, Real-Time Clock (RTC), Crystal, Power-Fail Control Circuit, and Lithium Energy Source**
- **Clock Registers are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations**
- **Century Byte Register (Y2K Compliant)**
- **Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power**
- **BCD-Coded Century, Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap Year Compensation Valid Up to the Year 2100**
- **Battery Voltage-Level Indicator Flag**
- **Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance**
- **Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time**
- **DIP Module Only:**
  Standard JEDEC Byte-Wide 512k x 8 Static RAM Pinout
- **PowerCap Module Board Only:**
  Surface-Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Power-On Reset Output
  Pin-for-Pin Compatible with Other Densities of DS174xP Timekeeping RAM
- **Also Available in Industrial Temperature Range: -40°C to +85°C**

PIN CONFIGURATIONS



Encapsulated DIP (512k x 8)



PowerCap Module Board
(Uses DS9034PCX+ or DS9034I-PCX+ PowerCap)

19-5504; Rev 6/13

PIN DESCRIPTION

PIN		NAME	FUNCTION
EDIP	PowerCap		
1	34	A18	Address Input
2	3	A16	
3	32	A14	
4	30	A12	
5	25	A7	
6	24	A6	
7	23	A5	
8	22	A4	
9	21	A3	
10	20	A2	
11	19	A1	
12	18	A0	
23	28	A10	
25	29	A11	
26	27	A9	
27	26	A8	
28	31	A13	
30	33	A17	
31	2	A15	
13	16	DQ0	Data Input/Output
14	15	DQ1	
15	14	DQ2	
17	13	DQ3	
18	12	DQ4	
19	11	DQ5	
20	10	DQ6	
21	9	DQ7	
16	17	GND	Ground
22	8	$\overline{CE}$	Active-Low Chip-Enable Input
24	7	$\overline{OE}$	Active-Low Output-Enable Input
29	6	$\overline{WE}$	Active-Low Write-Enable Input
32	5	V_{CC}	Power-Supply Input
—	1	N.C.	No Connection
—	4	$\overline{RST}$	Active-Low Power-On Reset Output
—	(See *Pin Configuration)*	X1, X2	Crystal Input, Output Connections
—	(See *Pin Configuration*)	V_{BAT}	Battery Connection

ORDERING INFORMATION

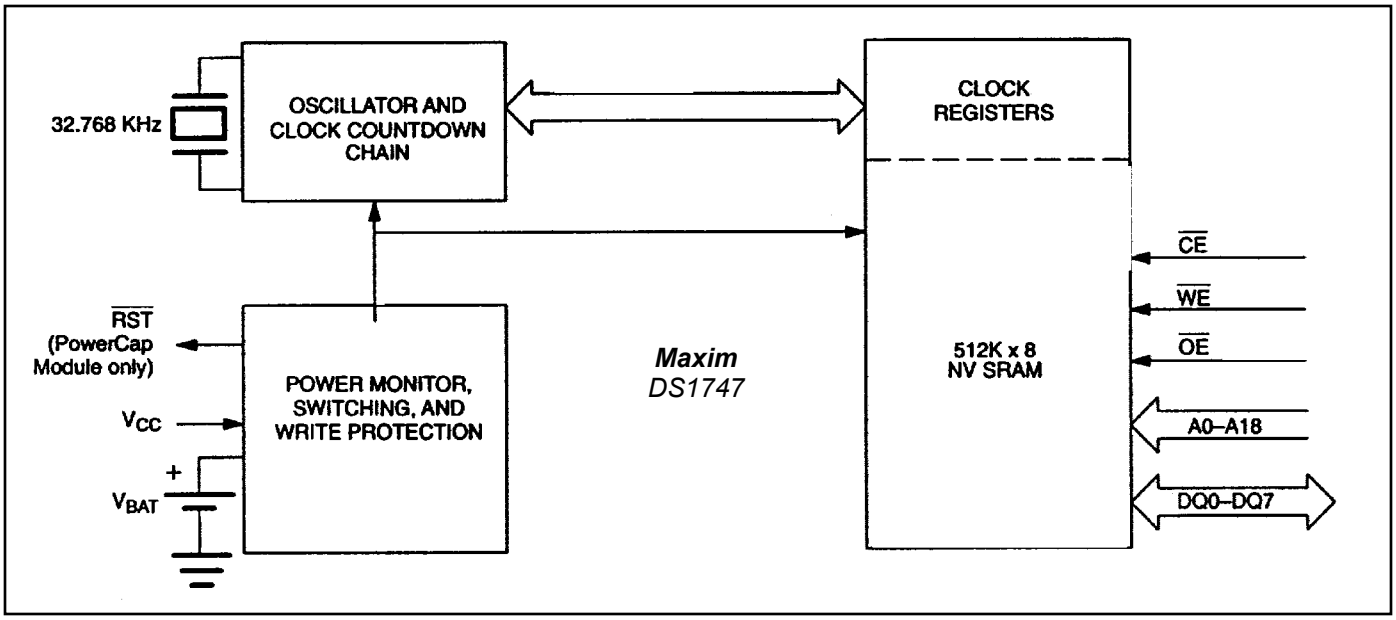
PART	SUPPLY VOLTAGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK†
DS1747-70+	5.0	0°C to +70°C	32 EDIP (0.740a)	DS1747-70+
DS1747-70IND+	5.0	-40°C to +85°C	32 EDIP (0.740a)	DS1747-70IND+
DS1747P-70+	5.0	0°C to +70°C	34 PowerCap*	DS1747P+70
DS1747P-70IND+	5.0	-40°C to +85°C	34 PowerCap*	DS1747P+70 IND
DS1747W-120+	3.3	0°C to +70°C	32 EDIP (0.740a)	DS1747W-120+
DS1747W-120IND+	3.3	-40°C to +85°C	32 EDIP (0.740a)	DS1747W-120IND+
DS1747WP-120+	3.3	0°C to +70°C	34 PowerCap*	DS1747WP+120
DS1747WP-120IND+	3.3	-40°C to +85°C	34 PowerCap*	DS1747WP+120 IND

+Denotes a lead(Pb)-free/RoHS-compliant package.
**DS9034PCX+ or DS9034I-PCX+ required (must be ordered separately).*
†A "+" indicates lead(Pb)-free. The top mark will include a "+" symbol on lead(Pb)-free devices.

DESCRIPTION

The DS1747 is a full-function, year-2000-compliant (Y2KC), real-time clock/calendar (RTC) and 512k x 8 nonvolatile static RAM. User access to all registers within the DS1747 is accomplished with a byte-wide interface as shown in Figure 1. The RTC information and control bits reside in the eight uppermost RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour binary-coded decimal (BCD) format. Corrections for the date of each month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1747 also contains its own power-fail circuitry that deselects the device when the V_{CC} supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

Figure 1. Block Diagram



PACKAGES

The DS1747 is available in two packages (32-pin DIP and 34-pin PowerCap module). The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the Power-Cap to be mounted on top of the DS1747P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers.

TIME AND DATE OPERATIONS

The contents of the time and date registers are in BCD format. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1747 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a one is written into the read bit, bit 6 of the century register (see Table 2). As long as a one remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All the DS1747 registers are updated simultaneously after the internal clock register updating process has been re-enabled. Updating is within a second after the read bit is written to zero. The READ bit must be set to a zero for a minimum of 500µs to ensure the external registers will be updated.

Table 1. Truth Table

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
$V_{CC}>V_{PF}$	V_{IH}	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
$V_{SO}<V_{CC}<V_{PF}$	X	X	X	Deselect	High-Z	CMOS Standby
$V_{CC}<V_{SO}<V_{PF}$	X	X	X	Deselect	High-Z	Data-Retention Mode

SETTING THE CLOCK

As shown in Table 2, bit 7 of the Control register is the W (write) bit. Setting the W bit to 1 halts updates to the device registers. The user can subsequently load correct date and time values into all eight registers, followed by a write cycle of 00h to the Control register to clear the W bit and transfer those new settings into the clock, allowing timekeeping operations to resume from the new set point.

Again referring to Table 2, bit 6 of the Control register is the R (read) bit. Setting the R bit to 1 halts updates to the device registers. The user can subsequently read the date and time values from the eight registers without those contents possibly changing during those I/O operations. A subsequent write cycle of 00h to the Control register to clear the R bit allows timekeeping operations to resume from the previous set point.

The pre-existing contents of the Control register bits 0:5 (Century value) are ignored/unmodified by a write cycle to Control if either the W or R bits are being set to 1 in that write operation.

The pre-existing contents of the Control register bits 0:5 (Century value) will be modified by a write cycle to Control if the W bit is being cleared to 0 in that write operation.

The pre-existing contents of the Control register bits 0:5 (Century value) will not be modified by a write cycle to Control if the R bit is being cleared to 0 in that write operation.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB (bit 7) of the seconds registers, see Table 2. Setting it to a one stops the oscillator.

FREQUENCY TEST BIT

As shown in Table 2, bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic “1” and the oscillator is running, the LSB of the seconds register will toggle at 512Hz. When the seconds register is being read, the DQ0 line will toggle at the 512Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, $\overline{WE}$ high, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The DS1747 is guaranteed to keep time accuracy to within ±1 minute per month at +25°C. The RTC is calibrated at the factory by Maxim using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. The

electrical environment also affects the clock accuracy, and caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, refer to *Application Note 58*.

CLOCK ACCURACY (PowerCap MODULE)

The DS1747 and DS9034PCX are each individually tested for accuracy. Once mounted together, the module typically keeps time accuracy to within ±1.53 minutes per month (35 ppm) at +25°C. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest-level EMI section of the PC board layout. For additional information, refer to *Application Note 58*.

Table 2. Register Map

ADDRESS	DATA								FUNCTION	RANGE
	B7	B6	B5	B4	B3	B2	B1	B0		
7FFFF	10 Year				Year				Year	00-99
7FFFE	X	X	X	10 Month	Month				Month	01-12
7FFFD	X	X	10 Date		Date				Date	01-31
7FFFC	BF	FT	X	X	X	Day			Day	01-07
7FFFB	X	X	10 Hour		Hour				Hour	00-23
7FFFA	X	10 Minutes			Minutes				Minutes	00-59
7FFF9	$\overline{OSC}$	10 Seconds			Seconds				Seconds	00-59
7FFF8	W	R	10 Century		Century				Century	00-39

$\overline{OSC}$ = Stop Bit R = Read Bit FT = Frequency Test

W = Write Bit X = See Note BF = Battery Flag

Note: *All indicated "X" bits are unused, but must be set to "0" during write cycles to ensure proper clock operation.*

RETRIEVING DATA FROM RAM OR CLOCK

The DS1747 is in the read mode whenever $\overline{OE}$ (output enable) is low, $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times and states are not met, valid data will be available at the latter of chip-enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1747 is in the write mode whenever $\overline{WE}$, and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the output t_{WEZ} after $\overline{WE}$ goes active.

DATA-RETENTION MODE

The 5V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. However, when V_{CC} is below the power failing point, V_{PF}, (point at which write protection occurs) the internal clock registers and SRAM are blocked from any access. At this time the power fail reset output signal ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the battery switch point V_{SO} (battery supply level), device power is switched from the V_{CC} pin to the backup battery. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. The 3.3V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. When V_{CC} falls below the power fail point, V_{PF}, access to the device is inhibited. At this time the power fail reset output signal ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. If V_{PF} is less than V_{SO}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than Vso, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{SO}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels. The $\overline{RST}$ signal is an open drain output and requires a pull up. Except for the $\overline{RST}$, all control, data, and address signals must be powered down when V_{CC} is powered down.

BATTERY LONGEVITY

The DS1747 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1747 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1747 is shipped from Maxim with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1747 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

BATTERY MONITOR

The DS1747 constantly monitors the battery voltage of the internal battery. The Battery Flag bit (bit 7) of the day register is used to indicate the voltage level range of the battery. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted lithium energy source is indicated and both the contents of the RTC and RAM are questionable.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground
- 5.5V Version……-0.3V to +6.0V
- 3.3V Version……-0.3V to +4.6V

Operating Temperature Range (Noncondensing)
- Commercial……0°C to +70°C
- Industrial……-40°C to +85°C

Storage Temperature Range
- EDIP ……-40°C to +85°C
- PowerCap ……-55°C to +125°C

Lead Temperature (soldering, 10s)……+260°C
- **Note:** EDIP is hand or wave-soldered only.

Soldering Temperature (reflow, PowerCap) ……+260°C

This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = Over the Operating Range)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage All Inputs	V_{CC} = 5V±10%	V_{IH}	2.2		V_{CC} + 0.3V	V	1
	V_{CC} = 3.3V±10%	V_{IH}	2.0		V_{CC} + 0.3V	V	1
Logic 0 Voltage All Inputs	V_{CC} = 5V±10%	V_{IL}	-0.3		+0.8	V	1
	V_{CC} = 3.3V±10%	V_{IL}	-0.3		+0.6	V	1

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	Icc			85	mA	2, 3, 10
TTL Standby Current ($\overline{CE}$ = V_{IH})	Icc_1			6	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)	Icc_2			4	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25		4.50	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT}			1, 4

DC ELECTRICAL CHARACTERISTICS

(V_{CC} **= 3.3V ±10%**, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	Icc			30	mA	2, 3, 10
TTL Standby Current ($\overline{CE}$ = V_{IH})	Icc_1			2	mA	2, 3
CMOS Standby Current ($\overline{CE}$ ≥ V_{CC} - 0.2V)	Icc_2			2	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	2.80		2.97	V	1
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	1, 4

AC CHARACTERISTICS—READ CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

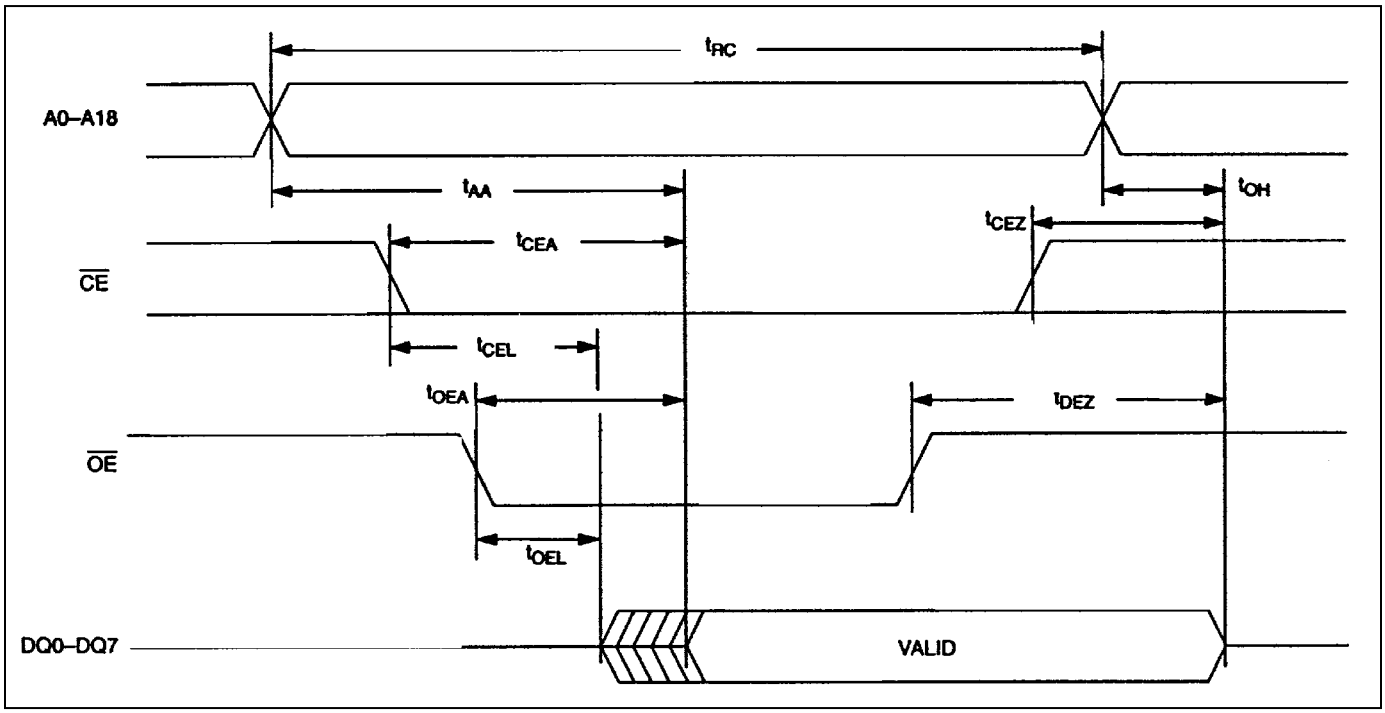
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70			ns	
Address Access Time	t_{AA}			70	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ Access Time	t_{CEA}			70	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			25	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			35	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			25	ns	
Output Hold from Address	t_{OH}	5			ns	

AC CHARACTERISTICS—READ CYCLE (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
Address Access Time	t_{AA}			120	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5			ns	
$\overline{CE}$ Access Time	t_{CEA}			120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}			40	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5			ns	
$\overline{OE}$ Access Time	t_{OEA}			100	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}			35	ns	
Output Hold from Address	t_{OH}	5			ns	

READ CYCLE TIMING DIAGRAM



AC CHARACTERISTICS—WRITE CYCLE (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

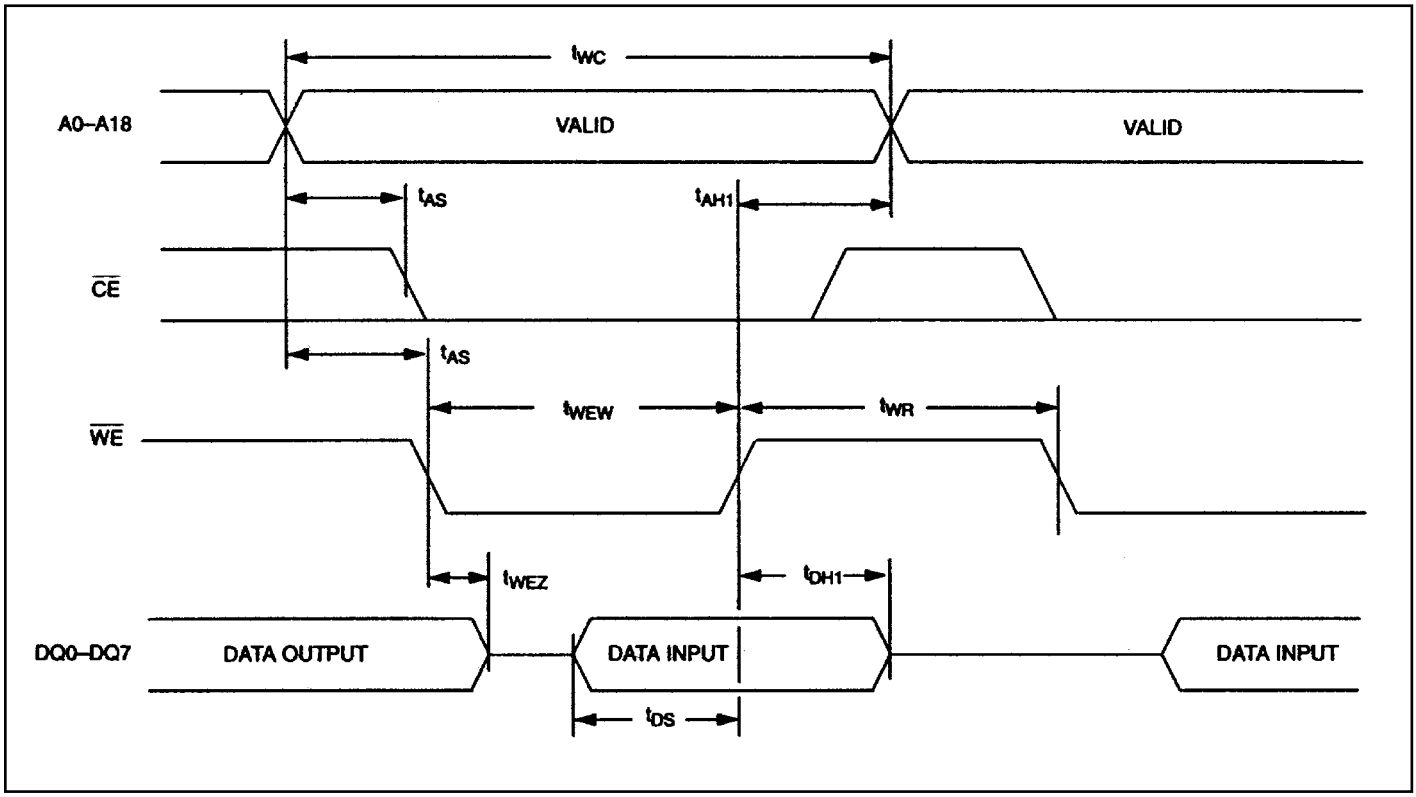
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	70			ns	
Address Setup Time	t_{AS}	0			ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60			ns	
Data Setup Time	t_{DS}	30			ns	
Data Hold Time	t_{DH1}	0			ns	8
Data Hold Time	t_{DH2}	0			ns	9
Address Hold Time	t_{AH1}	5			ns	8
Address Hold Time	t_{AH2}	5			ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}			25	ns	
Write Recovery Time	t_{WR}	5			ns	

AC CHARACTERISTICS—WRITE CYCLE (3.3V)

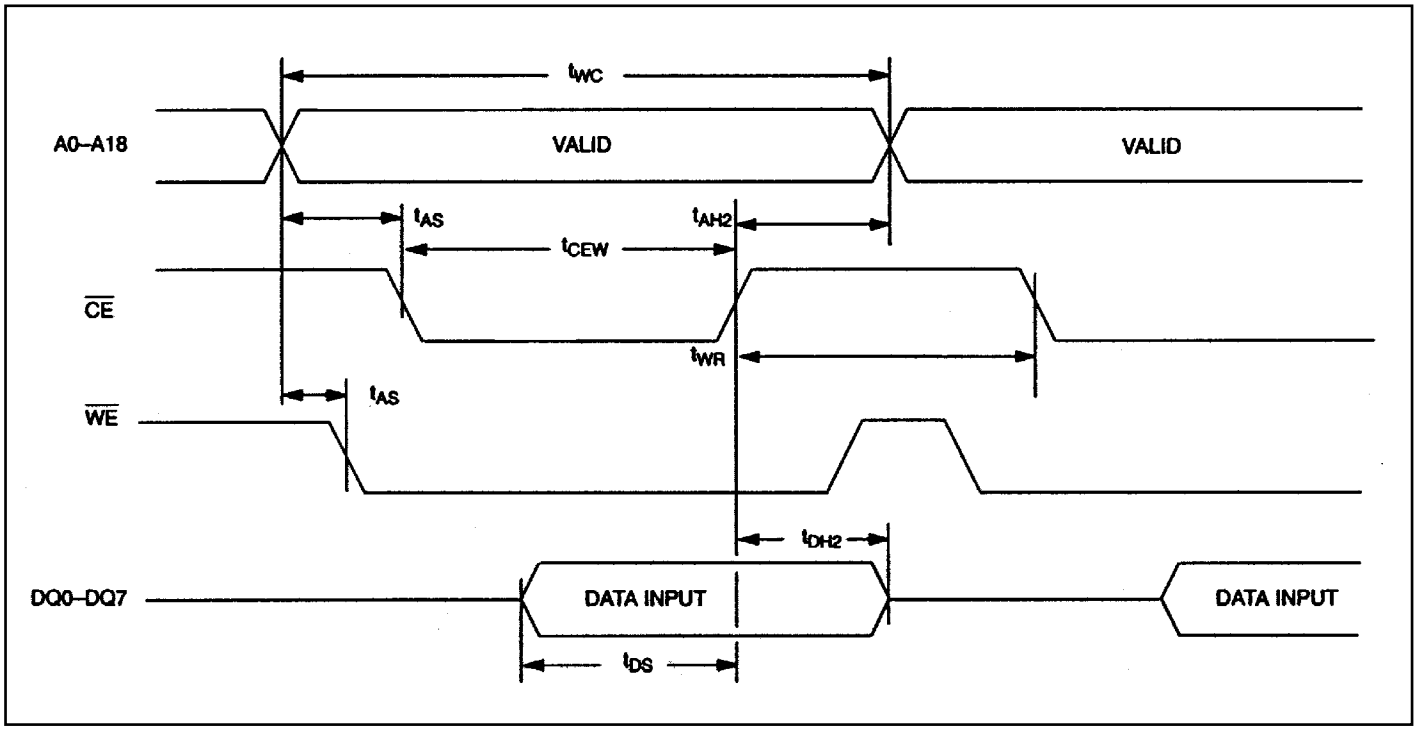
(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write Cycle Time	t_{WC}	120			ns	
Address Setup Time	t_{AS}	0		120	ns	
$\overline{WE}$ Pulse Width	t_{WEW}	100			ns	
$\overline{CE}$ Pulse Width	t_{CEW}	110			ns	
Data Setup Time	t_{DS}	80			ns	
Data Hold Time	t_{DH1}	0			ns	8
Data Hold Time	t_{DH2}	0			ns	9
Address Hold Time	t_{AH1}	0			ns	8
Address Hold Time	t_{AH2}	10			ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}			40	ns	
Write Recovery Time	t_{WR}	10			ns	

WRITE CYCLE TIMING DIAGRAM, WRITE-ENABLE CONTROLLED



WRITE CYCLE TIMING DIAGRAM, CHIP-ENABLE CONTROLLED

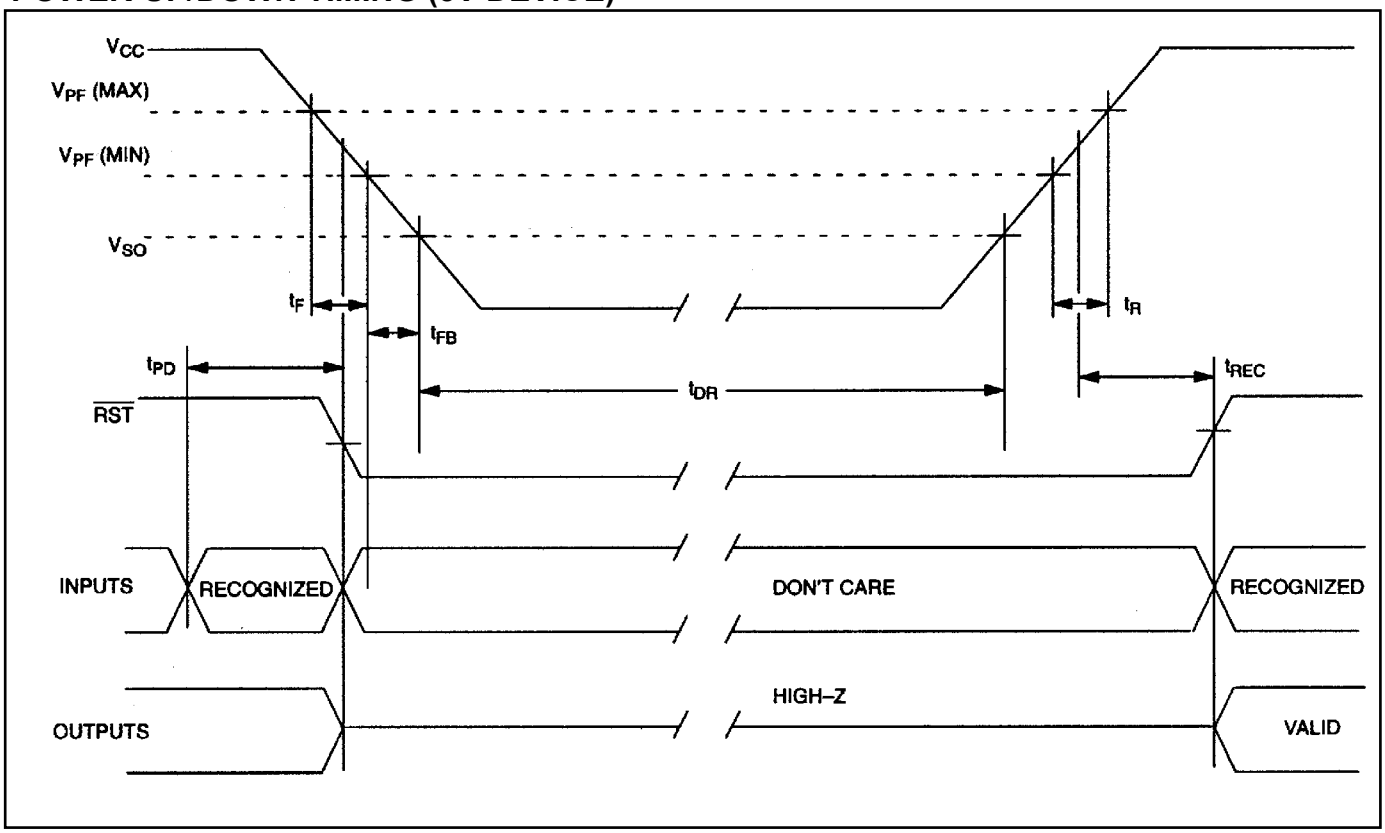


POWER-UP/DOWN AC CHARACTERISTICS (5V)

(V_{CC} = 5.0V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_H Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$) to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time VPF to $\overline{RST}$ High (PowerCap Only)	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator ON)	t_{DR}	10			years	5, 6

POWER-UP/DOWN TIMING (5V DEVICE)

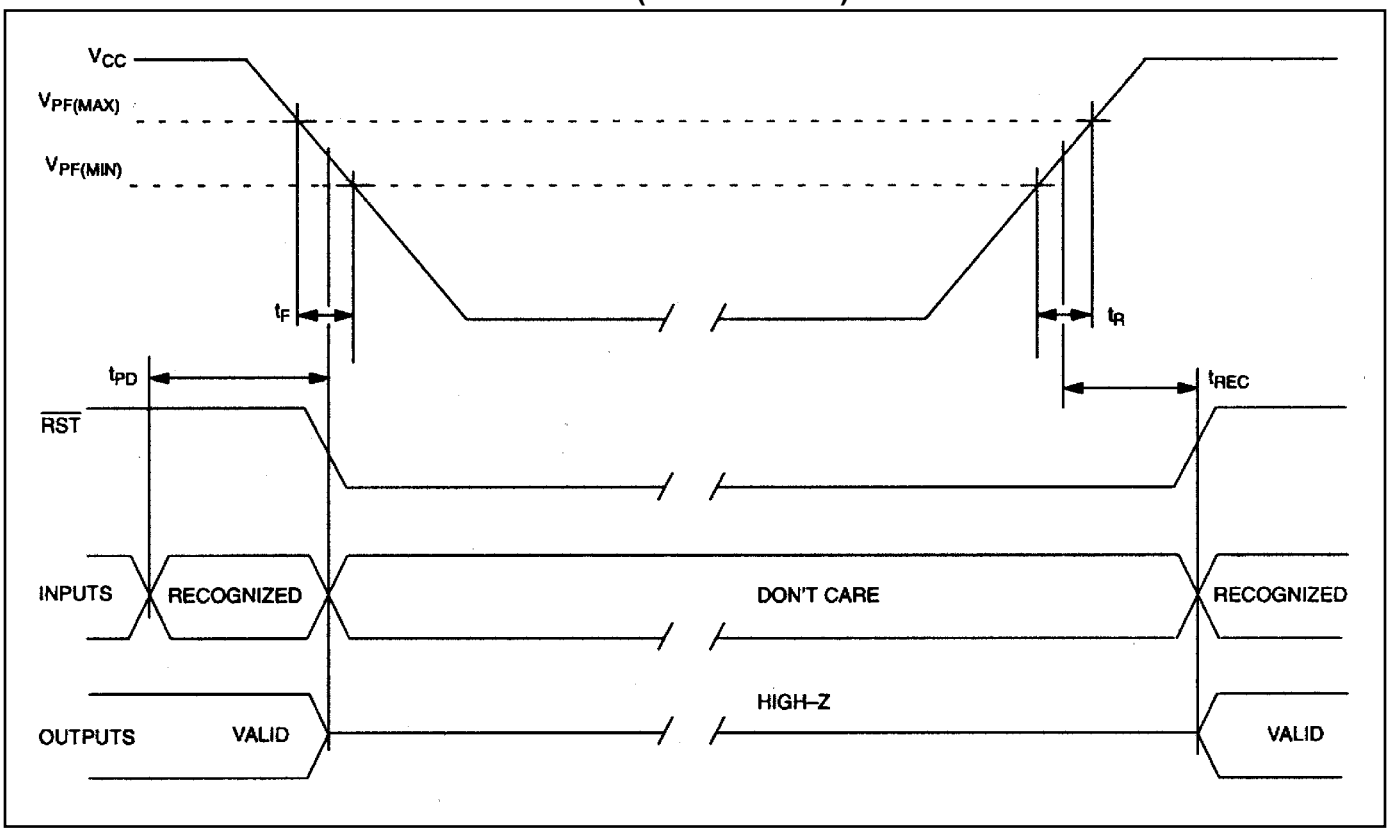


POWER-UP/DOWN CHARACTERISTICS (3.3V)

(V_{CC} = 3.3V ±10%, T_A = Over the Operating Range.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_H, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time V_{PF} to $\overline{RST}$ High (PowerCap Only)	t_{REC}			35	ms	
Expected Data-Retention Time (Oscillator ON)	t_{DR}	10			years	5, 6

POWER-UP/DOWN WAVEFORM TIMING (3.3V DEVICE)



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Input Pins	C_{IN}			14	pF	
Capacitance on All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 50 pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltages are referenced to ground.

2) Typical values are at +25°C and nominal supplies.

3) Outputs are open.

4) Battery switchover occurs at the lower of either the battery terminal voltage or V_{PF}.

5) Data-retention time is at +25°C.

6) Each DS1747 has a built-in switch that disconnects the lithium source until the user first applies V_{CC}. The expected t_{DR} is defined for DIP modules and assembled PowerCap modules as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

7) RTC encapsulated DIP (EDIP) modules can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultra-sonic vibration is not used.

   See the PowerCap package outline drawing for details regarding the PowerCap package.

8) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.

9) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.

10) t_{WC} = 200ns.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 EDIP	MDT32+4	**21-0245**	—
34 PWRCP	PC2+1	**21-0246**	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
9/10	Updated the *Ordering Information* table top mark information and removed leaded parts; updated the *Absolute Maximum Ratings* section to include the storage temperature range and lead and soldering temperatures for EDIP and PowerCap packages; added Note 10 to the I_{CC} parameter in the *DC Electrical Characteristics* tables (for 5.0V and 3.3V) and the *Notes* section; updated the *Package Information* table	3, 8, 9, 15
3/12	Updated the *Absolute Maximum Ratings* section to add the 5V and 3.3V voltage range	8
6/13	Replaced the *Setting the Clock* section	5

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