Si530/531

REVISION D

CRYSTAL OSCILLATOR (XO) (10 MHZ TO 1.4 GHZ)

Features

- Available with any-rate output frequencies from 10 MHz to 945 MHz and select frequencies to 1.4 GHz
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

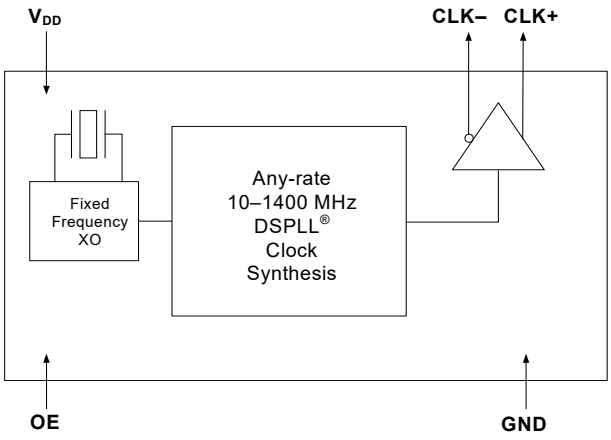
Applications

- SONET/SDH
- Networking
- SD/HD video
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clock generation

Description

The Si530/531 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low jitter clock at high frequencies. The Si530/531 is available with any-rate output frequency from 10 to 945 MHz and select frequencies to 1400 MHz. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si530/531 uses one fixed crystal to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si530/531 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage, output format, and temperature stability. Specific configurations are factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

Functional Block Diagram



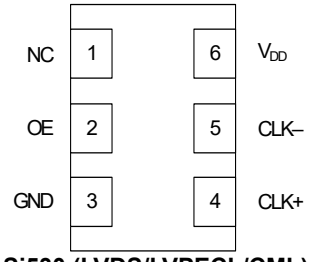
Ordering Information:

See page 7.

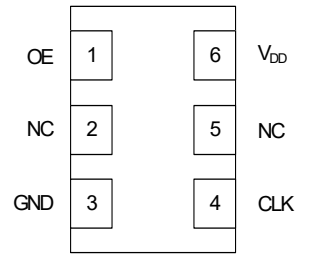
Pin Assignments:

See page 6.

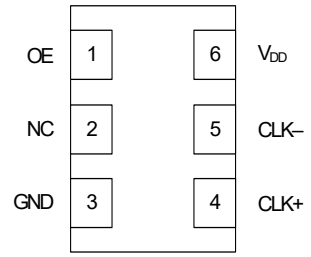
(Top View)



Si530 (LVDS/LVPECL/CML)



Si530 (CMOS)



Si531 (LVDS/LVPECL/CML)

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	I_{DD}	Output enabled LVPECL CML LVDS CMOS	 — — — —	 111 99 90 81	 121 108 98 88	mA
		Tristate mode	—	60	75	mA
Output Enable (OE)[2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	V
Operating Temperature Range	T_A		–40	—	85	ºC

Notes:
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 7 for further details.
2. OE pin includes a 17 kΩ pullup resistor to V_{DD}.

Table 2. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Frequency[1,2]	f_O	LVPECL/LVDS/CML	10	—	945	MHz
		CMOS	10	—	160	MHz
Initial Accuracy	f_i	Measured at +25 °C at time of shipping	—	±1.5	—	ppm
Temperature Stability[1,3]			–7 –20 –50	— — —	+7 +20 +50	ppm
Aging	f_a	Frequency drift over first year	—	—	±3	ppm
		Frequency drift over 20 year life	—	—	±10	ppm

Notes:
1. See Section 3. "Ordering Information" on page 7 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Selectable parameter specified by part number.
4. Time from powerup or tristate mode to f_O.

Table 2. CLK± Output Frequency Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Stability		Temp stability = ±7 ppm	—	—	±20	ppm
		Temp stability = ±20 ppm	—	—	±31.5	ppm
		Temp stability = ±50 ppm	—	—	±61.5	ppm
Powerup Time[4]	t_{OSC}		—	—	10	ms

Notes:
1. See Section 3. "Ordering Information" on page 7 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Selectable parameter specified by part number.
4. Time from powerup or tristate mode to f_O.

Table 3. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	2.5/3.3 V option mid-level	—	V_{DD} – 1.30	—	V
		1.8 V option mid-level	—	V_{DD} – 0.36	—	V
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	V_{PP}
CMOS Output Option[3]	V_{OH}	I_{OH} = 32 mA	0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}	I_{OL} = 32 mA	—	—	0.4	V
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V_{DD}/2	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF

Table 4. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Jitter (RMS)[1] for $F_{OUT} \geq$ 500 MHz	ϕ_J	12 kHz to 20 MHz (OC-48)	—	0.25	0.40	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	0.37	ps
Phase Jitter (RMS)[1] for F_{OUT} of 125 to 500 MHz	ϕ_J	12 kHz to 20 MHz (OC-48)	—	0.36	0.50	ps
		50 kHz to 80 MHz (OC-192)[2]	—	0.34	0.42	ps
Phase Jitter (RMS) for F_{OUT} of 10 to 160 MHz CMOS Output Only	ϕ_J	12 kHz to 20 MHz (OC-48)[2]	—	0.62	—	ps
		50 kHz to 20 MHz[2]	—	0.61	—	ps

Notes:
1. Refer to AN256 for further information.
2. Max offset frequencies: 80 MHz for FOUT $\geq$ 250 MHz, 20 MHz for 50 MHz $\leq$ FOUT <250 MHz, 2 MHz for 10 MHz $\leq$ FOUT <50 MHz.

Table 5. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Period Jitter*	J_{PER}	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	ps

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

Table 6. CLK± Output Phase Noise (Typical)

Offset Frequency (f)	120.00 MHz LVDS	156.25 MHz LVPECL	622.08 MHz LVPECL	Unit
100 Hz	–112	–105	–97	dBc/Hz
1 kHz	–122	–122	–107	
10 kHz	–132	–128	–116	
100 kHz	–137	–135	–121	
1 MHz	–144	–144	–134	
10 MHz	–150	–147	–146	
100 MHz	n/a	n/a	–148	

Table 7. Environmental Compliance

The Si530/531 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross & Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	J-STD-020, MSL1
Contact Pads	Gold over Nickel

Table 8. Thermal Characteristics

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	—	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	—	°C/W
Ambient Temperature	T_A		–40	—	85	°C
Junction Temperature	T_J		—	—	125	°C

Table 9. Absolute Maximum Ratings[1]

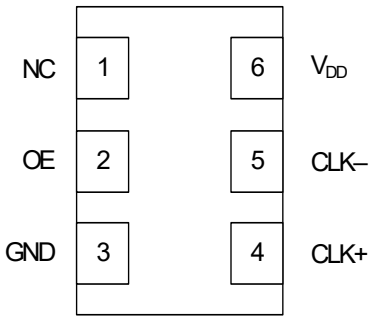
Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T_{AMAX}	85	ºC
Supply Voltage, 1.8 V Option	V_{DD}	–0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V_{DD}	–0.5 to +3.8	V
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	V
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	20–40	seconds

Notes:

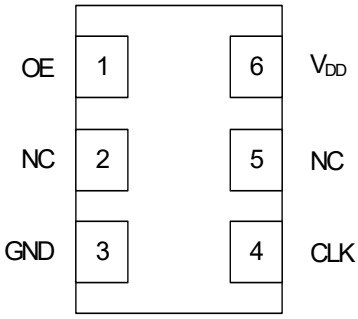
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

2. Pin Descriptions

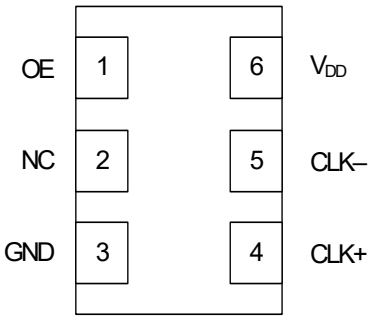
(Top View)



Si530
LVDS/LVPECL/CML



Si530
CMOS



Si531
LVDS/LVPECL/CML

Table 10. Pinout for Si530 Series

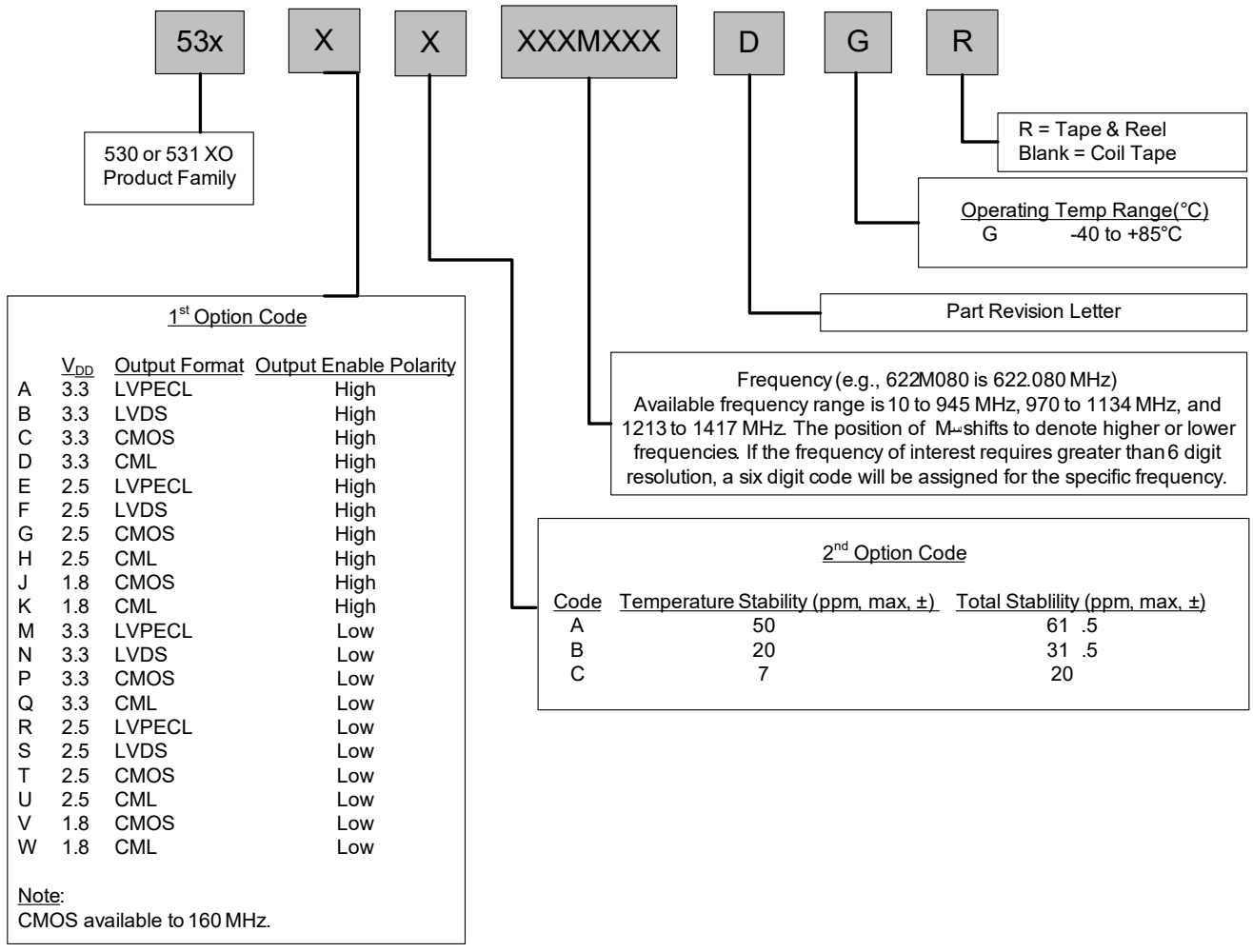
Pin	Symbol	LVDS/LVPECL/CML Function	CMOS Function
1	OE (CMOS only)*	No connection	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled
2	OE (LVPECL,LVDS, CML)*	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled	No connection
3	GND	Electrical and Case Ground	Electrical and Case Ground
4	CLK+	Oscillator Output	Oscillator Output
5	CLK–	Complementary Output	No connection
6	V_{DD}	Power Supply Voltage	Power Supply Voltage
***Note:** OE includes a 17 kΩ pullup resistor to V_{DD}.			

Table 11. Pinout for Si531 Series

Pin	Symbol	LVDS/LVPECL/CML Function
1	OE (LVPECL, LVDS, CML)*	Output enable 0 = clock output disabled (outputs tristated) 1 = clock output enabled
2	No connection	No connection
3	GND	Electrical and Case Ground
4	CLK+	Oscillator Output
5	CLK–	Complementary output
6	V_{DD}	Power Supply Voltage
***Note:** OE includes a 17 kΩ pullup resistor to V_{DD}.		

3. Ordering Information

The Si530/531 XO supports a variety of options including frequency, temperature stability, output format, and V_{DD}. Specific device configurations are programmed into the Si530/531 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Laboratories provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si530 and Si531 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm package. The Si531 Series supports an alternate OE pinout (pin #1) for the LVPECL, LVDS, and CML output formats. See Tables 10 and 11 for the pinout differences between the Si530 and Si531 series.



Example P/N: 530AB622M080DGR is a 5 x 7 XO in a 6 pad package. The frequency is 622.080 MHz, with a 3.3 V supply, LVPECL output and Output Enable active high polarity. Temperature stability is specifed as ±20 ppm. The part is specified for –40 to +85 °C ambient temperature range operation and is shipped in tape and reel format

Figure 1. Part Number Convention

4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si530/531. Table 12 lists the values for the dimensions shown in the illustration.

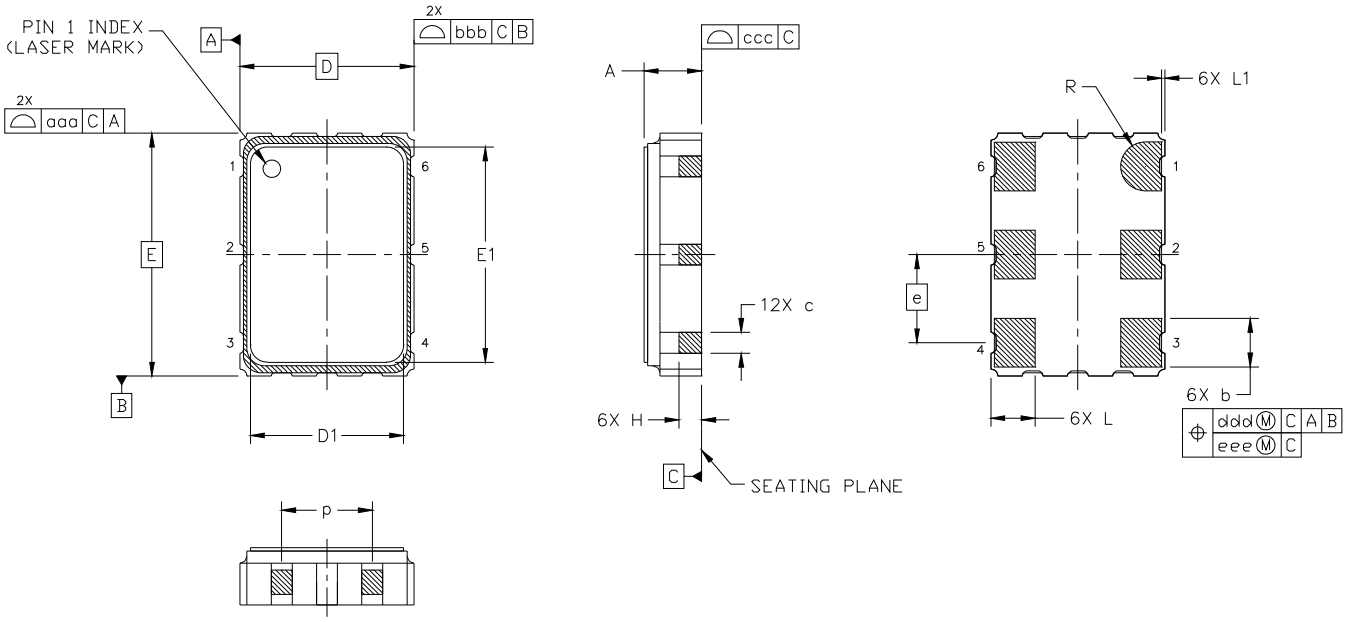


Figure 2. Si530/531 Outline Diagram

Table 12. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC	
E		7.00 BSC	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	1.80	—	2.60
R		0.70 REF	
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5. Si530/Si531 Mark Specification

Figure 3 illustrates the mark specification for the Si530/Si531. Table 13 lists the line information.

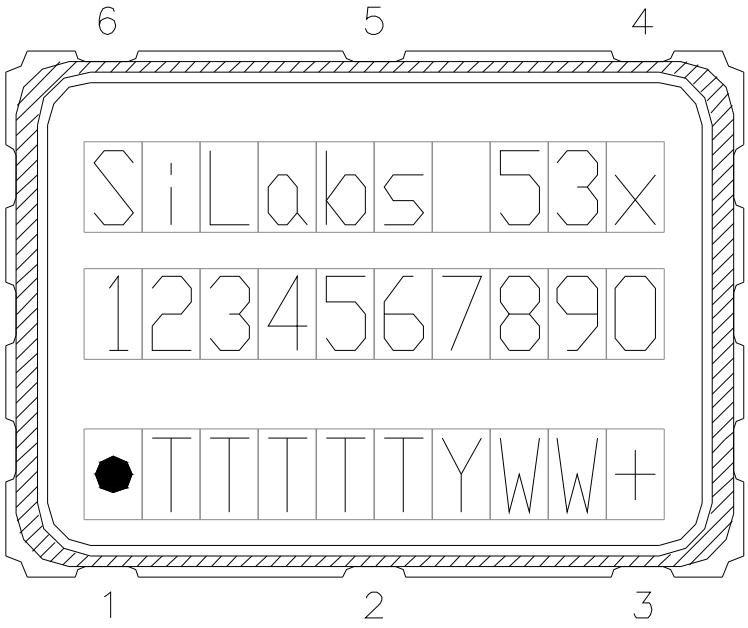


Figure 3. Mark Specification

Table 13. Si53x Top Mark Description

Line	Position	Description
1	1–10	“SiLabs"+ Part Family Number, 53x (First 3 characters in part number where x = 0 indicates a 530 device and x = 1 indicates a 531 device).
2	1–10	Si530, Si531: Option1 + Option2 + Freq(7) + Temp Si532, Si533, Si534, Si530/Si531 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si530/531. Table 14 lists the values for the dimensions shown in the illustration.

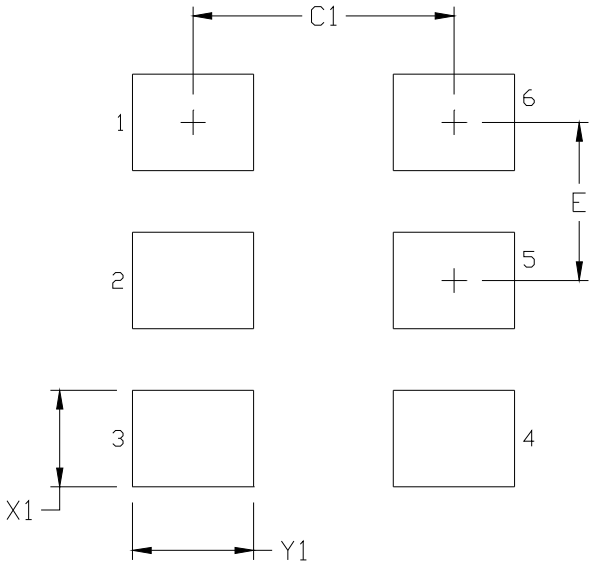


Figure 4. Si530/531 PCB Land Pattern

Table 14. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Document Change List

Revision 0.4 to Revision 0.5

- Updated Table 1, “Recommended Operating Conditions,” on page 2.
  - Added maximum supply current specifications.
  - Specified relationship between temperature at startup and operation temperature.
- Updated Table 4, “CLK± Output Phase Jitter,” on page 4 to include maximum rms jitter generation specifications and updated typical rms jitter specifications.
- Added Table 6, “CLK± Output Phase Noise (Typical),” on page 4.
- Added Output Enable active polarity as an option in Figure 1, “Part Number Convention,” on page 7.

Revision 0.5 to Revision 1.0

- Updated Note 3 in Table 1, “Recommended Operating Conditions,” on page 2.
- Updated Figure 1, “Part Number Convention,” on page 7.

Revision 1.0 to Revision 1.1

- Updated Table 1, “Recommended Operating Conditions,” on page 2.
  - Device maintains stable operation over –40 to +85 ºC operating temperature range.
  - Supply current specifications updated for revision D.
- Updated Table 2, “CLK± Output Frequency Characteristics,” on page 2.
  - Added specification for ±20 ppm lifetime stability (±7 ppm temperature stability) XO.
- Updated Table 3, “CLK± Output Levels and Symmetry,” on page 3.
  - Updated LVDS differential peak-peak swing specifications.
- Updated Table 4, “CLK± Output Phase Jitter,” on page 4.
- Updated Table 5, “CLK± Output Period Jitter,” on page 4.
  - Revised period jitter specifications.
- Updated Table 9, “Absolute Maximum Ratings[1],” on page 5 to reflect the soldering temperature time at 260 ºC is 20–40 sec per JEDEC J-STD-020C.
- Updated 3. "Ordering Information" on page 7.
  - Changed ordering instructions to revision D.
- Added 5. "Si530/Si531 Mark Specification" on page 9.

Revision 1.1 to Revision 1.2

- Updated 2.5 V/3.3 V and 1.8 V CML output level specifications for Table 3 on page 3.
- Added footnotes clarifying max offset frequency test conditions for Table 4 on page 4.
- Added CMOS phase jitter specs to Table 4 on page 4.
- Removed the words "Differential Modes: LVPECL/LVDS/CML" in the footnote referring to AN256 in Table 4 on page 4.
- Separated 1.8 V, 2.5 V/3.3 V supply voltage specifications in Table 9 on page 5.
- Updated and clarified Table 9 on page 5 to include the "Moisture Sensitivity Level" and "Contact Pads" rows.
- Updated Figure 3 on page 9 and Table 13 on page 9 to reflect specific marking information. Previously, Figure 3 was generic.

Revision 1.2 to Revision 1.3

- Added Table 8, “Thermal Characteristics,” on page 5.

Revision 1.3 to Revision 1.4

- Revised Figure 2 and Table 12 on page 8 to reflect current package outline diagram.
- Revised Figure 4 and Table 14 on page 10 to reflect the recommended PCB land pattern.

Revision 1.4 to Revision 1.5

- Changed “Trays” to “Coil Tape” in Ordering Guide.

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Silicon Laboratories Inc.
400 West Cesar Chavez
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