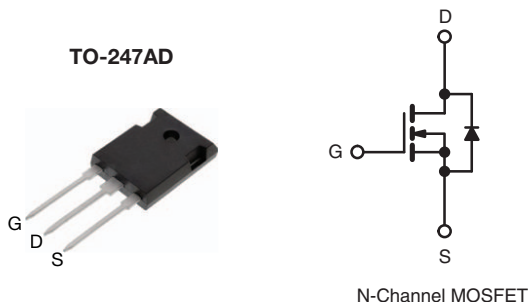


EF Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ typ. at 25 °C (Ω)	$V_{GS} = 10$ V	0.033
Q_g (Max.) (nC)	380	
Q_{gs} (nC)	62	
Q_{gd} (nC)	102	
Configuration	Single	



FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr} , Q_{rr} , and I_{RRM}
- Low figure-of-merit (FOM): $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Increased robustness due to low Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Lighting
 - High intensity discharge (HID)
 - Light emitting diodes (LEDs)
- Consumer and computing
 - ATX power supplies
- Industrial
 - Welding
 - Battery chargers
- Renewable energy
 - Solar (PV inverters)
- Switch mode power supplies (SMPS)
 - LLC
 - Phase shifted bridge (ZVS)
 - 3-level inverter
 - AC/DC bridge

ORDERING INFORMATION

Package	TO-247AD
Lead (Pb)-free and Halogen-free	SiHW70N60EF-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	229	
Linear Derating Factor		4.2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	1706	mJ
Maximum Power Dissipation	P_D	520	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	$T_J = 125$ °C	V/ns
Reverse Diode dV/dt ^d			
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DS} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 11$ A.
- 1.6 mm from case.
- $I_{SD} = 35$ A, $dI/dt = 600$ A/ μ s, $V_{DS} = 400$ V.

**THERMAL RESISTANCE RATINGS**

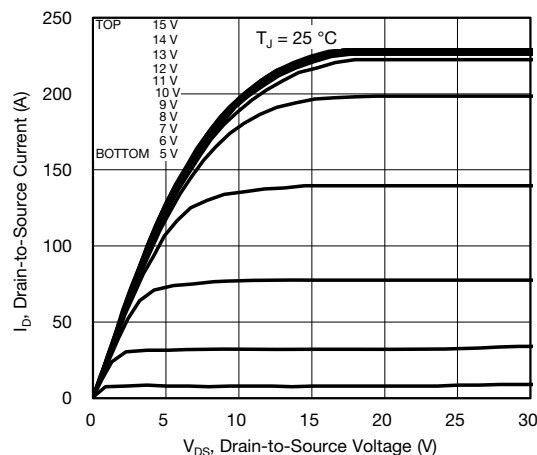
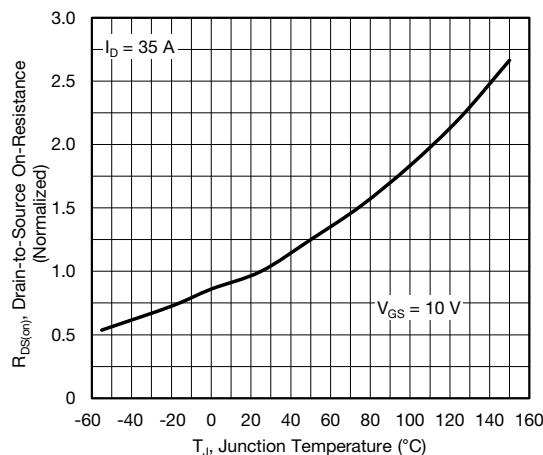
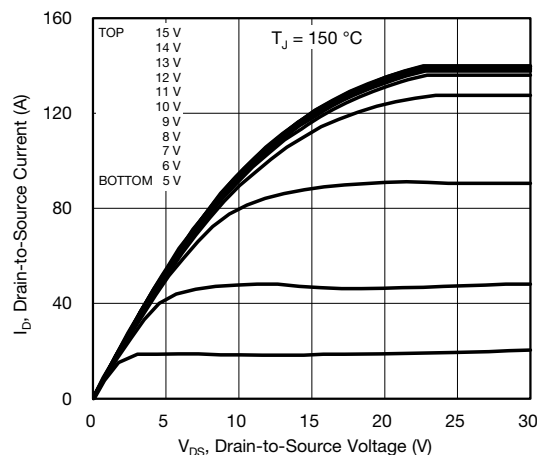
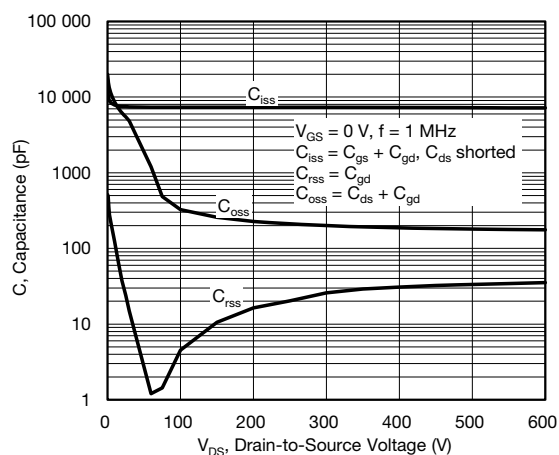
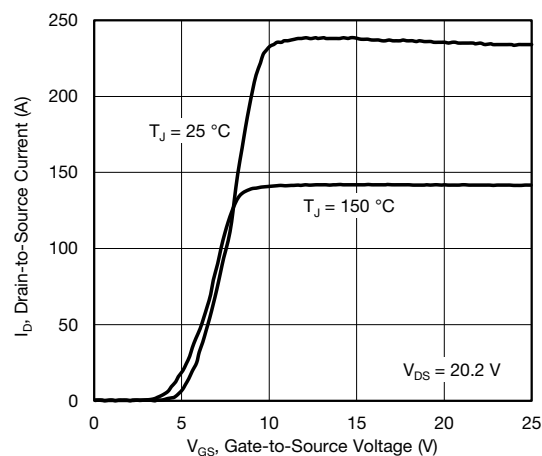
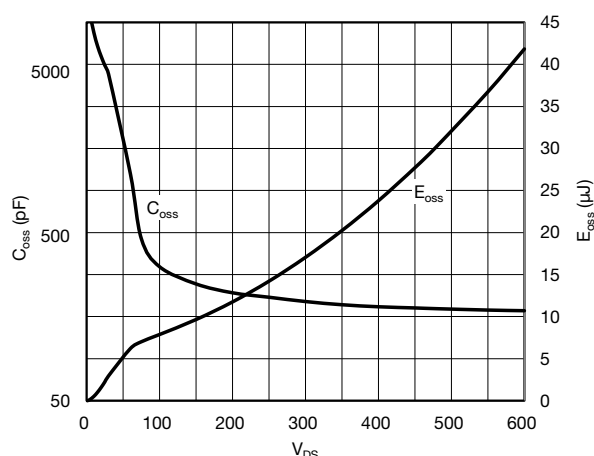
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.24	

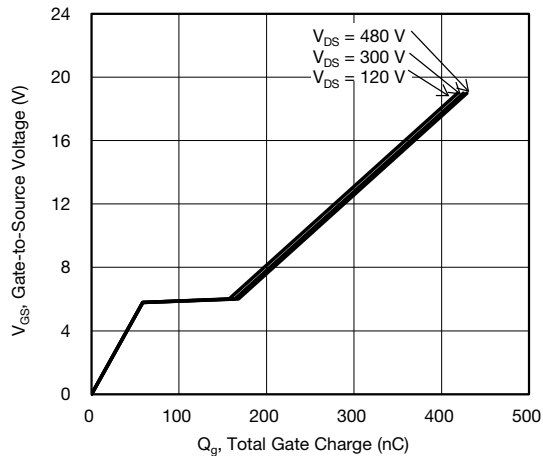
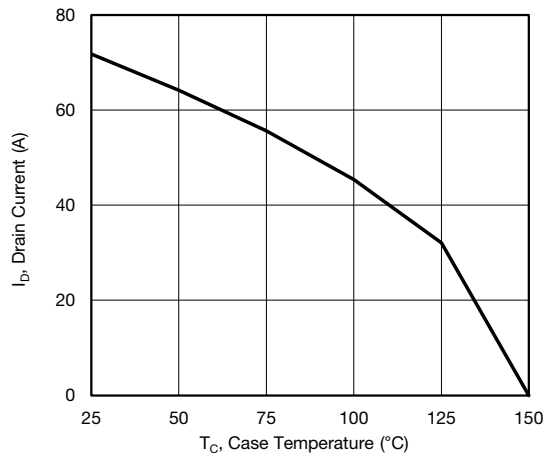
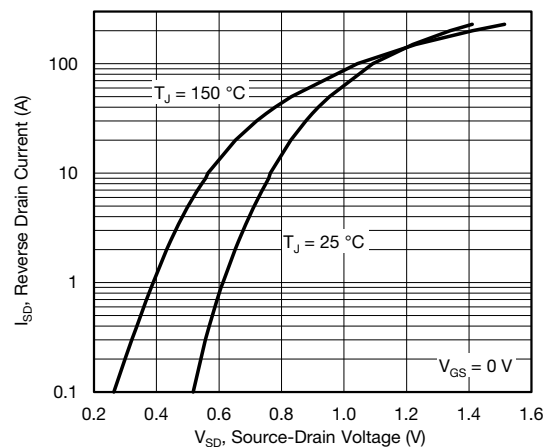
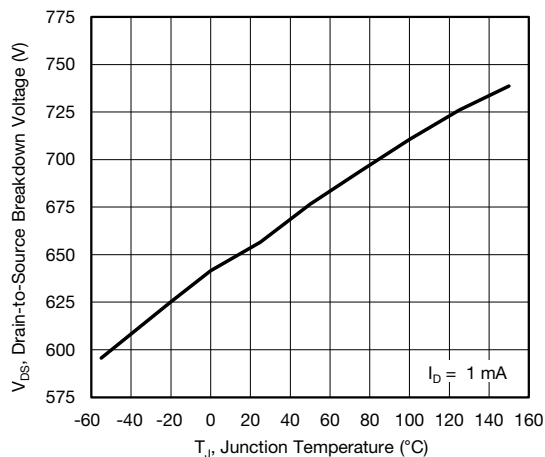
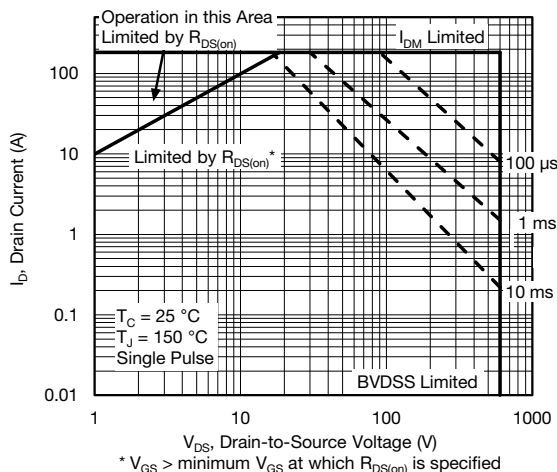
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

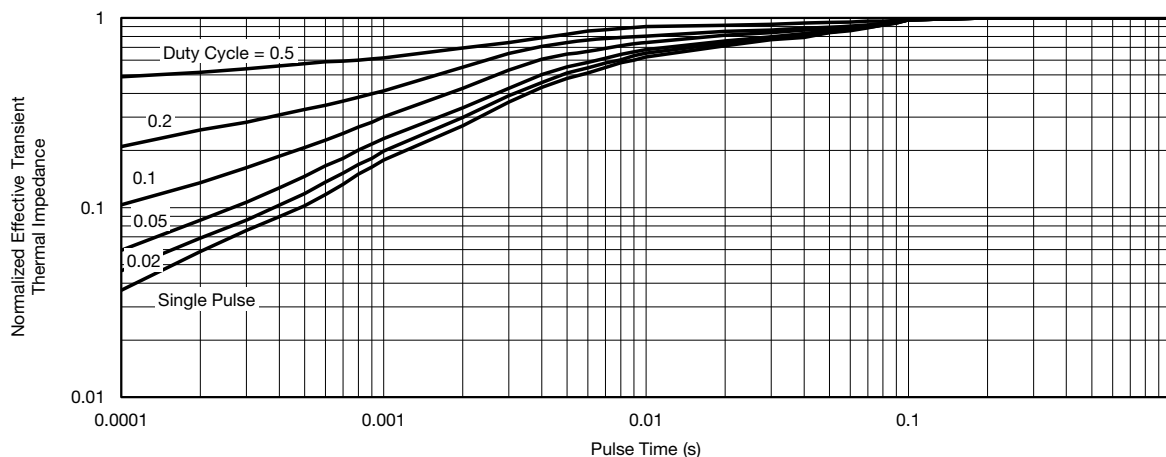
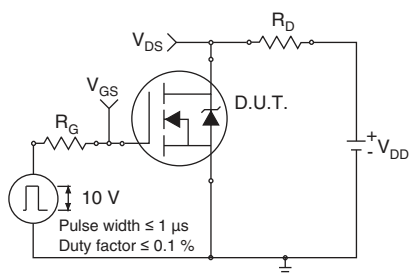
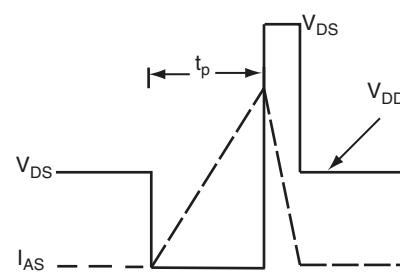
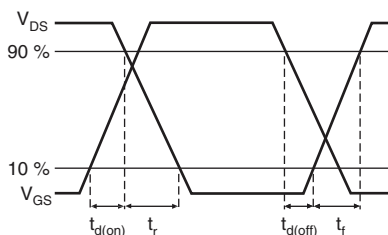
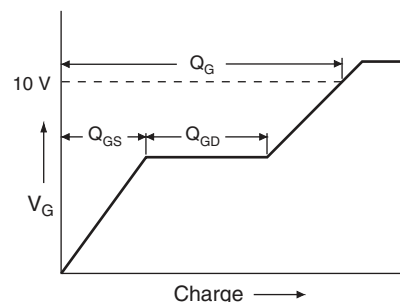
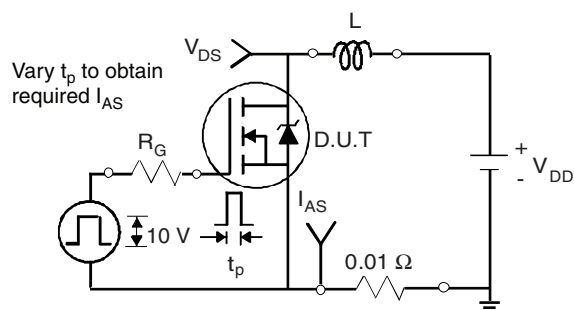
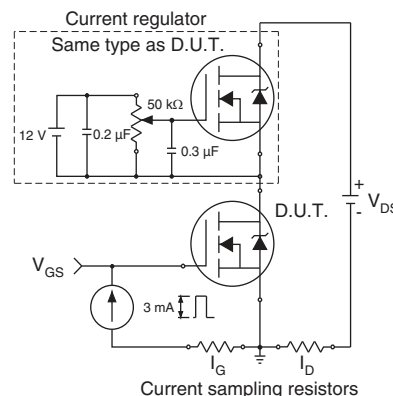
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.69	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	2	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 35\text{ A}$	-	0.033	0.038	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 35\text{ A}$	-	25	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	7500	-	pF
Output Capacitance	C_{oss}		-	378	-	
Reverse Transfer Capacitance	C_{rss}		-	5	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 480\text{ V}$	-	263	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$		-	926	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 35\text{ A}$, $V_{DS} = 480\text{ V}$	-	253	380	nC
Gate-Source Charge	Q_{gs}		-	62	-	
Gate-Drain Charge	Q_{gd}		-	102	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 35\text{ A}$ $R_g = 9.1\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	56	84	ns
Rise Time	t_r		-	107	161	
Turn-Off Delay Time	$t_{d(off)}$		-	257	386	
Fall Time	t_f		-	123	185	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	1.1	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	70	A
Pulsed Diode Forward Current	I_{SM}		-	-	229	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 35\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 35\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	-	213	426	ns
Reverse Recovery Charge	Q_{rr}		-	1.6	3.2	μC
Reverse Recovery Current	I_{RRM}		-	16	-	A

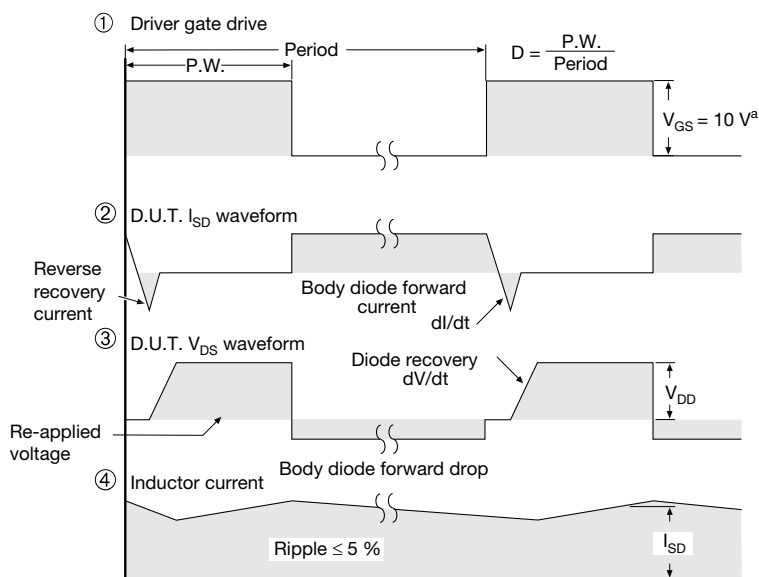
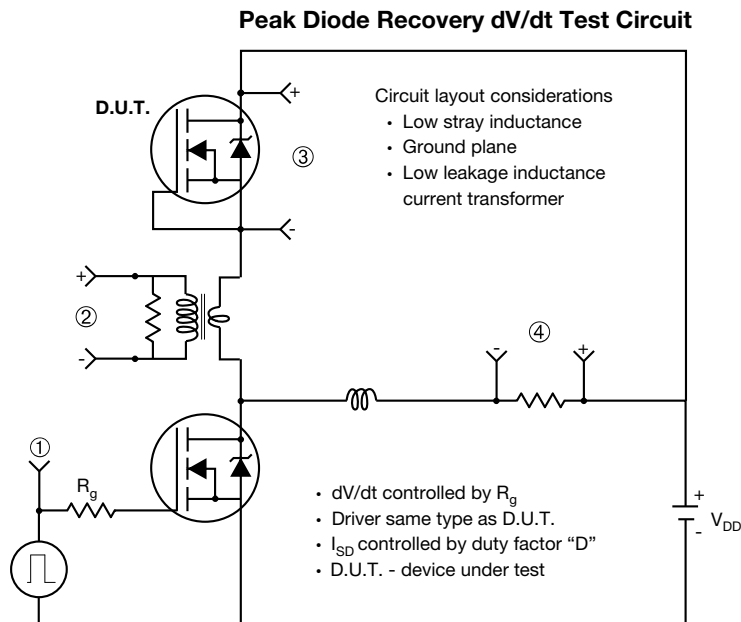
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit


Note

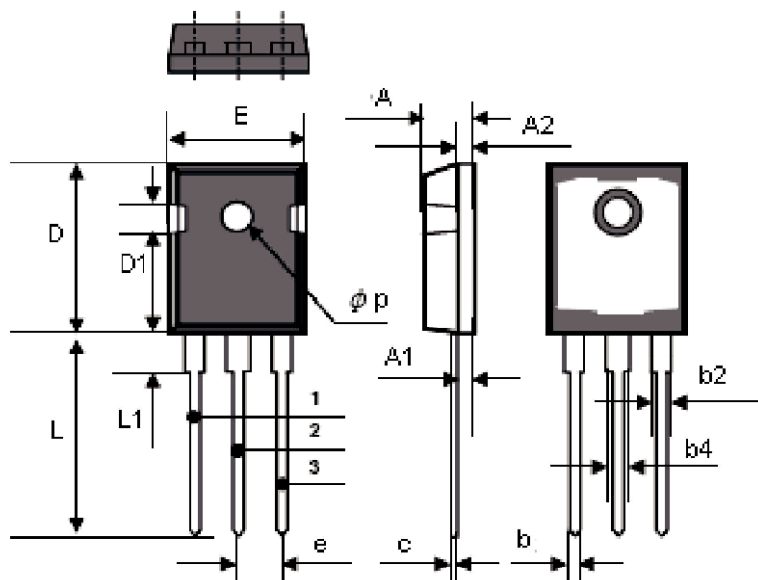
a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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TO-247AD (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.90	5.10	0.193	0.200
A1	2.30	2.40	0.090	0.094
A2	1.92	2.08	0.076	0.082
b	1.15	1.25	0.045	0.049
b2	1.95	2.05	0.077	0.081
b4	2.85	3.11	0.112	0.122
c	0.6 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	4.37	4.63	0.172	0.182
e	5.32	5.58	0.209	0.220
E	15.77	16.03	0.621	0.631
L	19.85	20.11	0.781	0.792
L1	4.07	4.33	0.160	0.170
Ø p	3.56	3.66	0.140	0.144

ECN: X12-0191-Rev. A, 22-Oct-12
DWG: 6010



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