

MC33887

5.0 A H-bridge with load current feedback

Rev. 17 — 17 September 2018

Data sheet: technical data

1 General description

The 33887 is a monolithic H-bridge power IC with a load current feedback feature making it ideal for closed-loop DC motor control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(on)}$ MOSFET output circuitry. The 33887 is able to control inductive loads with continuous DC load currents up to 5.0 A, and with peak current active limiting between 5.2 A and 7.8 A. Output loads can be pulse width modulated at frequencies up to 10 kHz. The load current feedback feature provides a proportional (1/375th of the load current) constant-current output suitable for monitoring by a microcontroller's A/D input. This feature facilitates the design of closed-loop torque/speed control as well as open load detection. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

A fault status output pin reports undervoltage, short-circuit, and overtemperature conditions. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two disable inputs force the H-bridge outputs to 3-state (exhibit high-impedance).

The 33887 is parametrically specified over a temperature range of $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ and a voltage range of $5.0\text{ V} \leq V_+ \leq 28\text{ V}$. Operation with voltages up to 40 V with derating of the specifications.

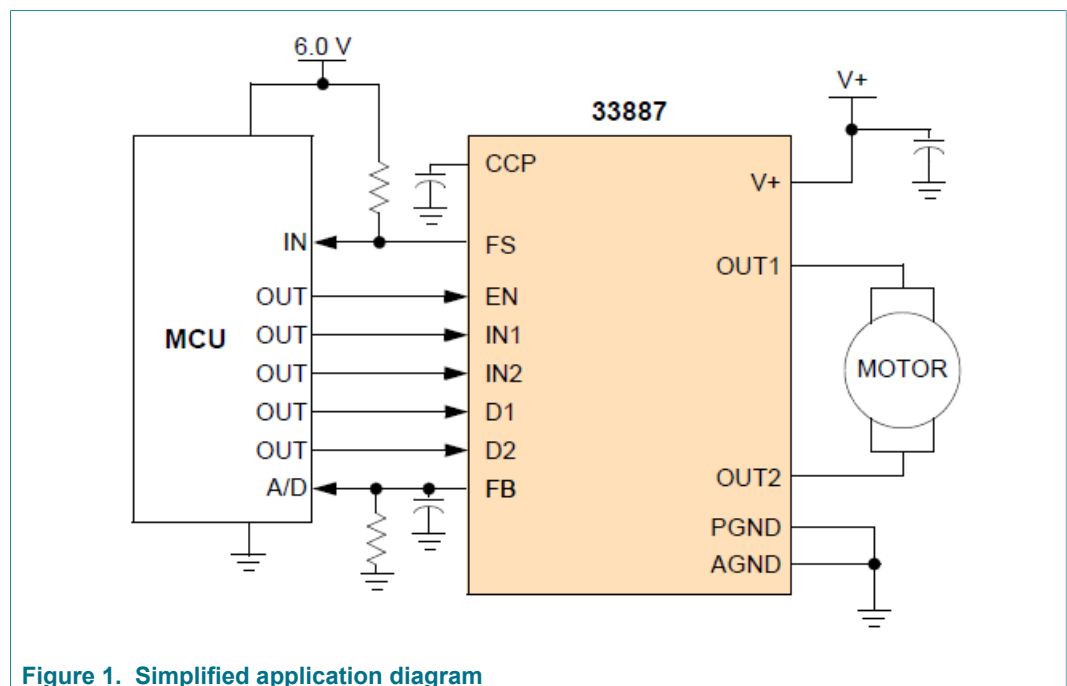


Figure 1. Simplified application diagram

2 Features and benefits

- Fully specified operation 5.0 V to 28 V
- Limited operation with reduced performance up to 40 V
- 120 mΩ $R_{DS(on)}$ typical H-bridge MOSFETs
- TTL/CMOS compatible Inputs
- PWM frequencies up to 10 kHz
- Active current limiting (regulation)
- Fault status reporting
- Sleep mode with current draw $\leq 50 \mu\text{A}$ (inputs floating or set to match default logic states)
- AEC-Q100 grade 1 qualified

3 Applications

- Electronic throttle control (ETC)
- Exhaust gas recirculation (EGR)
- Turbo flap control
- Industrial and medical pumps and motor control

4 Ordering information

Table 1. Ordering information

Type number ^[1]	Package			
	Name	Description	Operating temperature	Version
MC33887APVW	HSOP20	HSOP20, plastic, heatsink small outline package; 20 terminals; 1.27 mm pitch; 11 mm x 15.9 mm x 3.2 mm body	$T_A = -40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$	SOT397-2
MC33887PFK	HQFN36	HQFN36, 36 terminals; 0.8 mm pitch; 9 mm x 9 mm x 2.1 mm body		SOT1663-1
MC33887PEK	HSOP54	HSOP54, plastic, heatsink small outline package; 54 terminals; 0.65 mm pitch; 17.9 mm x 7.5 mm x 2.45 mm body		SOT1747-3

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Block diagram

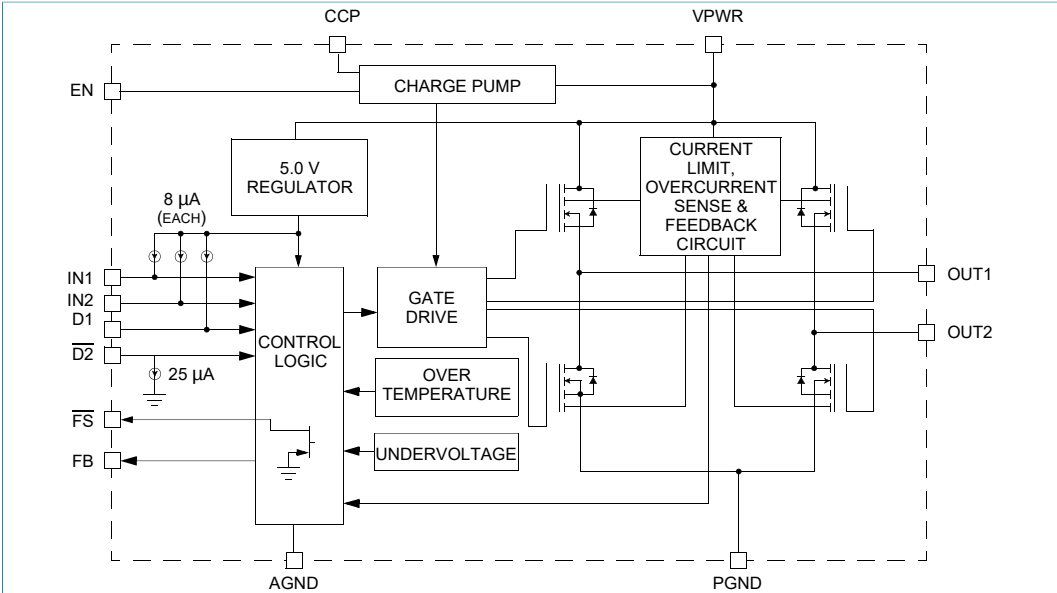


Figure 2. Block diagram

6 Pinning information

6.1 Pinning

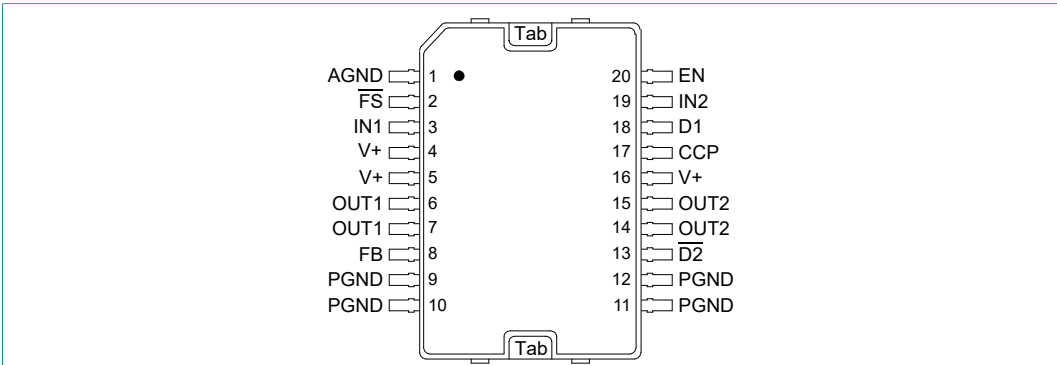


Figure 3. Pin configuration for HSOP20

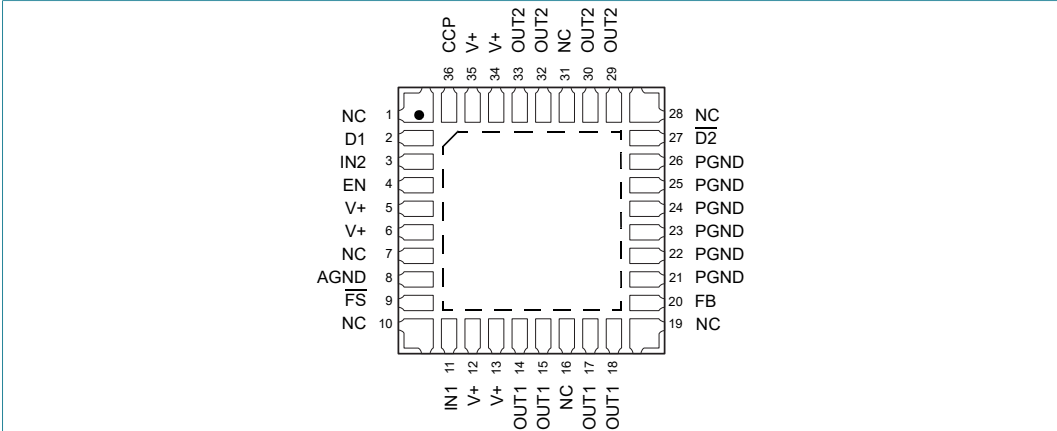


Figure 4. Pin configuration for HQFN36

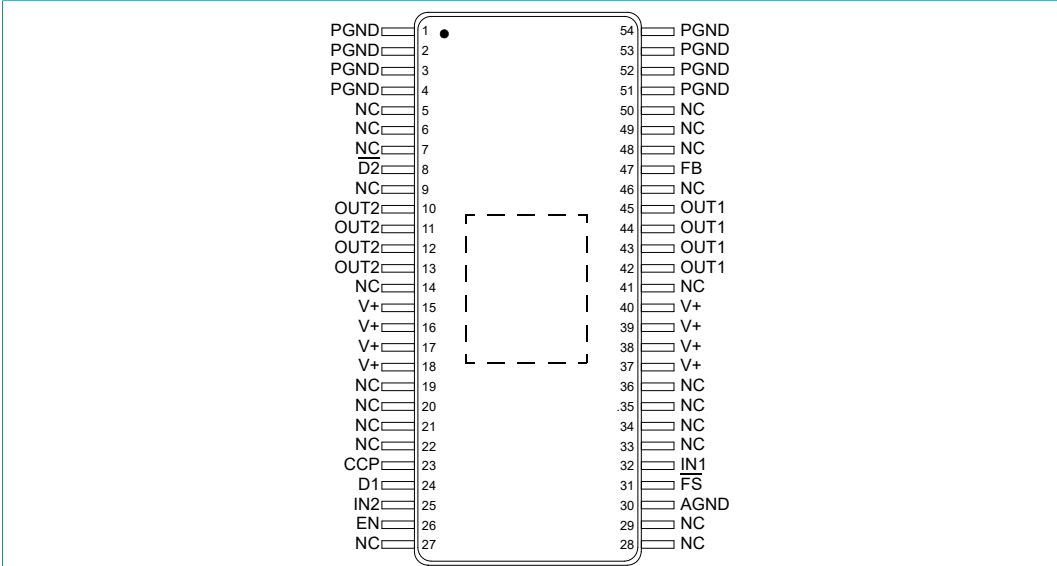


Figure 5. Pin configuration for HSOP54

6.2 Pin description

For functional description of each pin see [Section 14.2 "Functional pin description"](#).

Table 2. HSOP20 pin description

Symbol	Pin	Name	Description
AGND	1	Analog ground	Low-current analog signal ground
FS	2	Fault status for H-bridge	Open drain active low fault status output requiring a pull-up resistor to 5.0 V
IN1	3	Logic input control 1	Logic input control of OUT1 (i.e., IN1 logic high = OUT1 high)
V+	4, 5, 16	Positive power supply	Positive supply connections
OUT1	6, 7	H-bridge output 1	Output 1 of H-bridge
FB	8	Feedback for H-bridge	Current sensing feedback output providing ground referenced 1/375th (0.00266) of H-bridge high-side current
PGND	9, 10, 11, 12	Power ground	High-current power ground

5.0 A H-bridge with load current feedback

Symbol	Pin	Name	Description
D2	13	Disable 2	Active low input used to simultaneously 3-state disable both H-bridge outputs. When $\overline{D2}$ is logic low, both outputs are 3-stated.
OUT2	14, 15	H-bridge output 2	Output 2 of H-bridge
CCP	17	Charge pump capacitor	External reservoir capacitor connection for internal charge pump capacitor
D1	18	Disable 1	Active high input used to simultaneously 3-state disable both H-bridge outputs. When D1 is logic high, both outputs are 3-stated.
IN2	19	Logic input control 2	Logic input control of OUT2 (i.e., IN2 logic high = OUT2 high)
EN	20	Enable	Logic input enable control of device (i.e., EN logic high = full operation, EN logic low = Sleep mode)
Thermal interface	Tab/pad	Exposed pad thermal interface	Exposed pad thermal interface for sinking heat from the device ^[1]

[1] Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

Table 3. HQFN36 pin description

Symbol	Pin	Name	Description
n.c.	1, 7, 10, 16, 19, 28, 31	not connected	No internal connection to this pin
D1	2	Disable 1	Active high input used to simultaneously 3-state disable both H-bridge outputs. When D1 is logic high, both outputs are 3-stated.
IN2	3	Logic input control 2	Logic input control of OUT2 (i.e., IN2 logic high = OUT2 high)
EN	4	Enable	Logic input enable control of device (i.e., EN logic high = full operation, EN logic low = Sleep mode)
V+	5, 6, 12, 13, 34, 35	Positive power supply	Positive supply connections
AGND	8	Analog ground	Low-current analog signal ground
FS	9	Fault status for H-bridge	Open drain active low fault status output requiring a pull-up resistor to 5.0 V
IN1	11	Logic input control 1	Logic input control of OUT1 (i.e., IN1 logic high = OUT1 high)
OUT1	14, 15, 17, 18	H-bridge output 1	Output 1 of H-bridge
FB	20	Feedback for H-bridge	Current feedback output providing ground referenced 1/375th ratio of H-bridge high-side current
PGND	21, 22, 23, 24, 25, 26	Power ground	High-current power ground
$\overline{D2}$	27	Disable 2	Active low input used to simultaneously 3-state disable both H-bridge outputs. When $\overline{D2}$ is logic low, both outputs are 3-stated.
OUT2	29, 30, 32, 33	H-bridge output 2	Output 2 of H-bridge
CCP	36	Charge pump capacitor	External reservoir capacitor connection for internal charge pump capacitor
Thermal interface	Tab/pad	Exposed pad thermal interface	Exposed pad thermal interface for sinking heat from the device ^[1]

[1] Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

Table 4. HSOP54 pin description

Symbol	Pin	Name	Description
PGND	1, 2, 3, 4, 51, 52, 53, 54	Power ground	High-current power ground
n.c.	5, 6, 7, 9, 14, 19, 20, 21, 22, 27, 28, 29, 33, 34, 35, 36, 41, 46, 48, 49, 50	not connected	No internal connection to this pin
D2	8	Disable 2	Active low input used to simultaneously 3-state disable both H-bridge outputs. When D2 is logic low, both outputs are 3-stated.
OUT2	10, 11, 12, 13	H-bridge output 2	Output 2 of H-bridge
V+	15, 16, 17, 18, 37, 38, 39, 40	Positive power supply	Positive supply connections
CCP	23	Charge pump capacitor	External reservoir capacitor connection for internal charge pump capacitor
D1	24	Disable 1	Active high input used to simultaneously 3-state disable both H-bridge outputs. When D1 is logic high, both outputs are 3-stated.
IN2	25	Logic input control 2	Logic input control of OUT2 (i.e., IN2 logic high = OUT2 high)
EN	26	Enable	Logic input enable control of device (i.e., EN logic high = full operation, EN logic low = Sleep mode)
AGND	30	Analog ground	Low-current analog signal ground
FS	31	Fault status for H-bridge	Open drain active low fault status output requiring a pull-up resistor to 5.0 V
IN1	32	Logic input control 1	Logic input control of OUT1 (i.e., IN1 logic high = OUT1 high)
OUT1	42, 43, 44, 45	H-bridge output 1	Output 1 of H-bridge
FB	47	Feedback for H-bridge	Current feedback output providing ground referenced 1/375th ratio of H-bridge high-side current
Thermal interface	Pad	Exposed pad thermal interface	Exposed pad thermal interface for sinking heat from the device ^[1]

[1] Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

7 Maximum ratings

Table 5. Maximum ratings

All voltages are with respect to ground unless otherwise noted.

Symbol	Parameter	Value	Unit
Electrical ratings			
V+	Supply voltage	^[1] -0.3 to 40	V
V _{IN}	Input voltage	^[2] -0.3 to 7.0	V
V _{FS}	FS status output	^[3] -0.3 to 7.0	V
I _{OUT}	Continuous current	^[4] 5.0	A

Symbol	Parameter	Value	Unit
V_{ESD1} V_{ESD2}	ESD voltage • Human body model • Machine model	± 2000 ± 200	V

- [1] Performance at voltages greater than 28 V is degraded. See [Section 13](#) for typical performance. Extended operation at higher voltages has not been fully characterized and may reduce the operational lifetime.
- [2] Exceeding the input voltage on IN1, IN2, EN, D1, or D2 may cause a malfunction or permanent damage to the device.
- [3] Exceeding the pull-up resistor voltage on the open drain FS pin may cause permanent damage to the device.
- [4] Continuous current capability so long as junction temperature is $\leq 150^\circ\text{C}$.
- [5] ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100\text{ pF}$, $R_{ZAP} = 1500\ \Omega$), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200\text{ pF}$, $R_{ZAP} = 0\ \Omega$).

8 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature	-65 to 150	$^\circ\text{C}$
T_A	Operational ambient temperature	[1] -40 to 125	$^\circ\text{C}$
T_J	Operation junction temperature	[1] -40 to 150	$^\circ\text{C}$
T_{PPRT}	Peak package reflow temperature during reflow	[2] [3]	$^\circ\text{C}$
Thermal resistance and package dissipation [4] [5] [6] [7]			
$R_{\theta JB}$	Junction-to-board (bottom exposed pad soldered to board) • HSOP20 (6.0 W) • HQFN36 (4.0 W) • HSOP54 (2.0 W)	~ 7.0 ~ 8.0 ~ 9.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient, natural convection, single-layer board (1s) • HSOP20 (6.0 W) • HQFN36 (4.0 W) • HSOP54 (2.0 W)	[8] ~ 41 ~ 50 ~ 62	$^\circ\text{C/W}$
$R_{\theta JMA}$	Junction-to-ambient, natural convection, four-layer board (2s2p) • HSOP20 (6.0 W) • HQFN36 (4.0 W) • HSOP54 (2.0 W)	[9] ~ 18 ~ 21 ~ 23	$^\circ\text{C/W}$
$R_{\theta JC}$	Junction-to-case (exposed pad) • HSOP20 (6.0 W) • HQFN36 (4.0 W) • HSOP54 (2.0 W)	[10] ~ 0.8 ~ 1.2 ~ 2.0	$^\circ\text{C/W}$

- [1] The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief non-repetitive excursions of junction temperature above 150°C can be tolerated, provided the duration does not exceed 30 seconds maximum. Non-repetitive events are defined as not occurring more than once in 24 hours.
- [2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- [3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes and enter the core ID) to view all orderable parts, and review parametrics.
- [4] The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
- [5] Exposed heatsink pad plus the power and ground pins comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness. Maximum current at maximum die temperature represents $\sim 16\text{ W}$ of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the $R_{\theta JC}$ -total must be less than 5.0°C/W for maximum load at 70°C ambient. Module thermal design must be planned accordingly.
- [6] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- [7] Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- [8] Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
- [9] Per JEDEC JESD51-6 with the board horizontal.
- [10] Indicates the maximum thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

9 Static characteristics

Table 7. Static characteristics

Characteristics noted under conditions $5.0\text{ V} \leq V_+ \leq 28\text{ V}$ and $-40\text{ }^\circ\text{C} \leq T_A \leq 125\text{ }^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^\circ\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Power supply					
V_+	Operating voltage range ^[1]	5.0	—	28	V
$I_{Q(\text{SLEEP})}$	Sleep state supply current ^[2] • $I_{\text{OUT}} = 0\text{ A}$, $V_{\text{EN}} = 0\text{ V}$	—	25	50	μA
$I_{Q(\text{STANDBY})}$	Standby supply current • $I_{\text{OUT}} = 0\text{ A}$, $V_{\text{EN}} = 5.0\text{ V}$	—	—	20	mA
$V_{+(\text{THRES-OFF})}$	Threshold supply voltage • Switch OFF	4.15	4.4	4.65	V
$V_{+(\text{THRES-ON})}$	• Switch ON	4.5	4.75	5.0	V
$V_{+(\text{HYS})}$	• Hysteresis	150	—	—	mV
Charge pump					
$V_{\text{CP}} - V_+$	Charge pump voltage • $V_+ = 5.0\text{ V}$ • $8.0\text{ V} \leq V_+ \leq 28\text{ V}$	3.35 —	— —	— 20	V
Control inputs					
V_{IH} V_{IL} V_{HYS}	Input voltage (IN1, IN2, D1, D2) • Threshold high • Threshold low • Hysteresis	3.5 — 0.7	— — 1.0	— 1.4 —	V
I_{INP}	Input current (IN1, IN2, D1) • $V_{\text{IN}} = 0.0\text{ V}$	−200	−80	—	μA
I_{INP}	Input current ($\overline{\text{D2}}$, EN) • $V_{\overline{\text{D2}}} = 5.0\text{ V}$	—	25	100	μA
Power outputs OUT1, OUT2					
$R_{\text{DS(on)}}$	Output ON resistance ^[3] • $5.0\text{ V} \leq V_+ \leq 28\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$ • $8.0\text{ V} \leq V_+ \leq 28\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ • $5.0\text{ V} \leq V_+ \leq 8.0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	— — —	120 — —	— 225 300	m Ω
I_{LIM}	Active current limiting threshold (via internal constant OFF time PWM) on low-side MOSFETs ^[4]	5.2	6.5	7.8	A
I_{SCH}	High-side short-circuit detection threshold	11	—	—	A
I_{SCL}	Low-side short-circuit detection threshold	8.0	—	—	A
$I_{\text{OUT(LEAK)}}$	Leakage current ^[5] • $V_{\text{OUT}} = V_+$ • $V_{\text{OUT}} = \text{Ground}$	— —	100 30	200 60	μA
V_F	Output MOSFET body diode forward voltage drop • $I_{\text{OUT}} = 3.0\text{ A}$	—	—	2.0	V
T_{LIM} T_{HYS}	Overtemperature shutdown • Thermal limit • Hysteresis	175 10	— —	225 30	$^\circ\text{C}$
High-side current sense feedback					
I_{FB}	Feedback current • $I_{\text{OUT}} = 0\text{ mA}$ • $I_{\text{OUT}} = 500\text{ mA}$ • $I_{\text{OUT}} = 1.5\text{ A}$ • $I_{\text{OUT}} = 3.0\text{ A}$ • $I_{\text{OUT}} = 6.0\text{ A}$	— 1.07 3.6 7.2 14.4	— 1.33 4.0 8.0 16	600 1.68 4.62 9.24 18.48	μA mA mA mA mA

5.0 A H-bridge with load current feedback

Symbol	Parameter	Min	Typ	Max	Unit
Fault status ^[6]					
$I_{FS(LEAK)}$	Fault status leakage current • $V_{FS} = 5.0\text{ V}$	—	—	10	μA
$V_{FS(LOW)}$	Fault status set voltage • $I_{FS} = 300\text{ }\mu\text{A}$	—	—	1.0	V

- [1] Specifications are characterized over the range of $5.0\text{ V} \leq V+ \leq 28\text{ V}$. See [Section 13](#) and [Section 14](#) for information about operation outside of this range.
- [2] $I_{Q(sleep)}$ is with sleep mode function enabled.
- [3] Output ON resistance as measured from output to V+ and ground.
- [4] Active current limitation applies only for the low-side MOSFETs.
- [5] Outputs switched OFF via D1 or D2.
- [6] Fault status output is an open drain output requiring a pull-up resistor to 5.0 V.
- [7] Fault status leakage current is measured with fault status high and not set.
- [8] Fault status set voltage is measured with fault status low and set with $I_{FS} = 300\text{ }\mu\text{A}$.

10 Dynamic characteristics

Table 8. Dynamic characteristics

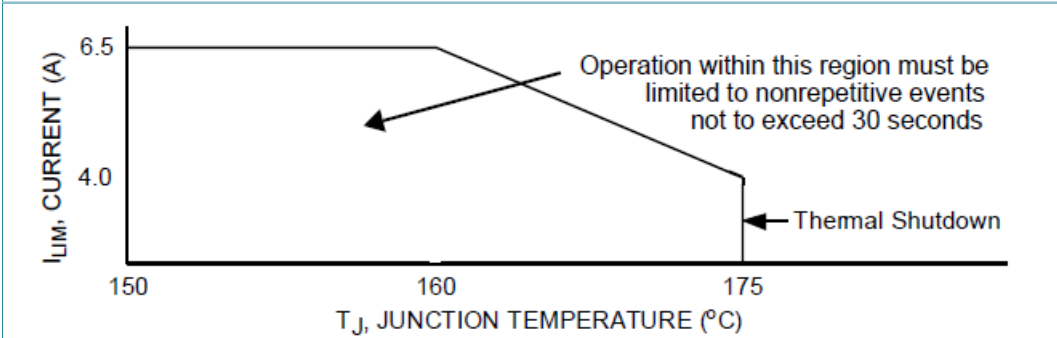
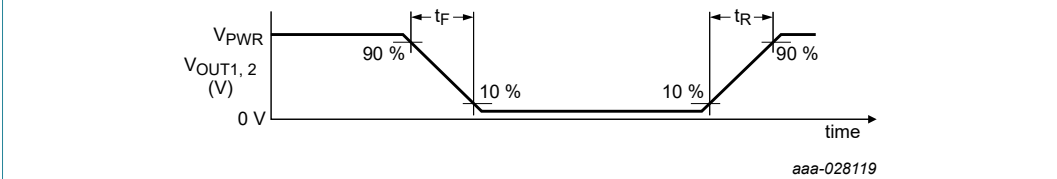
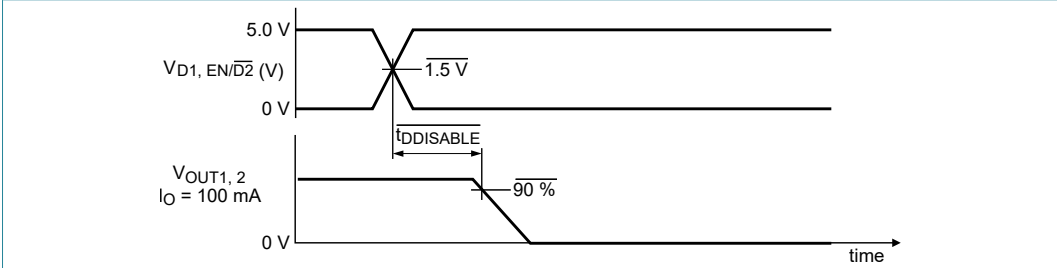
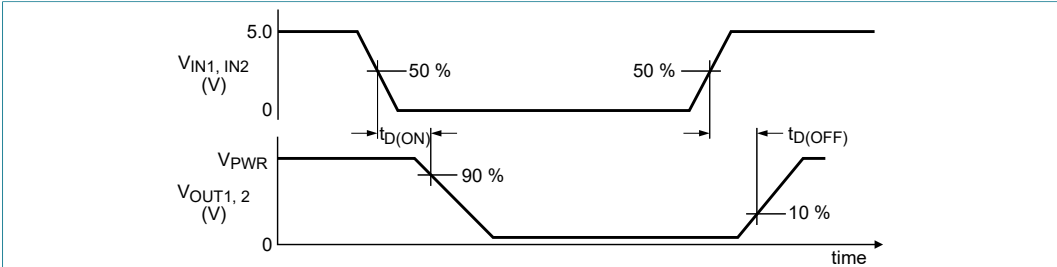
Characteristics noted under conditions $5.0\text{ V} \leq V+ \leq 28\text{ V}$ and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Timing characteristics					
f_{PWM}	PWM frequency ^[1]	—	10	—	kHz
f_{MAX}	Maximum switching frequency during active current limiting ^[2]	—	—	20	kHz
$t_{D(ON)}$	Output ON delay • $V+ = 14\text{ V}$ ^[3]	—	—	18	μs
$t_{D(OFF)}$	Output OFF delay • $V+ = 14\text{ V}$ ^[3]	—	—	18	μs
t_A	I_{LIM} output constant OFF time for low-side MOSFETs ^{[4] [5]}	15	20.5	26	μs
t_B	I_{LIM} blanking time for low-side MOSFETs ^{[5] [6]}	12	16.5	21	μs
t_F, t_R	Output rise and fall time • $V+ = 14\text{ V}, I_{OUT} = 3.0\text{ A}$ ^[7]	2.0	5.0	8.0	μs
$t_{D(DISABLE)}$	Disable delay time ^[8]	—	—	8.0	μs
t_{POD}	Power ON delay time ^[9]	—	1.0	5.0	ms
t_{WUD}	Wake-up delay time ^[9]	—	1.0	5.0	ms
t_{RR}	Output MOSFET body diode reverse recovery time ^[10]	100	—	—	ns

- [1] The outputs can be PWM-controlled from an external source. This is typically done by holding one input high while applying a PWM pulse train to the other input. The maximum PWM frequency obtainable is a compromise between switching losses and switching frequency. See [Section 12](#).
- [2] The maximum switching frequency during active current limiting is internally implemented. The internal current limit circuitry produces a constant OFF time pulse-width modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (OFF time + ON time) and thus the PWM frequency during current limit.
- [3] Output delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10 % or 90 % point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning high to low, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning low to high, the delay is from the midpoint of the input signal to the 10 % point of the output response signal. See [Figure 6](#).
- [4] I_{LIM} output constant OFF time is the time during which the internal constant OFF time PWM current regulation circuit has 3-stated the output bridge.
- [5] Load currents ramping up to the current regulation threshold become limited at the I_{LIM} value. The short-circuit current possess a di/dt that ramps up to the I_{SCH} or I_{SCL} threshold during the I_{LIM} blanking time, registering as a short-circuit event detection and causing the shutdown circuitry to force the output into an immediate 3-state latch OFF. See [Figure 10](#) and [Figure 11](#). Operation in current limit mode may cause junction temperatures to rise. Junction temperatures above $\sim 160\text{ }^{\circ}\text{C}$ causes the output current limit threshold to progressively foldback, or decrease with temperature, until $\sim 175\text{ }^{\circ}\text{C}$ is reached, after which the T_{LIM} thermal latch OFF occurs. Permissible operation within this foldback region is limited to nonrepetitive transient events of duration not to exceed 30 seconds. See [Figure 9](#).
- [6] I_{LIM} blanking time is the time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act.
- [7] Rise time is from the 10 % to the 90 % level and fall time is from the 90 % to the 10 % level of the output signal. See [Figure 8](#).
- [8] Disable delay time measurement is defined in [Figure 7](#).

[9] Parameter has been characterized but not production tested.
[10] Parameter is guaranteed by design but not production tested.

11 Timing diagrams



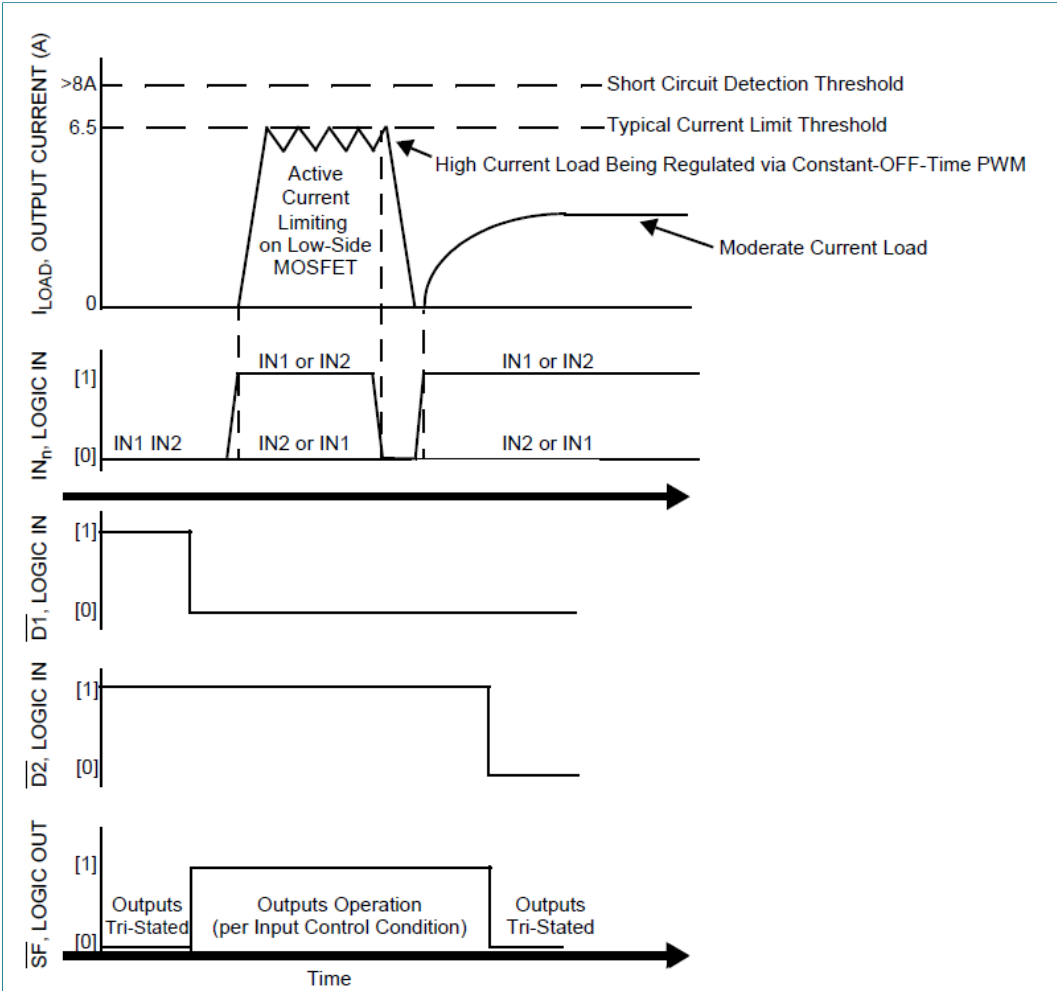


Figure 10. Operating states

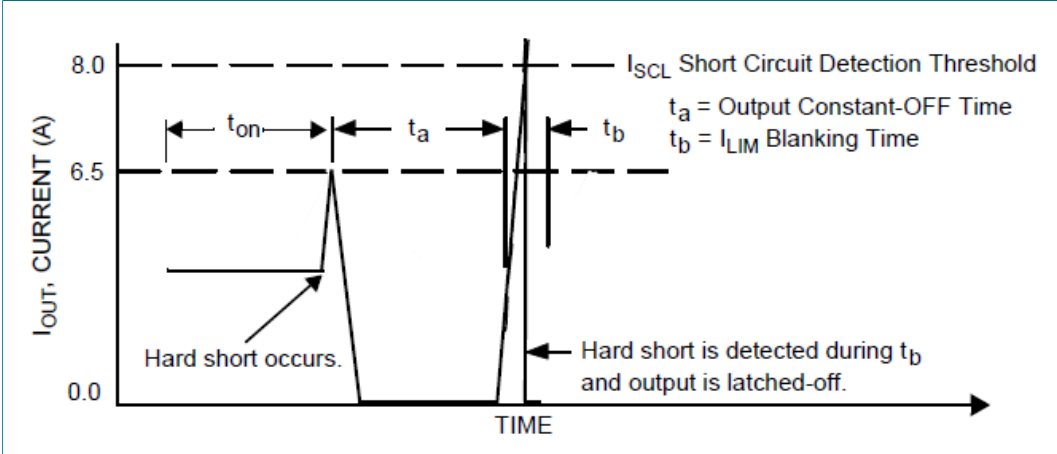


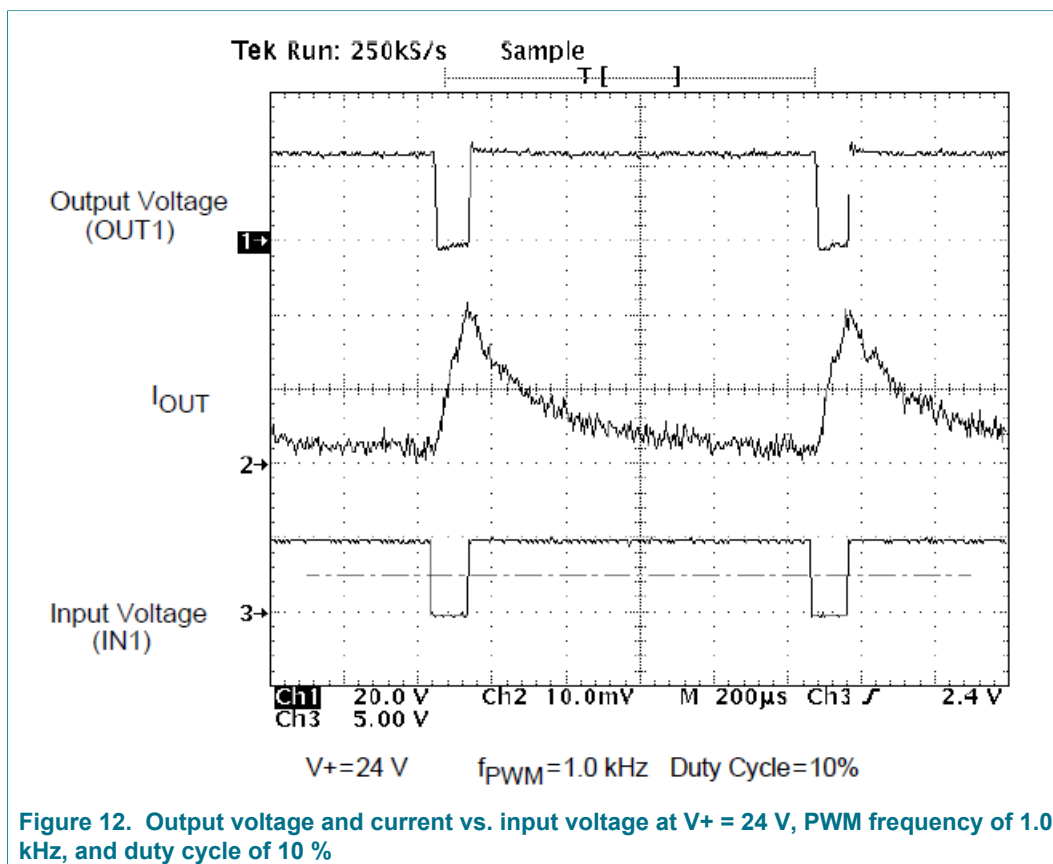
Figure 11. Example short-circuit detection detail on low-side MOSFET

12 Typical switching waveforms

Important: For all plots, the following applies:

5.0 A H-bridge with load current feedback

- $Ch2 = 2.0 \text{ A per division}$
- $L_{LOAD} = 533 \mu\text{H} @ 1.0 \text{ kHz}$
- $L_{LOAD} = 530 \mu\text{H} @ 10.0 \text{ kHz}$
- $R_{LOAD} = 4.0 \Omega$



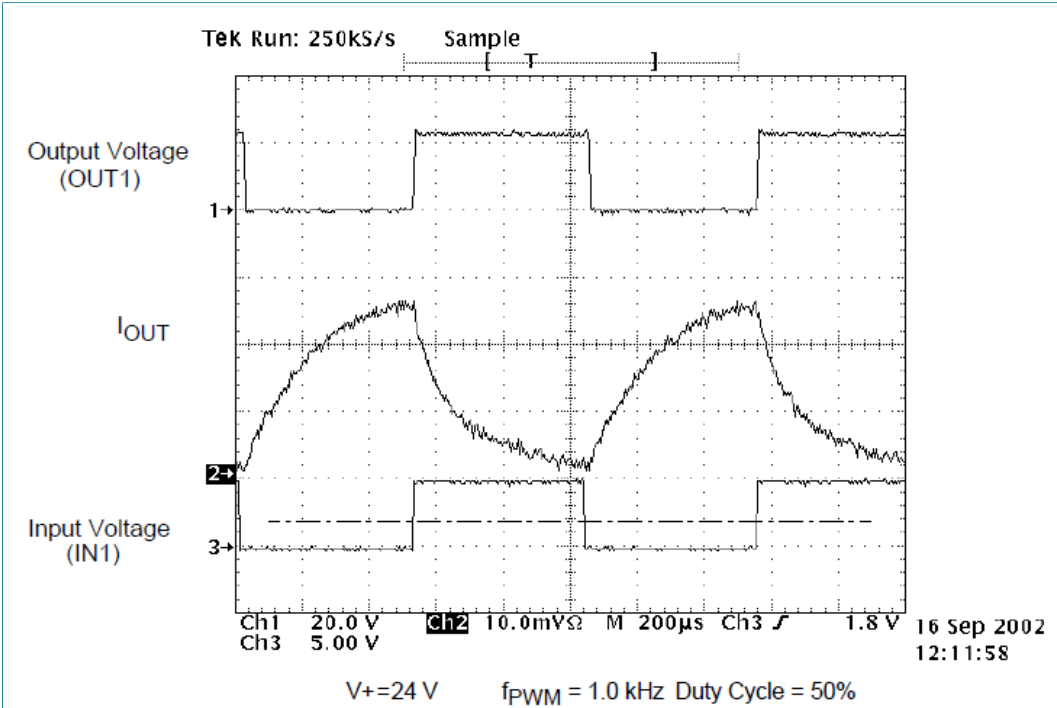


Figure 13. Output voltage and current vs. input voltage at $V+ = 24\text{ V}$, PWM frequency of 1.0 kHz, and duty cycle of 50 %

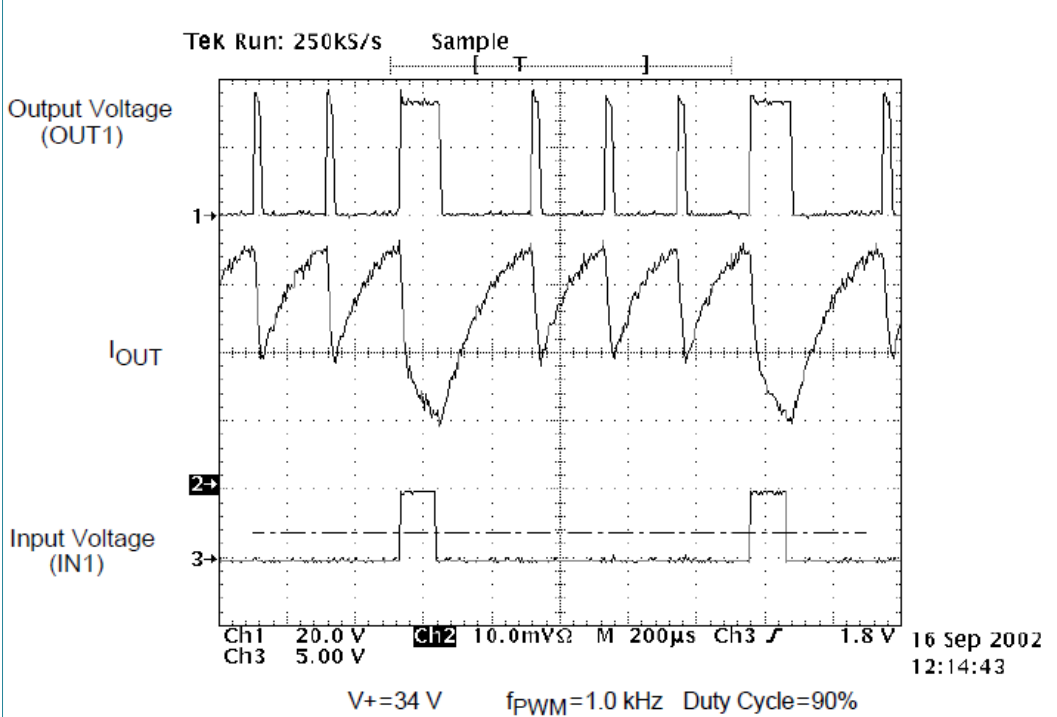


Figure 14. Output voltage and current vs. input voltage at $V+ = 34\text{ V}$, PWM frequency of 1.0 kHz, and duty cycle of 90 %, showing device in current limiting mode

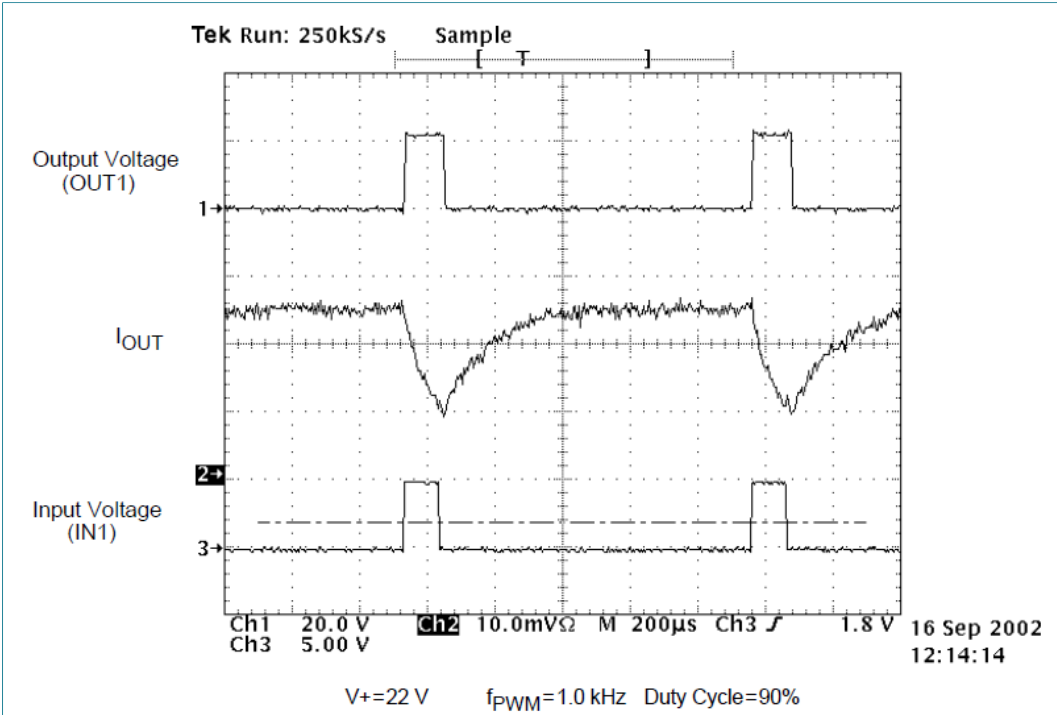


Figure 15. Output voltage and current vs. input voltage at $V+ = 22\text{ V}$, PWM frequency of 1.0 kHz, and duty cycle of 90 %

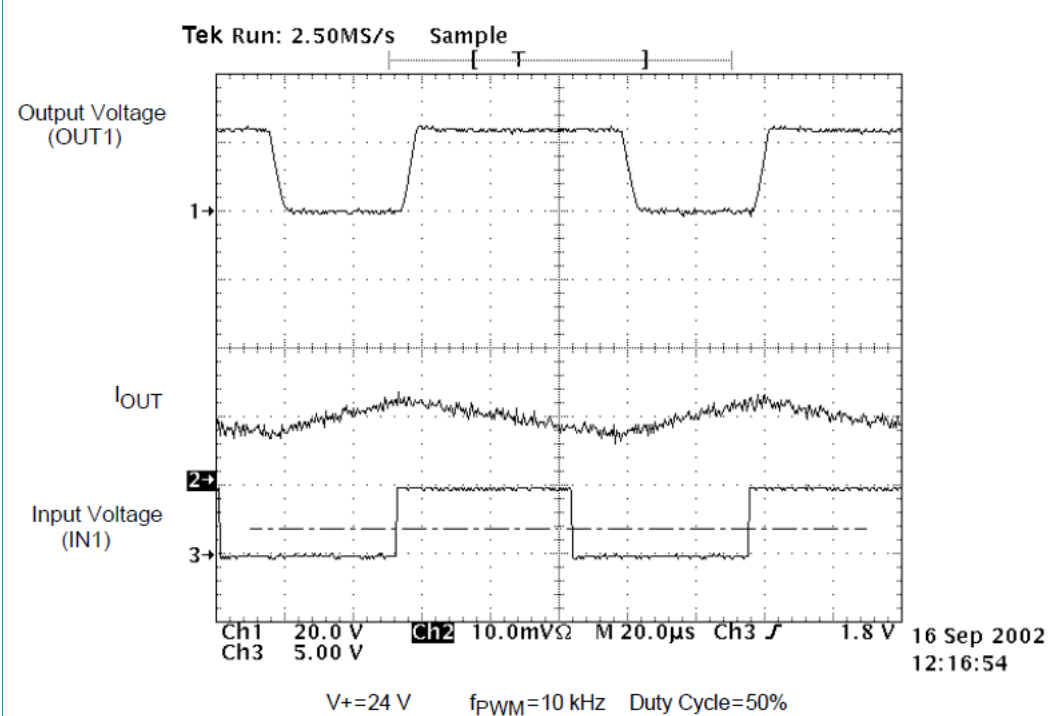


Figure 16. Output voltage and current vs. input voltage at $V+ = 24\text{ V}$, PWM frequency of 10 kHz, and duty cycle of 50 %

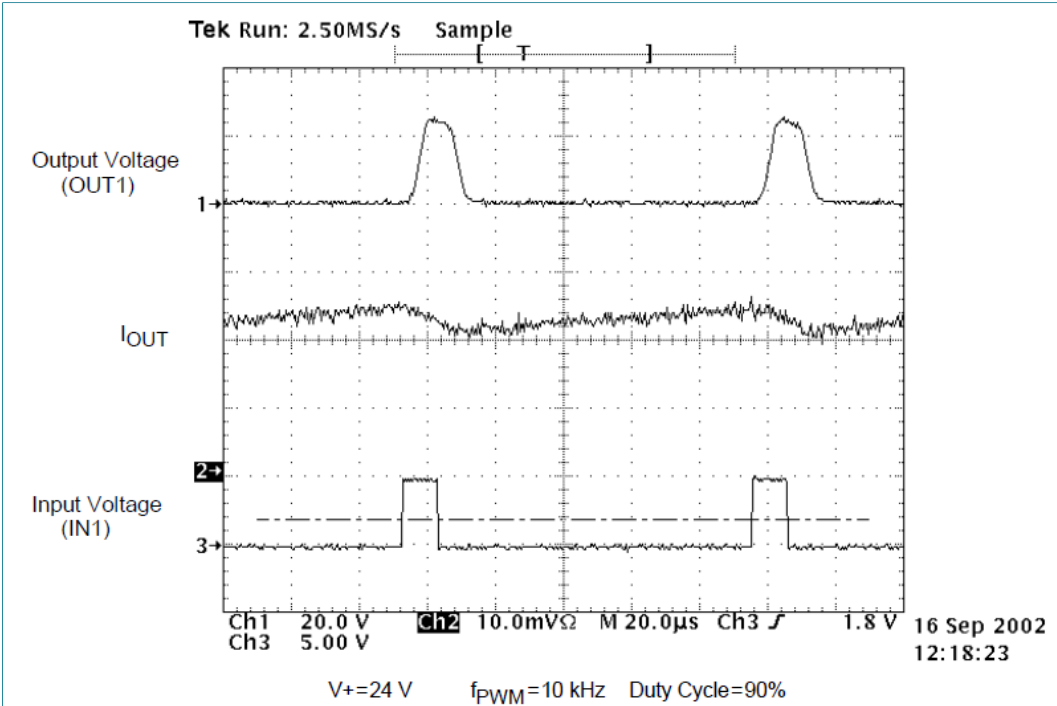


Figure 17. Output voltage and current vs. input voltage at $V+ = 24\text{ V}$, PWM frequency of 10 kHz, and duty cycle of 90 %

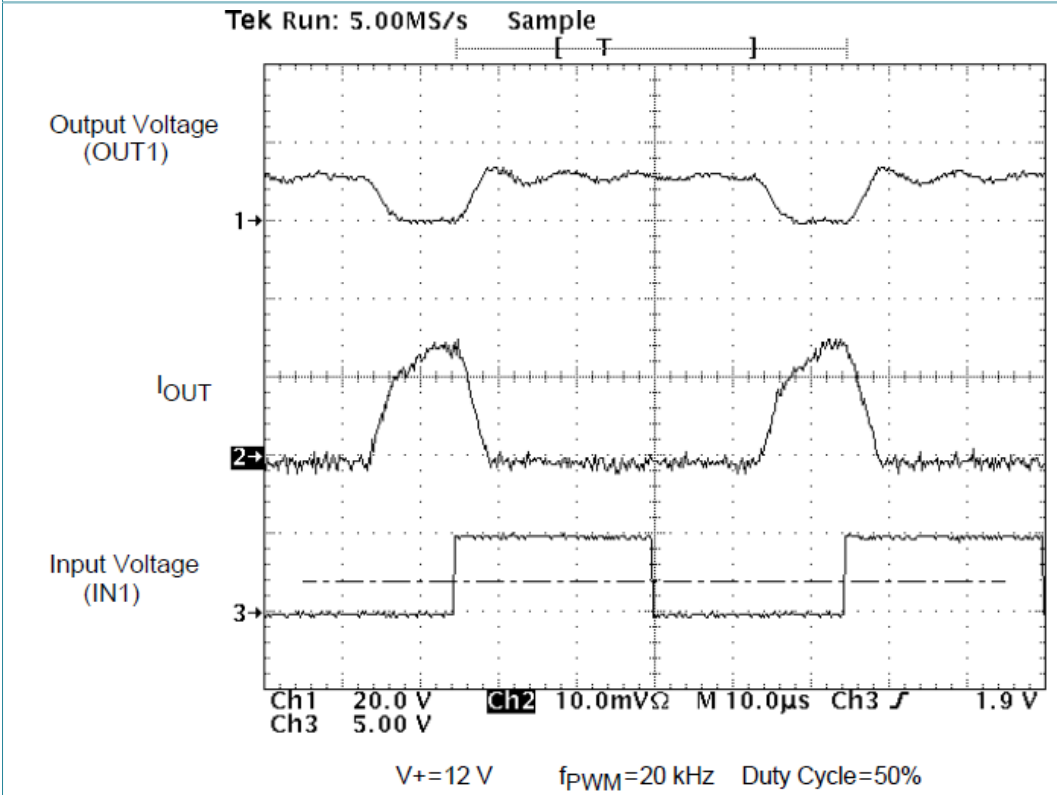
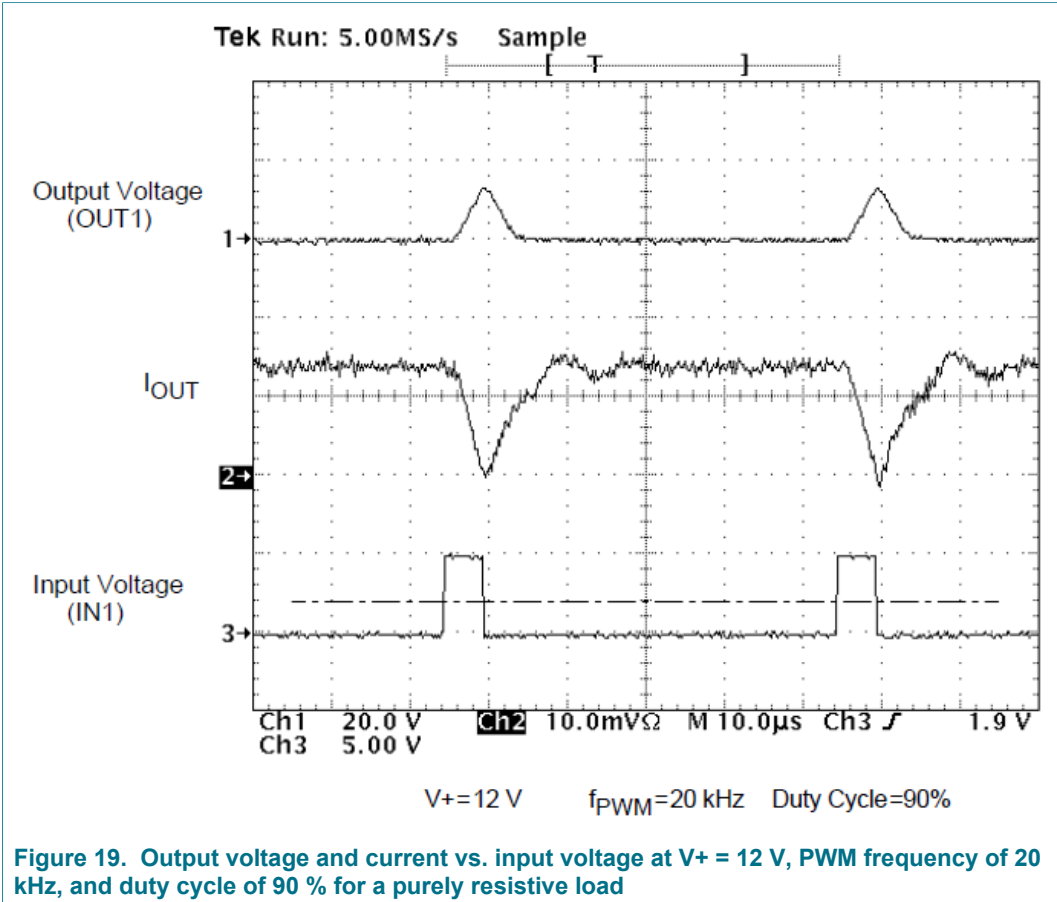
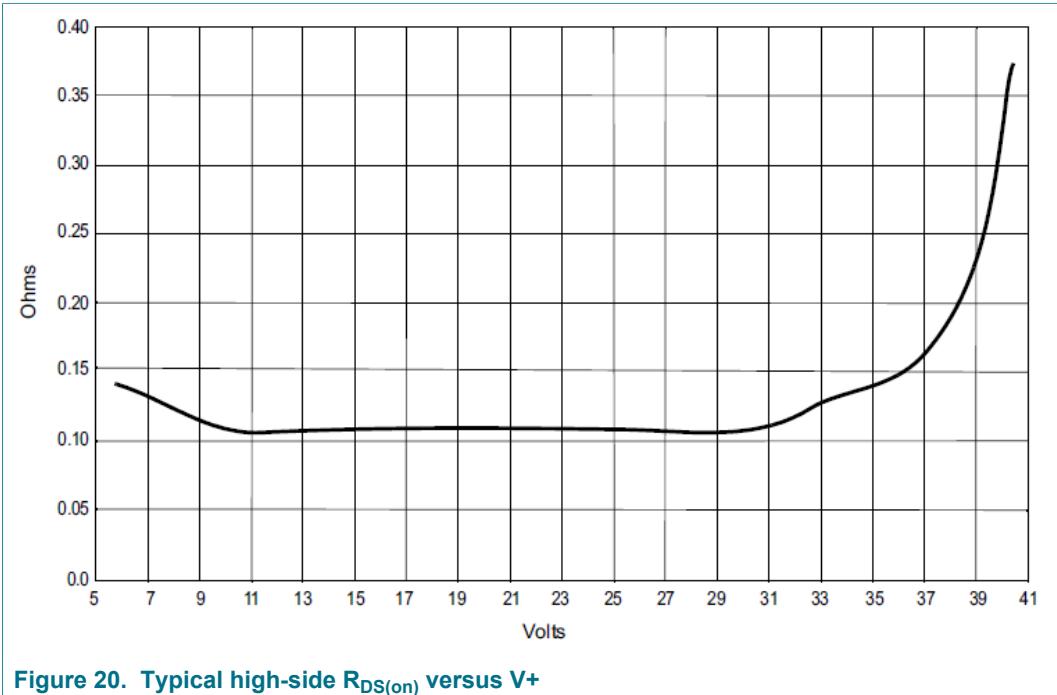


Figure 18. Output voltage and current vs. input voltage at $V+ = 12\text{ V}$, PWM frequency of 20 kHz, and duty cycle of 50 % for a purely resistive load



13 Electrical performance curves



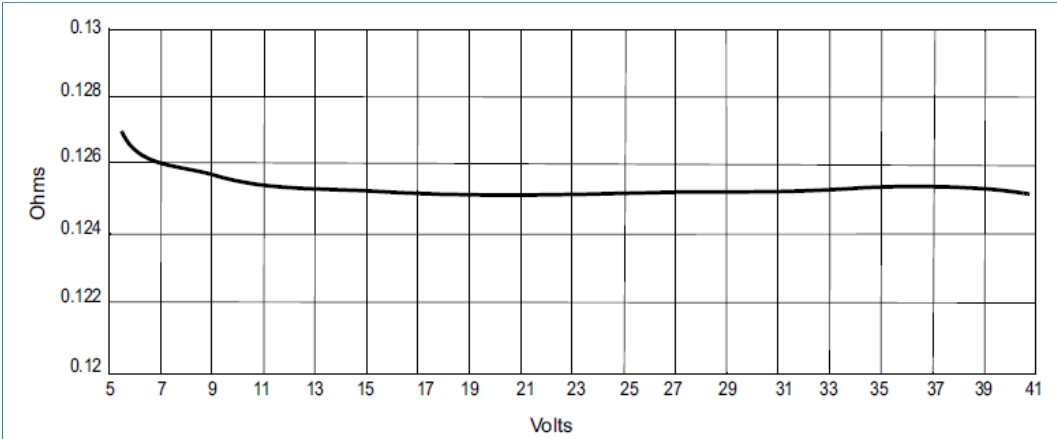


Figure 21. Typical low-side R_{DS(on)} versus V+

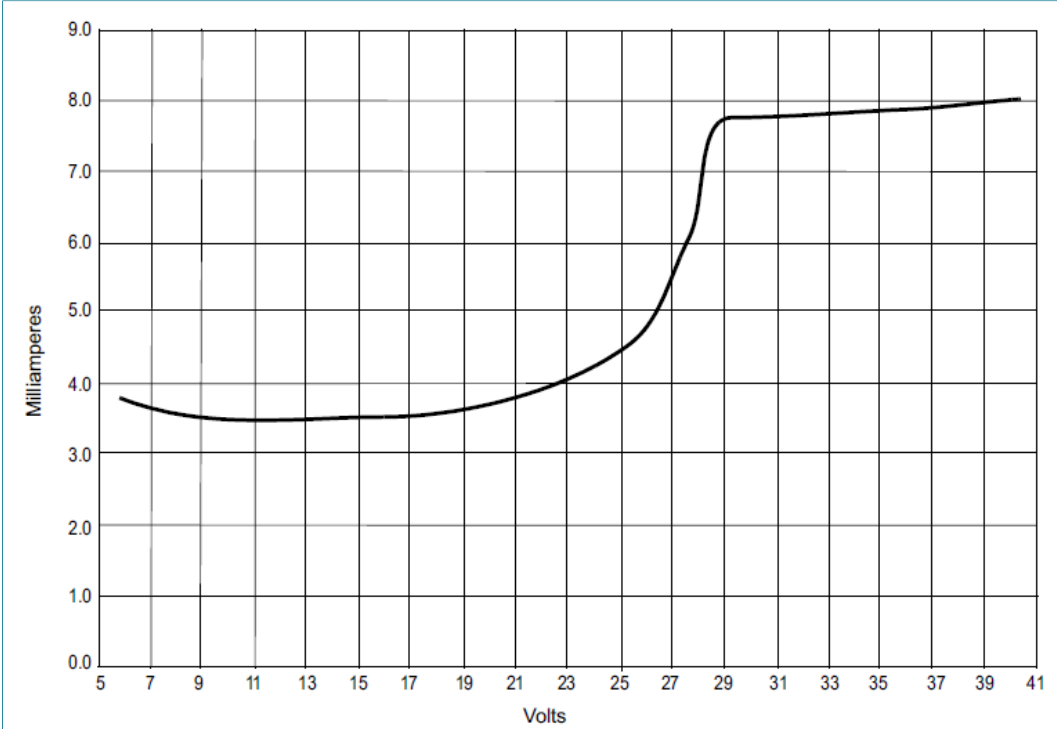


Figure 22. Typical quiescent supply current versus V+

Table 9. Truth table

The 3-state conditions and the status flag are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = low, H = high, X = high or low, and Z = high-impedance.

Device state	Input conditions					Fault status flag	Output state	
	EN	D1	$\overline{D2}$	IN1	IN2	$\overline{FS}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Freewheeling low	H	L	H	L	L	H	L	L
Freewheeling high	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 disconnected	H	L	H	Z	X	H	H	X
IN2 disconnected	H	L	H	X	Z	H	X	H
D1 disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage ^[1]	H	X	X	X	X	L	Z	Z
Overtemperature ^[2]	H	X	X	X	X	L	Z	Z
Short-circuit ^[2]	H	X	X	X	X	L	Z	Z
Sleep mode EN	L	X	X	X	X	H	Z	Z
EN disconnected	Z	X	X	X	X	H	Z	Z

[1] In the event of an undervoltage condition, the outputs 3-state and status flag are set to logic low. Upon undervoltage recovery, status flag is reset automatically or automatically cleared and the outputs are restored to their original operating condition.

[2] When a short-circuit or overtemperature condition is detected, the power outputs are 3-state latched OFF independent of the input signals and the fault status flag is set logic low.

14 Functional description

14.1 Introduction

Numerous protection and operational features (speed, torque, direction, dynamic braking, PWM control, and closed-loop control), in addition to the 5.0 A current capability, make the 33887 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 33887 devices can be used to control bipolar stepper motors. The 33887 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

14.2 Functional pin description

14.2.1 Power ground and analog ground (PGND and AGND)

The power and analog ground pins should be connected together with a very low-impedance connection.

14.2.2 Positive power supply (V+)

V+ pins are the power supply inputs to the device. All V+ pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

V+ pins have an undervoltage threshold. If the supply voltage drops below a V+ undervoltage threshold, the output power stage switches to a 3-state condition and the fault status flag is set and the fault status pin voltage switches to a logic low. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins and the fault status flag is automatically reset logic high.

As V+ increases in value above 28 V, the charge pump performance begins to degrade. At +40 V, the charge pump is effectively non-functional. Operation at this high voltage level results in the output FETs not being enhanced when turned on. This means that the voltage on the output will be $V_{OUT} = (V+) - V_{GS}$. This increased voltage drop under load produces a higher power dissipation.

14.2.3 Fault status (FS)

The $\overline{FS}$ pin is the device fault status output. This output is an active low open drain structure requiring a pull-up resistor to 5.0 V. See [Table 9](#).

14.2.4 Logic input control and disable (IN1, IN2, D1, and $\overline{D2}$)

These pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complementary inputs used to 3-state disable the H-bridge outputs.

When either D1 or $\overline{D2}$ is set (D1 = logic high or D2 = logic low) in the disable state, outputs OUT1 and OUT2 are both 3-state disabled; however, the rest of the circuitry is fully operational and the supply $I_{Q(standby)}$ current is reduced to a few milliamperes. See [Table 9](#) and [Table 7](#).

14.2.5 H-bridge output (OUT1, OUT2)

These pins are the outputs of the H-bridge with integrated output MOSFET body diodes. The bridge output is controlled using the IN1, IN2, D1 and $\overline{D2}$ inputs. The low-side MOSFETs have active current limiting above the I_{LIM} threshold. The outputs also have thermal shutdown (3-state latch off) with hysteresis as well as short-circuit latch off protection.

A disable timer (time t_b) used to detect currents that are higher than current limit is activated at each output activation to facilitate hard short detection (see [Figure 11](#)).

14.2.6 Charge pump capacitor (CCP)

A filter capacitor (up to 33 nF) can be connected from the charge pump output pin and PGND. The device can operate without the external capacitor, although the C_{CP} capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

14.2.7 Enable (EN)

The EN pin is used to place the device in a Sleep mode so as to consume very low currents. When the EN pin voltage is a logic low state, the device is in the Sleep mode. The device is enabled and fully operational when the EN pin voltage is logic high.

An internal pull-down resistor maintains the device in Sleep mode in the event EN is driven through a high impedance I/O or an unpowered microcontroller, or the EN input becomes disconnected.

14.2.8 Feedback for H-bridge (FB)

The 33887 has a feedback output (FB) for real time monitoring of H-bridge high-side current to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-bridge high-side drivers. When running in forward or reverse direction, a ground referenced 1/375th (0.00266) of load current is output to this pin. Through an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can read the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is $100 < R_{FB} < 200 \Omega$.

If PWM-ing is implemented using the disable pin inputs (either D1 or $\overline{D2}$), a small filter capacitor (1.0 μF or less) may be required in parallel with the external resistor to ground for fast spike suppression.

15 Functional device operation

15.1 Operational modes

The 33887 (see [Figure 2](#)), is a fully protected monolithic H-bridge with enable, fault status reporting, and high-side current sense feedback to accommodate closed-loop PWM control.

For a DC motor to run, the input conditions need be as follows: Enable input logic high, D1 input logic low, $\overline{D2}$ input logic high, $\overline{FS}$ flag cleared (logic high), one IN logic low and the other IN logic high (to define output polarity). The 33887 can execute dynamic braking by simultaneously turning on either both high-side MOSFETs or both low-side MOSFETs in the output H-bridge; e.g., IN1 and IN2 logic high or IN1 and IN2 logic low.

The 33887 outputs are capable of providing a continuous DC load current of 5.0 A from a 28 V V+ source. An internal charge pump supports PWM frequencies to 10 kHz. An external pull-up resistor is required at the $\overline{FS}$ pin for fault status reporting. The 33887 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant current source ratioed to the active high-side MOSFET. This can be used to provide real time monitoring of load current to facilitate closed-loop operation for motor speed/torque control.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) provide the means to force the H-bridge outputs to a high-impedance state (all H-bridges switch off). An EN pin controls an enable function that allows the 33887 to be placed in a power-conserving sleep mode.

The 33887 has undervoltage shutdown with automatic recovery, active current limiting, output short-circuit latch off, and overtemperature latch off. An undervoltage shutdown, output short-circuit latch off, or overtemperature latch off fault condition causes the outputs to turn off (i.e., become high impedance or 3-stated) and the fault output flag to be set low. Either of the disable inputs or V+ must be toggled to clear the fault flag.

Active current limiting is accomplished by a constant OFF time PWM method employing active current limiting threshold triggering. The active current limiting scheme is unique in that it incorporates a junction temperature dependent current limit threshold. This means the active current limiting threshold is ramped down as the junction temperature increases above 160 °C, until at 175 °C the current is decreased to about 4.0 A. Above 175 °C, the overtemperature shutdown (latch off) occurs. This combination of features allows the device to remain in operation for 30 seconds at junction temperatures above 150 °C for nonrepetitive unexpected loads.

15.2 Protection and diagnostic features

15.2.1 Short-circuit protection

If an output short-circuit condition is detected, the power outputs 3-state (latch off) independent of the input (IN1 and IN2) states, and the fault status output flag is set logic low. If the D1 input changes from logic high to logic low, or if the $\overline{D2}$ input changes from logic low to logic high, the output bridge becomes operational again and the fault status flag is reset (cleared) to a logic High state.

The output stage always switches into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

15.2.2 Active current limiting

The maximum current flow under normal operating conditions is internally limited to I_{LIM} (5.2 A to 7.8 A). When the maximum current value is reached, the output stages are 3-stated for a fixed time (t_a) of 20 μ s typical. Depending on the time constant associated with the load characteristics, the current decreases during the 3-state duration until the next output ON cycle occurs (see [Figure 11](#) and [Figure 14](#)).

The current limiting threshold value is dependent upon the device junction temperature. When $-40\text{ }^{\circ}\text{C} \leq T_J \leq 160\text{ }^{\circ}\text{C}$, I_{LIM} is between 5.2 A to 7.8 A. When T_J exceeds 160 °C, the I_{LIM} current decreases linearly down to 4.0 A typical at 175 °C. Above 175 °C the device overtemperature circuit detects T_{LIM} and overtemperature shutdown occurs (see [Figure 9](#)). This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160 °C.

15.2.3 Output avalanche protection

An inductive flyback event, namely when the outputs are suddenly disabled and V+ is lost, could result in electrical overstress of the drivers. To prevent this, the V+ input to the 33887 should not exceed the maximum rating during a flyback condition. This may be done with either a zener clamp and/or an appropriately valued input capacitor with sufficiently low ESR.

15.2.4 Overtemperature shutdown and hysteresis

If an overtemperature condition occurs, the power outputs are 3-stated (latched off) and the fault status flag is set to logic low.

To reset from this condition, D1 must change from logic high to logic low, or $\overline{D2}$ must change from logic low to logic high. When reset, the output stage switches ON again,

provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Important:

Resetting from the fault condition clears the fault status flag.

16 Typical applications

Figure 23 shows a typical application schematic. For precision high-current applications in harsh, noisy environments, the V+ bypass capacitor may need to be substantially larger.

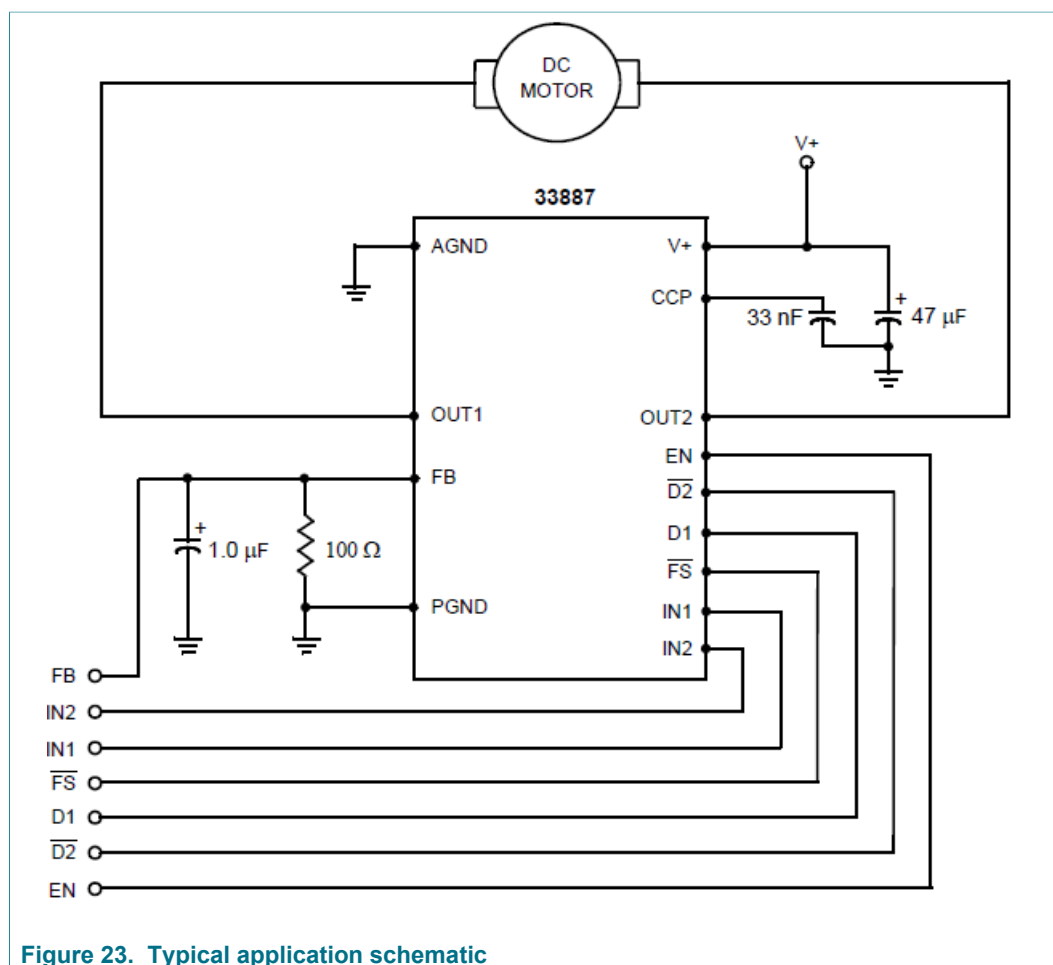


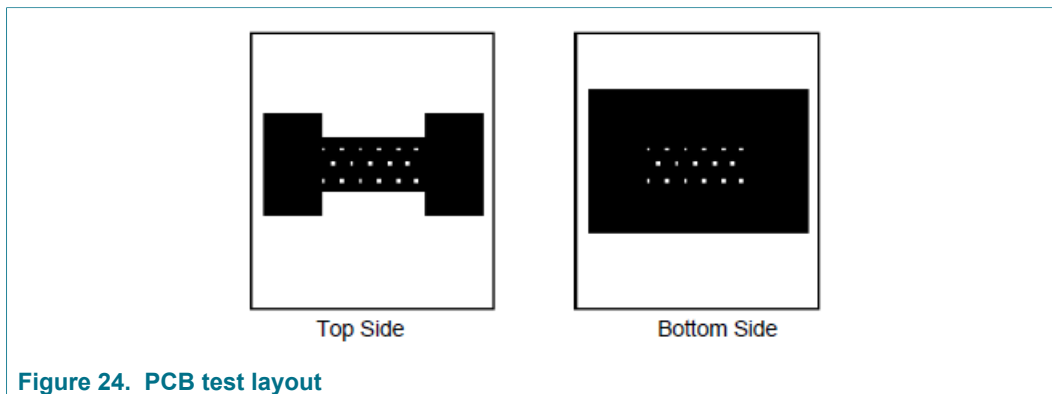
Figure 23. Typical application schematic

17 Packaging

17.1 Soldering information

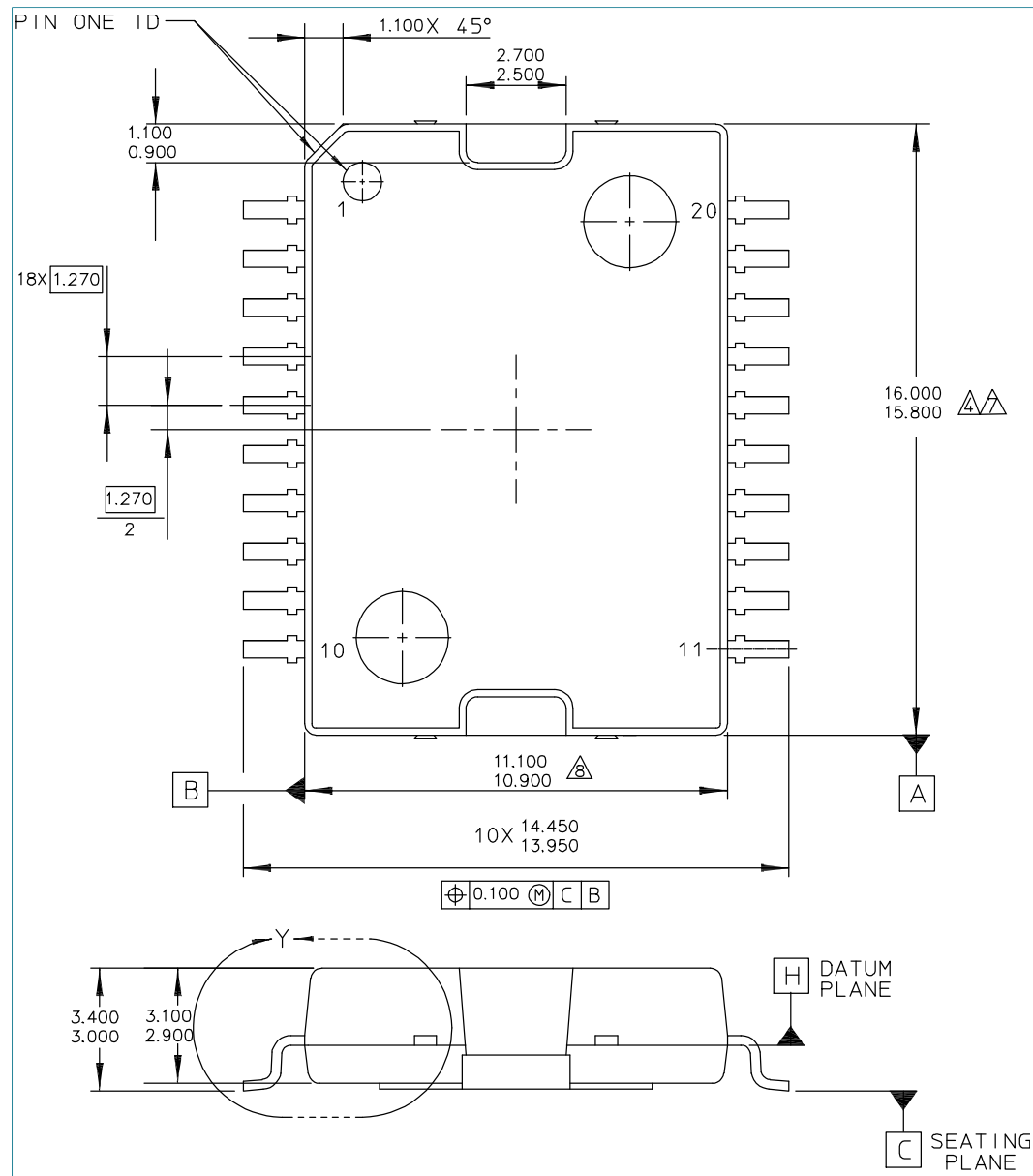
The 33887 packages are designed for thermal performance. The significant feature of these packages is the exposed pad on which the power die is soldered. When soldered to a PCB, this pad provides a path for heat flow to the ambient environment. The more copper area and thickness on the PCB, the better the power dissipation and transient behavior.

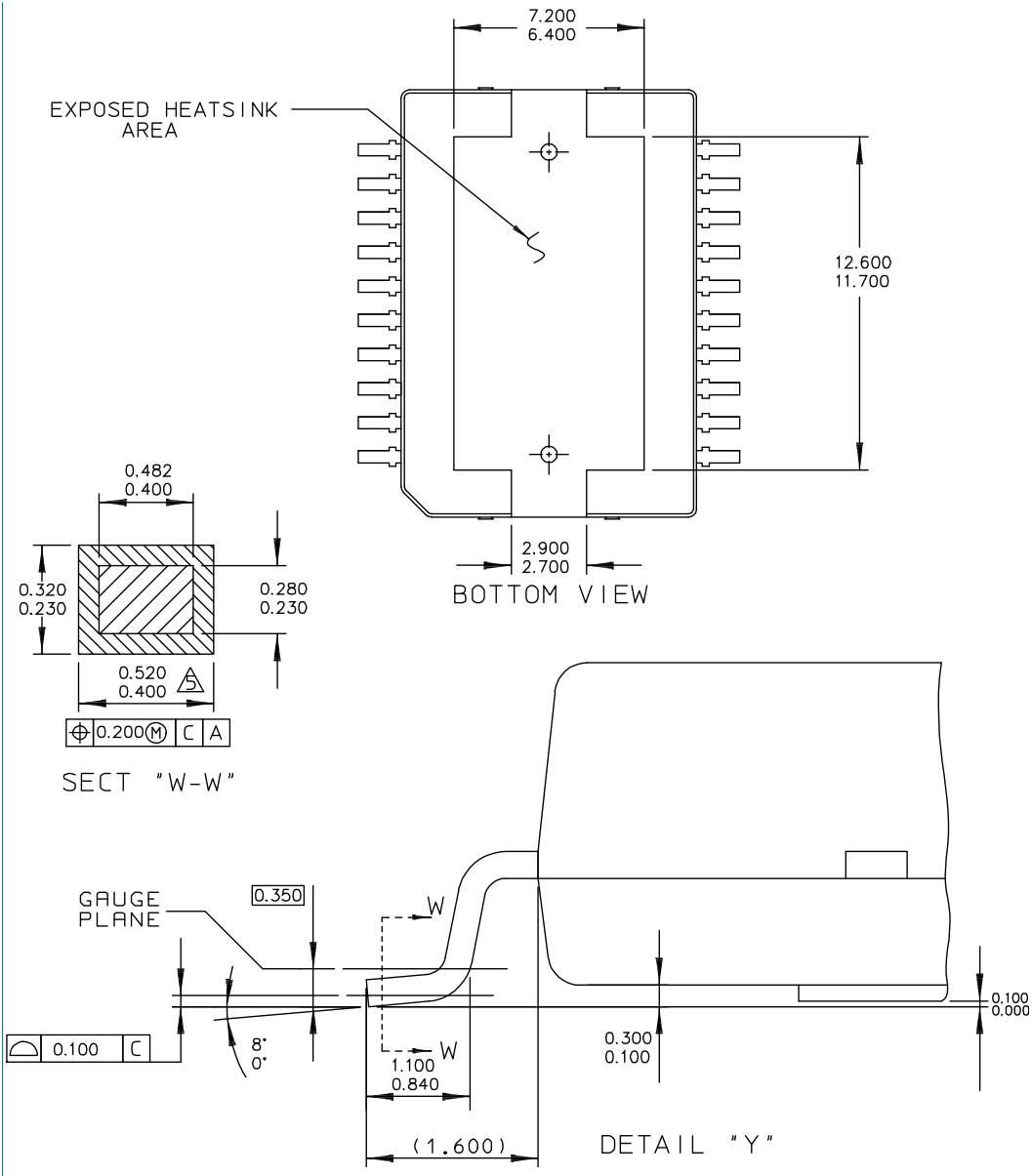
Example characterization on a double-sided PCB: bottom side area of copper is 7.8 cm^2 ; top surface is 2.7 cm^2 (see Figure 24); grid array of 24 vias 0.3 mm in diameter



17.2 Package outline

Important: The most current package outline is available at www.nxp.com.

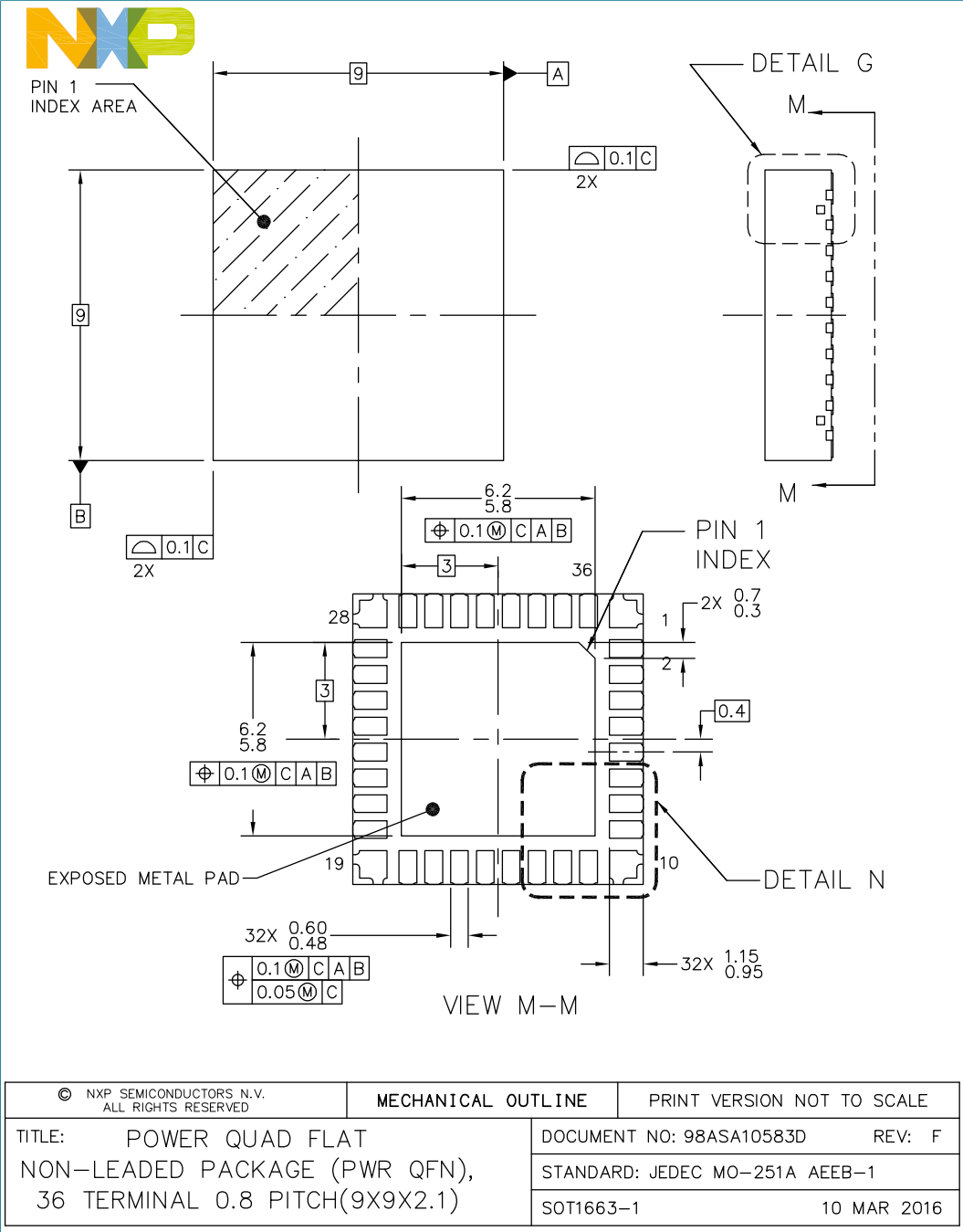




NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF THE LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.150 PER SIDE. THIS DIMENSION DOES INCLUDE MOLD MISMATCH AND IS DETERMINED AT DATUM H.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.
8. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.250 PER SIDE. THIS DIMENSION DOES INCLUDE MOLD MISMATCH AND IS DETERMINED AT DATUM H.

Figure 25. Package outline HSOP20 (SOT397-2)

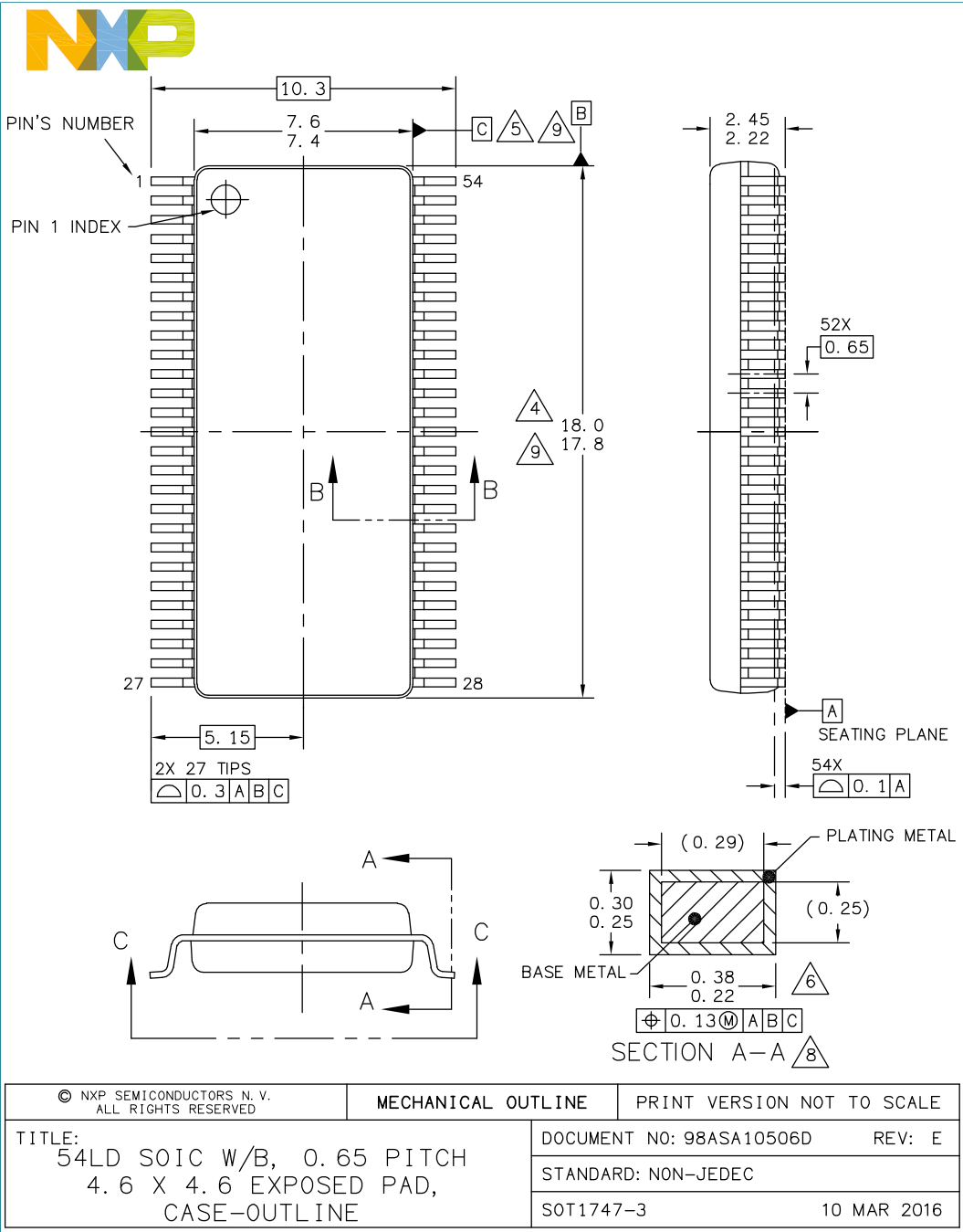


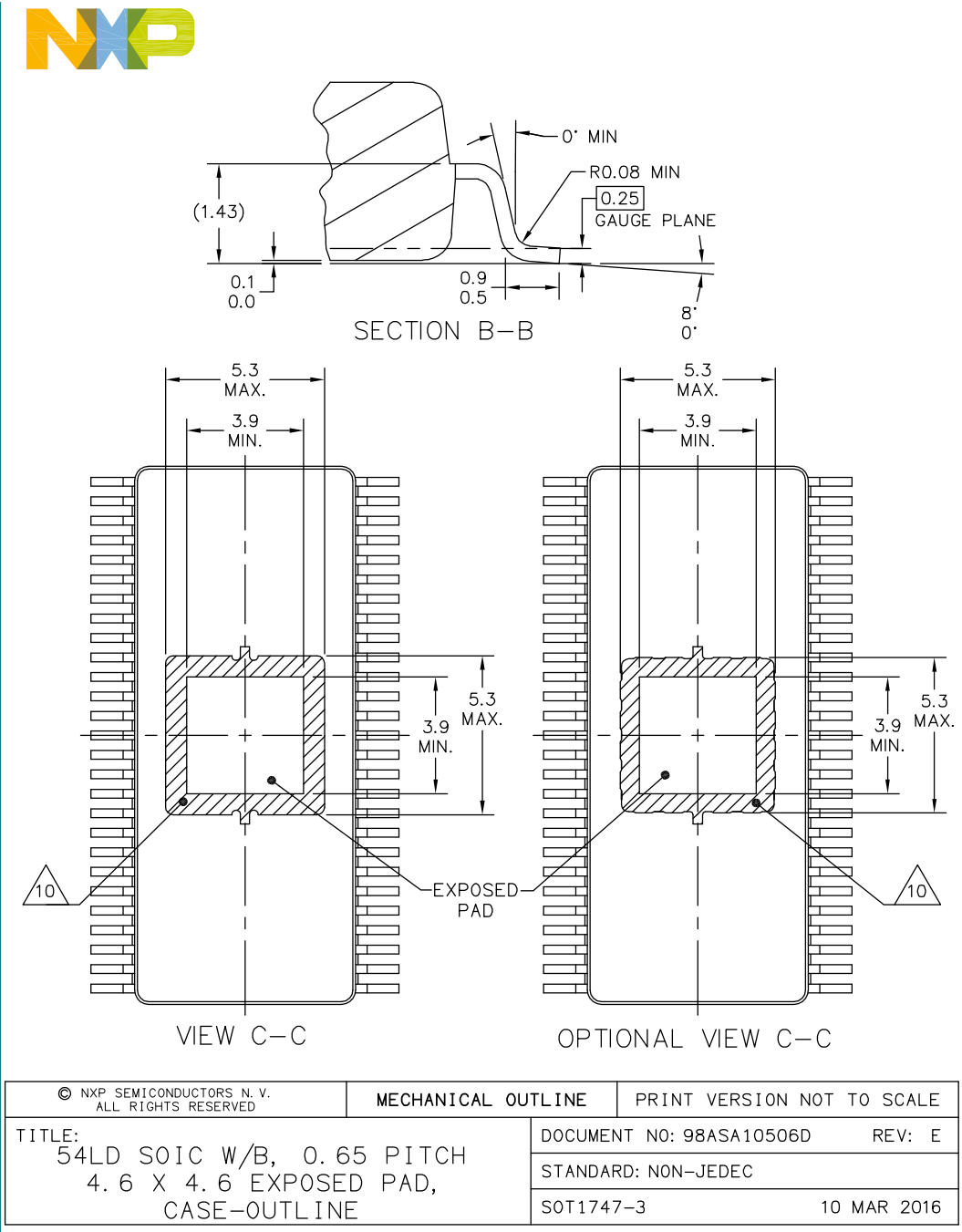


- NOTES:
- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 - 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - 3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: F-PQFP-N.
 - 4.  COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND EXPOSED PAD.
 - 5. MINIMUM METAL GAP SHOULD BE 0.25MM.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN), 36 TERMINAL 0.8 PITCH(9X9X2.1)	DOCUMENT NO: 98ASA10583D REV: F	
	STANDARD: JEDEC MO-251A AEEB-1	
	SOT1663-1	10 MAR 2016

Figure 26. Package outline HQFN (SOT1663-1)







NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
- 6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
- 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
- 9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- 10. HATCHED AREA TO BE KEEP-OUT ZONE FOR PCB ROUTING.

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH 4.6 X 4.6 EXPOSED PAD, CASE-OUTLINE	DOCUMENT NO: 98ASA10506D REV: E	
	STANDARD: NON-JEDEC	
	SOT1747-3	10 MAR 2016

Figure 27. Package outline HSOP54 (SOT1747-3)

18 Thermal addendum (rev. 2.0)

18.1 Introduction

This thermal addendum is provided as a supplement to the MC33887 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

18.2 Packaging and thermal considerations

The MC33887 is offered in a 20-pin HSOP exposed pad, single die package. There is a single heat source (P), a single junction temperature (T_J) and thermal resistance (R_{θJA}). This thermal addendum is specific to the 32-pin SOICW-EP package.

{T_J} = [R_{θJA}] · {P}

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to, and will not predict the performance of a package in an application-specific environment.

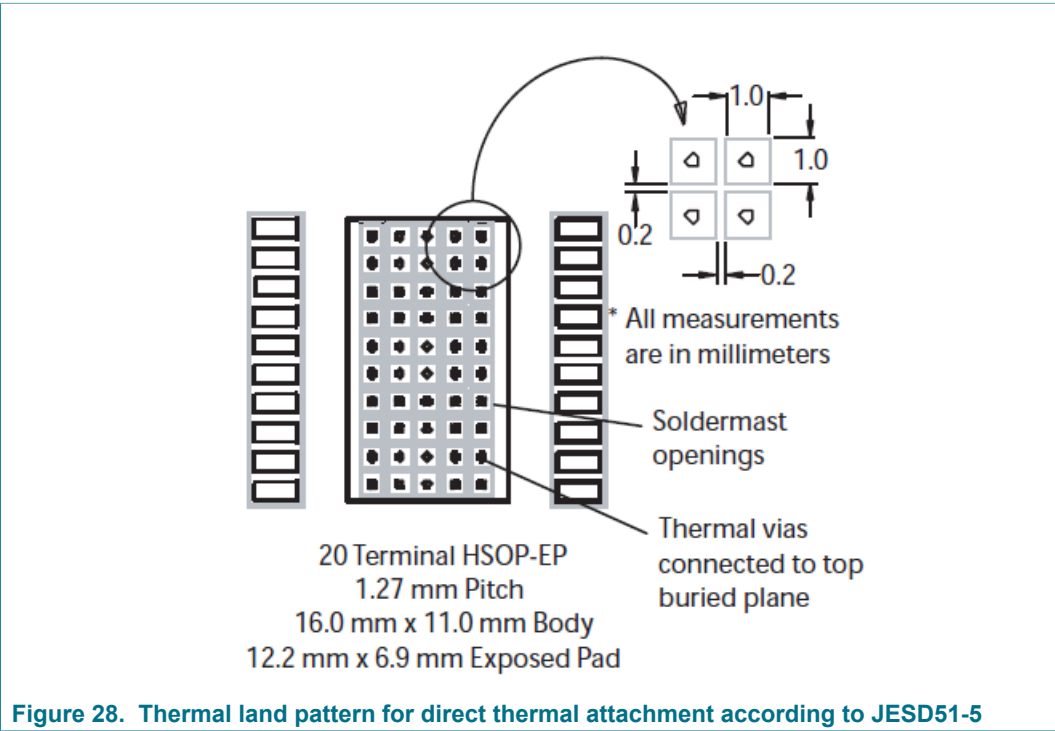
Stated values were obtained by measurement and simulation according to the standards listed in [Section 18.3 "Standards"](#).

18.3 Standards

Table 10. Thermal performance comparison

Thermal resistance	[°C/W]
R _{θJA} ^{[1][2]}	20
R _{θJB} ^{[2][3]}	6.0
R _{θJA} ^{[1][4]}	52
R _{θJC} ^[5]	1.0

- [1] Per JEDEC JESD51-2 at natural convection, still air condition.
- [2] 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
- [3] Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
- [4] Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
- [5] Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated.



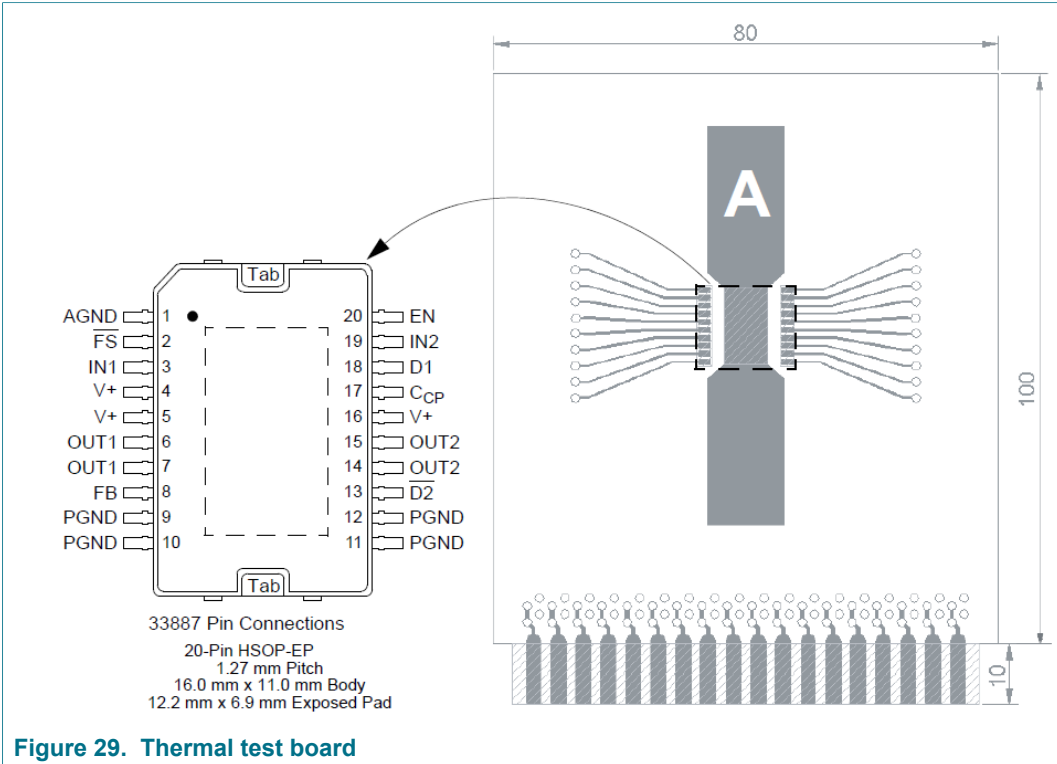


Figure 29. Thermal test board

18.4 Device on thermal test board

Material:	single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient conditions:	natural convection, still air

Table 11. Thermal resistance performance

Thermal resistance	Area A (mm ²)	°C/W
R _{θJA}	0.0	52
	300	36
	600	32
R _{θJS}	0.0	10
	300	7.0
	600	6.0

R_{θJA} is the thermal resistance between die junction and ambient air.

R_{θJS} is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package (see [Figure 29](#)).

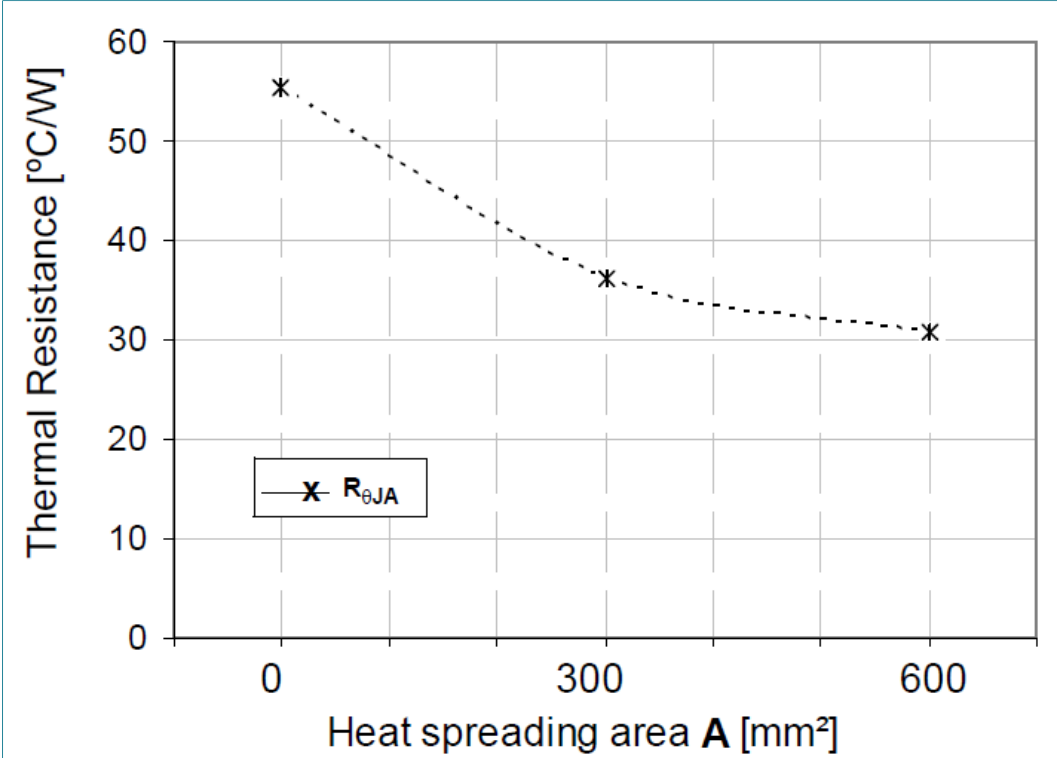


Figure 30. Device on thermal test board $R_{\theta JA}$

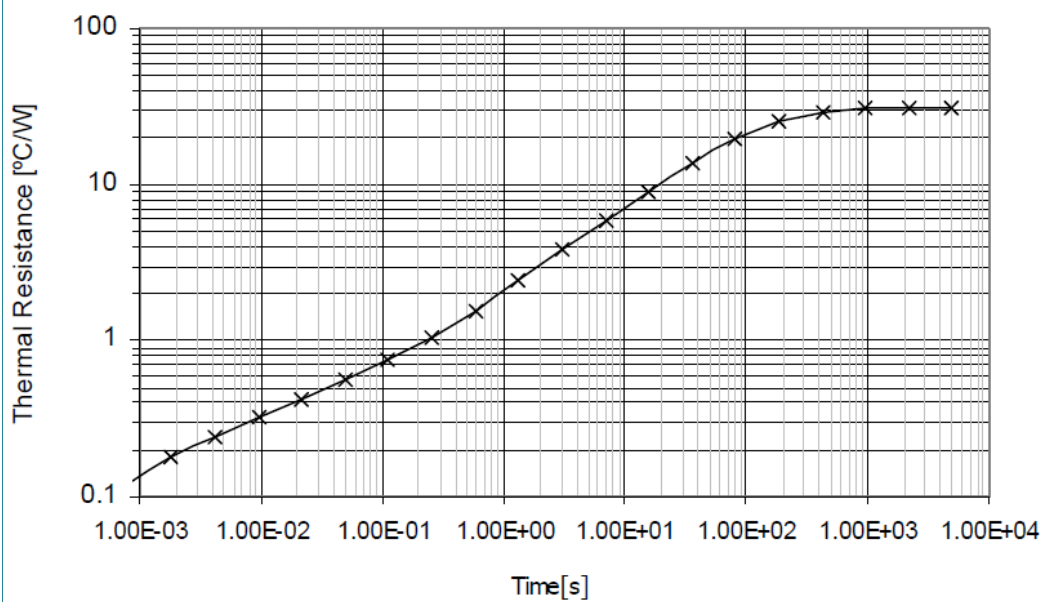


Figure 31. Transient thermal resistance $R_{\theta JA}$, device on thermal test board area $A = 600$ (mm^2)

19 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33887 v.17	9/2018	Technical Data	-	DOC_ID v.16
Modifications	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. - Added AEC-Q100 grade 1 qualified to Section 1 and Section 2 - Updated package drawings to comply with the new identity guidelines of NXP Semiconductors (no technical change)			
MC33887 v.16	10/2012	Technical Data	-	DOC_ID v.15
Modifications	Changed "my" to "may" in note "I_{LIM} blanking time is the time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act" for Table 8			
MC33887 v.15	9/2011	Technical Data	-	DOC_ID v.14
Modifications	- Removed the DH suffix information from Table 5 - Changed VW suffix HSOP, SOICW-EP, and PQFN ESD Voltage to ESD Voltage in Table 5 - Updated Freescale form and style			
MC33931 v.14	3/2011	Technical Data	-	DOC_ID v.13
Modifications	Removed part numbers MC33887APVW/R2, MC33887DH/R2, MC33887DWB/R2, MC33887AVW/R2, MC33887PNB/R2 and MCZ33887EK/R2 and replaced with part numbers MC33887APVW/R2, MC33887PFK/R2 and MC33887PEK/R2 in Table 1			
MC33887 v.13	10/2008	Technical Data	-	DOC_ID v.12
Modifications	Added part number MC33887AVW/R2 to Table 1			
MC33887 v.12	1/2007	Advance information	-	DOC_ID v.11
Modifications	- Modified third paragraph in Section 1 - Updated Section 2 (altered feature number 1 and added feature number 2) - Changed maximum supply voltage (-0.3 to 40 V) in Table 5 - Added note "Performance at voltages greater than 28V is degraded. See Section 13 for typical performance. Extended operation at higher voltages has not been fully characterized and may reduce the operational lifetime" to Table 5 - Updated note "Specifications are characterized over the range of 5.0 V ≤ V₊ ≤ 28 V. See Section 13 and Section 14 for information about operation outside of this range" in Table 7 - Added a third paragraph to Section 14.2.2 - Replaced Figure 20, Figure 21, and Figure 22 with updated information			
MC33887 v.11	11/2006	Advance information	-	DOC_ID v.10
Modifications	- Updated ordering information block with new epp information - Changed the supply/operating voltage from 40 V to 28 V - Updated all package drawings to the current revision - Adjusted to match device performance characteristics - Updated the document to the prevailing Freescale form and style - Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Section 7 - Added note "NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes and enter the core ID) to view all orderable parts, and review parametrics" to Table 6 - Added MCZ33887EK/R2 to Table 1 - Removed the 33887A from the data sheet and deleted Product Variation section now that is no longer needed			
MC33887 v.10	7/2005	Advance information	-	DOC_ID v.9.0
Modifications	- Added thermal addendum and converted to Freescale format, revised PQFN drawing, made several minor spelling corrections - Added 33887A			

20 Legal information

20.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
[short] Data sheet: product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
[short] Data sheet: advance information	Qualification	This document contains information on a new product. Specifications and information herein are subject to change without notice.
[short] Data sheet: technical data	Production	This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a technical data data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the technical data data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

SMARTMOS — is a trademark of NXP B.V.

Tables

Tab. 1.	Ordering information	2	Tab. 7.	Static characteristics	8
Tab. 2.	HSOP20 pin description	4	Tab. 8.	Dynamic characteristics	9
Tab. 3.	HQFN36 pin description	5	Tab. 9.	Truth table	18
Tab. 4.	HSOP54 pin description	6	Tab. 10.	Thermal performance comparison	33
Tab. 5.	Maximum ratings	6	Tab. 11.	Thermal resistance performance	34
Tab. 6.	Thermal characteristics	7	Tab. 12.	Revision history	36

Figures

Fig. 1.	Simplified application diagram	1	Fig. 16.	Output voltage and current vs. input voltage at $V_+ = 24$ V, PWM frequency of 10 kHz, and duty cycle of 50 %	14
Fig. 2.	Block diagram	3	Fig. 17.	Output voltage and current vs. input voltage at $V_+ = 24$ V, PWM frequency of 10 kHz, and duty cycle of 90 %	15
Fig. 3.	Pin configuration for HSOP20	3	Fig. 18.	Output voltage and current vs. input voltage at $V_+ = 12$ V, PWM frequency of 20 kHz, and duty cycle of 50 % for a purely resistive load ...	15
Fig. 4.	Pin configuration for HQFN36	4	Fig. 19.	Output voltage and current vs. input voltage at $V_+ = 12$ V, PWM frequency of 20 kHz, and duty cycle of 90 % for a purely resistive load ...	16
Fig. 5.	Pin configuration for HSOP54	4	Fig. 20.	Typical high-side $R_{DS(on)}$ versus V_+	16
Fig. 6.	Output delay time	10	Fig. 21.	Typical low-side $R_{DS(on)}$ versus V_+	17
Fig. 7.	Disable delay time	10	Fig. 22.	Typical quiescent supply current versus V_+	17
Fig. 8.	Output switching time	10	Fig. 23.	Typical application schematic	22
Fig. 9.	Active current limiting versus temperature (typical)	10	Fig. 24.	PCB test layout	23
Fig. 10.	Operating states	11	Fig. 25.	Package outline HSOP20 (SOT397-2)	24
Fig. 11.	Example short-circuit detection detail on low-side MOSFET	11	Fig. 26.	Package outline HQFN (SOT1663-1)	27
Fig. 12.	Output voltage and current vs. input voltage at $V_+ = 24$ V, PWM frequency of 1.0 kHz, and duty cycle of 10 %	12	Fig. 27.	Package outline HSOP54 (SOT1747-3)	30
Fig. 13.	Output voltage and current vs. input voltage at $V_+ = 24$ V, PWM frequency of 1.0 kHz, and duty cycle of 50 %	13	Fig. 28.	Thermal land pattern for direct thermal attachment according to JESD51-5	33
Fig. 14.	Output voltage and current vs. input voltage at $V_+ = 34$ V, PWM frequency of 1.0 kHz, and duty cycle of 90 %, showing device in current limiting mode	13	Fig. 29.	Thermal test board	34
Fig. 15.	Output voltage and current vs. input voltage at $V_+ = 22$ V, PWM frequency of 1.0 kHz, and duty cycle of 90 %	14	Fig. 30.	Device on thermal test board R0JA	35
			Fig. 31.	Transient thermal resistance R0JA, device on thermal test board area A = 600 (mm ²)	35

Contents

1	General description	1
2	Features and benefits	2
3	Applications	2
4	Ordering information	2
5	Block diagram	3
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Maximum ratings	6
8	Thermal characteristics	7
9	Static characteristics	8
10	Dynamic characteristics	9
11	Timing diagrams	10
12	Typical switching waveforms	11
13	Electrical performance curves	16
14	Functional description	18
14.1	Introduction	18
14.2	Functional pin description	18
14.2.1	Power ground and analog ground (PGND and AGND)	18
14.2.2	Positive power supply (V+)	18
14.2.3	Fault status (FS)	19
14.2.4	Logic input control and disable (IN1, IN2, D1, and D2)	19
14.2.5	H-bridge output (OUT1, OUT2)	19
14.2.6	Charge pump capacitor (CCP)	19
14.2.7	Enable (EN)	19
14.2.8	Feedback for H-bridge (FB)	20
15	Functional device operation	20
15.1	Operational modes	20
15.2	Protection and diagnostic features	21
15.2.1	Short-circuit protection	21
15.2.2	Active current limiting	21
15.2.3	Output avalanche protection	21
15.2.4	Overtemperature shutdown and hysteresis	21
16	Typical applications	22
17	Packaging	22
17.1	Soldering information	22
17.2	Package outline	23
18	Thermal addendum (rev. 2.0)	32
18.1	Introduction	32
18.2	Packaging and thermal considerations	33
18.3	Standards	33
18.4	Device on thermal test board	34
19	Revision history	36
20	Legal information	37

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2018.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 September 2018
Document identifier: MC33887