#### March 2004



#### AS7C3513B

#### **Features**

- Industrial and commercial temperature
- Organization: 32,768 words  $\times$  16 bits
- Center power and ground pins
- High speed
- 10/12/15/20 ns address access time
- 5, 6, 7, 8 ns output enable access time
- Low power consumption: ACTIVE
- 288 mW / max @ 10 ns
- Low power consumption: STANDBY
- 18 mW / max CMOS
- 6T 0.18m CMOS Technology

- Easy memory expansion with  $\overline{CE}$ ,  $\overline{OE}$  inputs
- TTL-compatible, three-state I/O
- 44-pin JEDEC standard package
- 400 mil SOJ
- 400 mil TSOP 2
- ESD protection  $\geq$  2000 volts
- Latch-up current  $\geq 200 \text{ mA}$

# Logic block diagram $A0 \xrightarrow{A0} \xrightarrow{1} \xrightarrow{1} \xrightarrow{1}$

#### V<sub>CC</sub> decoder A2 $32K \times 16$ - GND A3 Array A4 Row A5 A6 Α7 I/O buffer I/O0–I/O7 Control circuit I/O8-I/O15 Column decoder WE A12-AII UB-OE LB CE

#### **Pin arrangement**

44-Pin SOJ, TSOP 2 (400 mil)

NC	1 (	)	44	A4
A3	2		43	A5
A2	3		42	A6
A1	4		41	OE
A0	5		40	UB
CE	6		39	LB
I/O0	7		38	I/O15
I/O1	8	В	37	I/O14
I/O2	9	C3513B	36	I/O13
I/O3	10	5	35	I/O12
V <sub>CC</sub>	11	3	34	GND
GND	12	ĸ	33	V <sub>CC</sub>
I/O4	13	AS7(	32	I/011
I/O5	14	<,	31	I/O10
I/O6	15		30	I/O9
I/O7	16		29	I/O8
WE	17		28	NC
A14	18		27	A7
A13	19		26	A8
A12	20		25	A9
A11	21		24	A10
NC	22		23	NC

#### **Selection guide**

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	80	75	70	65	mA
Maximum CMOS standby current	5	5	5	5	mA

P.1 of 10

#### **Functional description**

The AS7C3513B is a high performance CMOS 524,288-bit Static Random Access Memory (SRAM) device organized as 32,768 words  $\times 16$  bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times  $(t_{AA}, t_{RC}, t_{WC})$  of 10/12/15/20 ns with output enable access times  $(t_{OE})$  of 5, 6, 7, 8 ns are ideal for high performance applications. The chip enable input  $\overline{CE}$  permits easy memory expansion with multiple-bank memory systems.

When  $\overline{CE}$  is high, the device enters standby mode. If inputs are still toggling, the device consumes I<sub>SB</sub> power. If the bus is static, then the full standby power is reached (I<sub>SB1</sub>). The AS7C3513B is guaranteed not to exceed 18mW power consumption under nominal full standby conditions.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ), ( $\overline{UB}$ ) and/or ( $\overline{LB}$ ), and chip enable ( $\overline{CE}$ ). Data on the input pins I/O0 - I/O7, and/or I/O8 – I/O15, is written on the rising edge of  $\overline{WE}$  (write cycle 1) or  $\overline{CE}$  (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable  $(\overline{OE})$ ,  $(\overline{UB})$  and  $(\overline{LB})$ , and chip enable  $(\overline{CE})$ , with write enable  $(\overline{WE})$  high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, or  $(\overline{UB})$  and  $(\overline{LB})$ , output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read.  $\overline{LB}$  controls the lower bits, I/O0 – I/O7, and  $\overline{UB}$  controls the higher bits, I/O8 – I/O15.

All chip inputs and outputs are TTL-compatible. The AS7C3513B is packaged in common industry standard packages.

#### **Absolute maximum ratings**

Parameter	Symbol	Min	Max	Unit
Voltage on V <sub>CC</sub> relative to GND	V <sub>t1</sub>	-0.50	+5.0	V
Voltage on any pin relative to GND	V <sub>t2</sub>	-0.50	V <sub>CC</sub> +0.50	V
Power dissipation	P <sub>D</sub>	_	1.0	W
Storage temperature (plastic)	T <sub>stg</sub>	-65	+150	° C
Ambient temperature with $\mathrm{V}_{\mathrm{CC}}$ applied	T <sub>bias</sub>	-55	+125	° C
DC current into outputs (low)	I <sub>OUT</sub>	_	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **Truth table**

CE	WE	OE	LB	UB	I/O0–I/O7	I/O8–I/O15	Mode
Н	Х	Х	Х	Х	High Z	High Z	Standby $(I_{SB}, I_{SBI})$
L	Н	L	L	Н	D <sub>OUT</sub>	High Z	Read I/O0–I/O7 (I <sub>CC</sub> )
L	Н	L	Н	L	High Z	D <sub>OUT</sub>	Read I/O8–I/O15 (I <sub>CC</sub> )
L	Н	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	Read I/O0–I/O15 (I <sub>CC</sub> )
L	L	Х	L	L	D <sub>IN</sub>	D <sub>IN</sub>	Write I/O0–I/O15 (I <sub>CC</sub> )
L	L	Х	L	Н	D <sub>IN</sub>	High Z	Write I/O0–I/O7 (I <sub>CC</sub> )
L	L	Х	Н	L	High Z	D <sub>IN</sub>	Write I/O8–I/O15 (I <sub>CC</sub> )
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I <sub>CC</sub> )

Key: X = Don't care; L = Low; H = High



#### **Recommended operating conditions**

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	
Imput volta an	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> + 0.5		
input voitage	Input voltage			-	0.8	V
	commercial	T <sub>A</sub>	0	-	70	° C
Ambient operating temperature	industrial	T <sub>A</sub>	-40	-	85	° C

 $V_{IL}$  = -1.0V for pulse width less than 5ns

 $V_{IH} = V_{CC} + 1.5V$  for pulse width less than 5ns

### DC operating characteristics (over the operating range) $^{I}$

			-1	10	-1	12	-1	15	-20		
Parameter	Sym	Test conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>CC</sub> = Max V <sub>IN</sub> = GND to V <sub>CC</sub>	_	1	١	1	I	1	I	1	μA
Output leakage current	I <sub>LO</sub>	V <sub>CC</sub> = Max V <sub>OUT</sub> = GND to V <sub>CC</sub>	_	1	I	1		1	I	1	μA
Operating power supply current	I <sub>CC</sub>	$V_{CC} = Max, \overline{CE} \le V_{IL}$ f = f <sub>Max</sub> , I <sub>OUT</sub> = 0mA	_	80	Ι	75	I	70		65	mA
o. 11	I <sub>SB</sub>	$V_{CC} = Max, \overline{CE} \ge V_{IH}$ $f = f_{Max}$	-	30	Ι	25		20		20	mA
Standby power supply current	I <sub>SB1</sub>	$\begin{split} V_{CC} &= Max, \ \overline{CE} \geq V_{CC} 0.2V \\ V_{IN} \leq 0.2V \ \text{or} \ V_{IN} \geq V_{CC} 0.2V, \\ f &= 0 \end{split}$	_	5	Ι	5	l	5	l	5	mA
Output voltage	V <sub>OL</sub>	$I_{OL}$ = 8 mA, $V_{CC}$ = Min	_	0.4	-	0.4	_	0.4	_	0.4	V
Output voltage	V <sub>OH</sub>	$I_{OH}$ = -4 mA, $V_{CC}$ = Min	2.4	_	2.4	_	2.4	_	2.4	-	V

#### Capacitance (f = 1MHz, $T_a = 25^{\circ}$ C, $V_{CC} = NOMINAL)^2$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C <sub>IN</sub>	A, $\overline{\text{CE}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ , $\overline{\text{LB}}$ , $\overline{\text{UB}}$	$V_{in} = 0V$	5	pF
I/O capacitance	C <sub>I/O</sub>	I/O	$V_{in} = V_{out} = 0V$	7	pF



# Read cycle (over the operating range) <sup>3,9</sup>

		-10 -12		2	-1	15	-20				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	10		12		15		20		ns	
Address access time	t <sub>AA</sub>	Ι	10	Ι	12	Ι	15	Ι	20	ns	3
Chip enable ( $\overline{CE}$ ) access time	t <sub>ACE</sub>	Ι	10	Ι	12	Ι	15	Ι	20	ns	3
Output enable $(\overline{OE})$ access time	t <sub>OE</sub>	Ι	5	Ι	6	Ι	7	Ι	8	ns	
Output hold from address change	t <sub>OH</sub>	3	_	3	_	3	_	3	_	ns	5
$\overline{\text{CE}}$ low to output in low Z	t <sub>CLZ</sub>	3	-	3	-	3	-	3	-	ns	4,5
$\overline{\text{CE}}$ high to output in high Z	t <sub>CHZ</sub>	-	3	-	3	_	4	-	5	ns	4,5
$\overline{OE}$ low to output in low Z	t <sub>OLZ</sub>	0	-	0	-	0	-	0	-	ns	4,5
Byte select access time	t <sub>BA</sub>	-	5	-	6	_	7	-	8	ns	
Byte select Low to low Z	t <sub>BLZ</sub>	0	-	0	-	0	-	0	-	ns	4,5
Byte select High to high Z	t <sub>BHZ</sub>	-	5	-	6	_	6	-	8	ns	4,5
$\overline{\text{OE}}$ high to output in high Z	t <sub>OHZ</sub>	-	5	-	6	_	7	-	8	ns	4,5
Power up time	t <sub>PU</sub>	0		0		0		0		ns	4,5
Power down time	t <sub>PD</sub>	-	10	-	12	-	15		20	ns	4,5

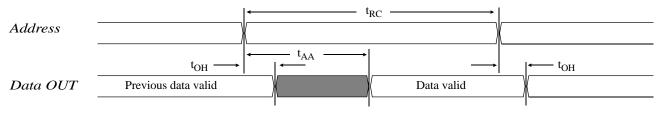
#### Key to switching waveforms

Rising input

\_\_\_\_\_

Undefined output/don't care

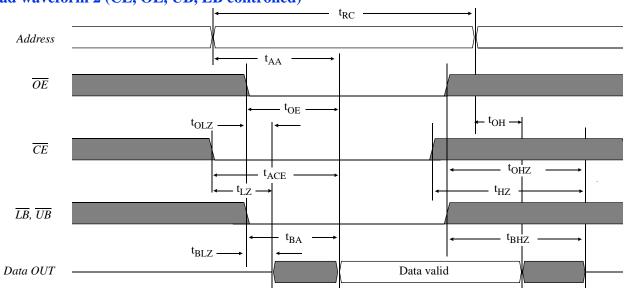
# Read waveform 1 (address controlled)<sup>3,6,7,9</sup>



— Falling input



# Read waveform 2 (CE, OE, UB, LB controlled)<sup>3,6,8,9</sup>

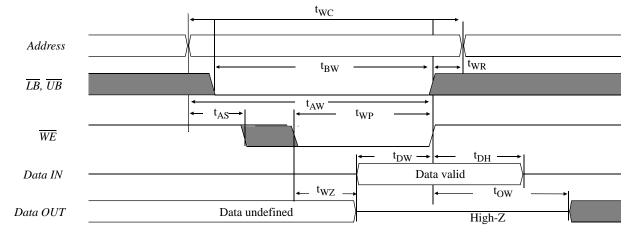


# Write cycle (over the operating range)<sup>11</sup>

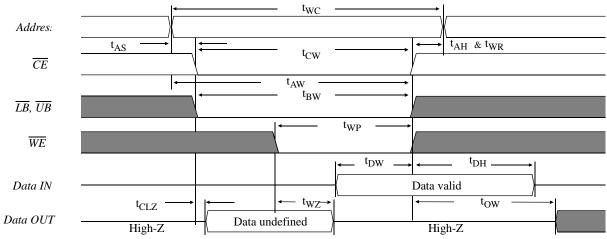
		-10		-1	12	-15		-2	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	10	_	12	_	15	_	20	_	ns	
Chip enable ( $\overline{CE}$ ) to write end	t <sub>CW</sub>	8	-	9	_	10	-	12	-	ns	
Address setup to write end	t <sub>AW</sub>	8	-	9	_	10	-	12	-	ns	
Address setup time	t <sub>AS</sub>	0	-	0	-	0	-	0	_	ns	
Write pulse width	t <sub>WP</sub>	7	-	8	-	9	-	12	_	ns	
Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	0	_	ns	
Address hold from end of write	t <sub>AH</sub>	0	-	0	-	0	-	0	_	ns	
Data valid to write end	t <sub>DW</sub>	5	-	6	-	8	-	10	_	ns	
Data hold time	t <sub>DH</sub>	0	-	0	-	0	-	0	_	ns	5
Write enable to output in high Z	t <sub>WZ</sub>	_	5	_	6	-	7	_	8	ns	4,5
Output active from write end	t <sub>OW</sub>	1	_	1	_	1	_	2	_	ns	4,5
Byte select low to end of write	t <sub>BW</sub>	7	_	8	_	9	-	9	_	ns	



# Write waveform 1(WE controlled)<sup>11</sup>

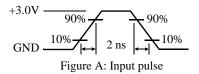


# Write waveform 2 (CE controlled)<sup>11</sup>



#### AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.



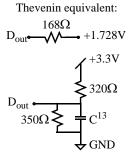
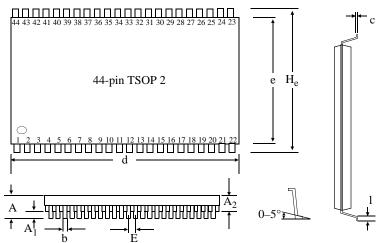


Figure B: 3.3V Output load

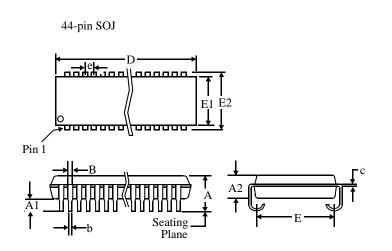
#### Notes

- $1 \quad \text{During } V_{\text{CC}} \text{ power-up, a pull-up resistor to } V_{\text{CC}} \text{ on } \overline{\text{CE}} \text{ is required to meet } I_{\text{SB}} \text{ specification.}$
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4 These parameters are specified with  $C_L = 5pF$ , as in Figure B. Transition is measured  $\pm 500mV$  from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- $\overline{\text{WE}}$  is High for read cycle.
- 7  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  are Low for read cycle.
- 8 Address valid prior to or coincident with  $\overline{\text{CE}}$  transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 Not applicable.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13 C=30pF, except on High Z and Low Z parameters, where C=5pF.

## AS7C3513B



	44-pin TSOP 2					
Symbol	Min (mm)	Max (mm)				
А		1.2				
A <sub>1</sub>	0.05	0.15				
$A_2$	0.95	1.05				
b	0.3	0.45				
с	0.12	0.21				
d	18.31	18.52				
e	10.06	10.26				
H <sub>e</sub>	11.68	11.94				
Е	0.80 (typical)					
1	0.40	0.60				



	44-pin SOJ 400 mil					
Symbol	Min	Max				
А	0.128	0.148				
A1	0.025	-				
A2	0.105	0.115				
В	0.026	0.032				
b	0.015	0.020				
с	0.007	0.013				
D	1.120	1.130				
Е	0.370	NOM				
E1	0.395	0.405				
E2	0.435	0.445				
e	0.050 NOM					

# Package dimensions



#### **Ordering codes**

Package\A	ccess time	<b>10 ns</b>	<b>12 ns</b>	15 ns	20 ns
Plastic SOJ, 400	Commercial	AS7C3513B-10JC	AS7C3513B-12JC	AS7C3513B-15JC	AS7C3513B-20JC
mil	Industrial	AS7C3513B-10JI	AS7C3513B-12JI	AS7C3513B-15JI	AS7C3513B-20JI
TSOP 2,	Commercial	AS7C3513B-10TC	AS7C3513B-12TC	AS7C3513B-15TC	AS7C3513B-20TC
18.4×10.2 mm	Industrial	AS7C3513B-10TI	AS7C3513B-12TI	AS7C3513B-15TI	AS7C3513B-20TI

Note:

Add suffix 'N' to the above part number for lead free parts (Ex. AS7C3513B-10JCN)

#### Part numbering system

AS7C	3	513B	-XX	X	С	X
SRAM prefix	Voltage: 3.3V CMOS	Device number	Access time	Package: J = SOJ 400 mil T =TSOP 2 18.4×10.2 mm	Temperature range: C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C	N=Lead Free Part



Alliance Semiconductor Corporation 2575, Augustine Drive, Santa Clara, CA 95054 Tel: 408 - 855 - 4900 Fax: 408 - 855 - 4999

www.alsc.com

Copyright © Alliance Semiconductor All Rights Reserved Part Number: AS7C3513B Document Version: v.1.2

© Copyright 2003 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warrantes related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life suporting systems i