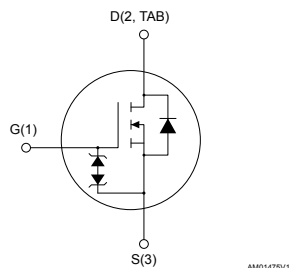
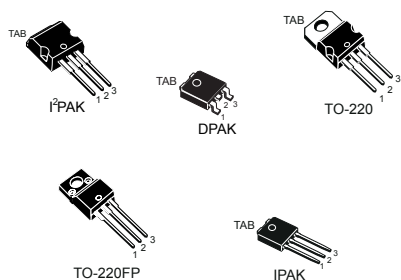


N-channel 500 V, 1.22 Ω typ., 4.4 A SuperMESH™ Power MOSFETs in I²PAK, DPAK, TO-220, TO-220FP and IPAK packages



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D	Package
STB5NK50Z-1	500 V	1.5 Ω	4.4 A	I ² PAK
STD5NK50ZT4				DPAK
STP5NK50Z				TO-220
STP5NK50ZFP				TO-220FP
STU5NK50Z				IPAK

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STB5NK50Z-1](#)

[STD5NK50ZT4](#)

[STP5NK50Z](#)

[STP5NK50ZFP](#)

[STU5NK50Z](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I ² PAK, DPAK, TO-220, IPAK	TO-220FP	
V _{DS}	Drain-source voltage	500		V
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	4.4	4.4 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	2.7	2.7 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	17.6	17.6 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	70	25	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	3		kV
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T _C = 25 °C)		2.5	kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
T _j	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 4.4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}.

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		I ² PAK, TO-220	TO-220FP	DPAK	IPAK	
R _{thj-case}	Thermal resistance junction-case	1.78	5	1.78		°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5			100	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb			50		°C/W

1. When mounted on an 1-inch² FR-4, 2oz Cu board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j Max)	4.4	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	130	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.2\text{ A}$		1.22	1.5	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	535		pF
C_{oss}	Output capacitance			75		
C_{rss}	Reverse transfer capacitance			17		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	45		pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 4.4\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	20	28	nC
Q_{gs}	Gate-source charge			4		
Q_{gd}	Gate-drain charge			10		

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 2.2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	15	-	ns
t_r	Rise time			10		
$t_{d(off)}$	Turn-off delay time			32		
t_f	Fall time			15		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		4.4	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				17.6	
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 4.4 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 4.4 A, di/dt = 100 A/μs V _{DD} = 30 V, T _j = 150°C (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	310		ns
Q _{rr}	Reverse recovery charge			1.425		μC
I _{RRM}	Reverse recovery current			9.2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for I²PAK, DPAK, TO-220, IPAK

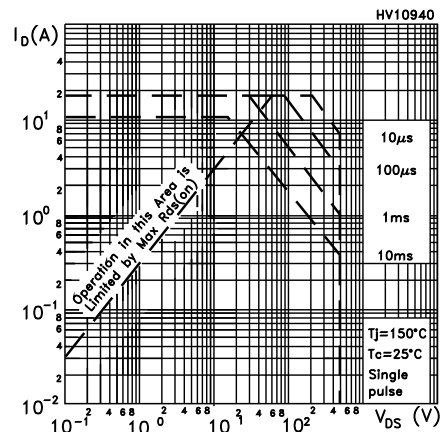


Figure 2. Thermal impedance for I²PAK, DPAK, TO-220, IPAK

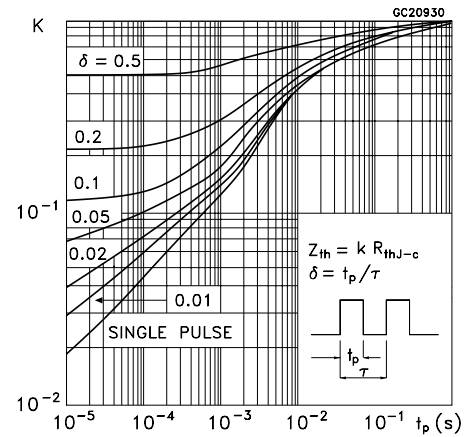


Figure 3. Safe operating area for TO-220FP

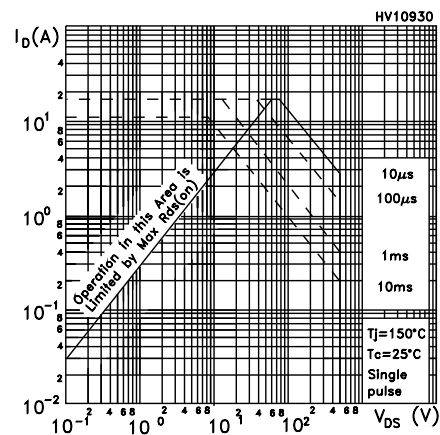


Figure 4. Thermal impedance for TO-220FP

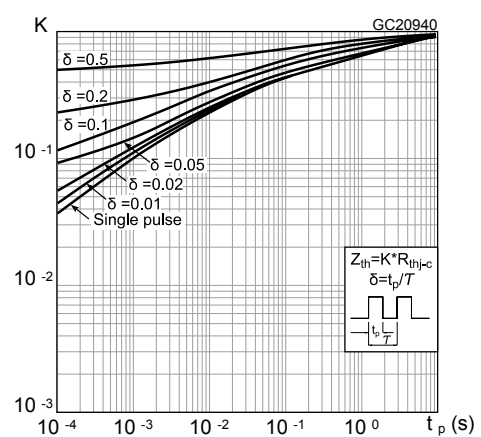


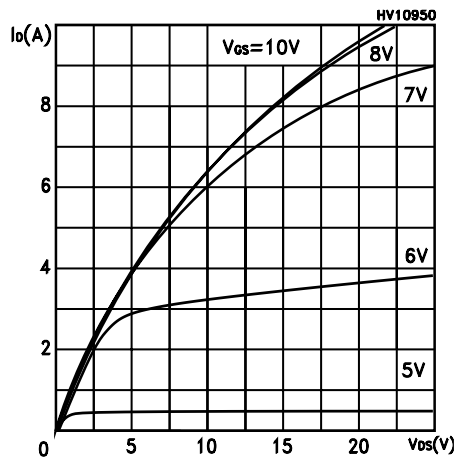
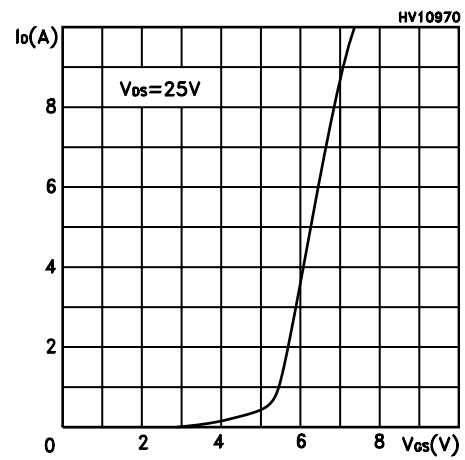
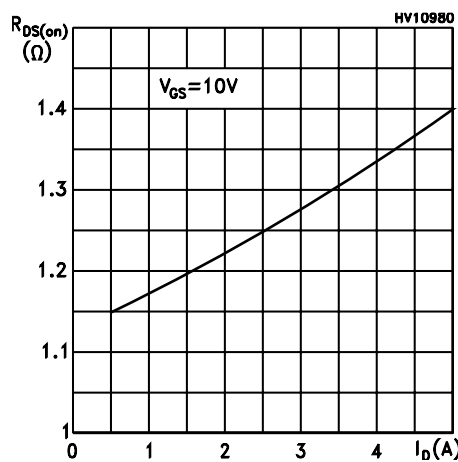
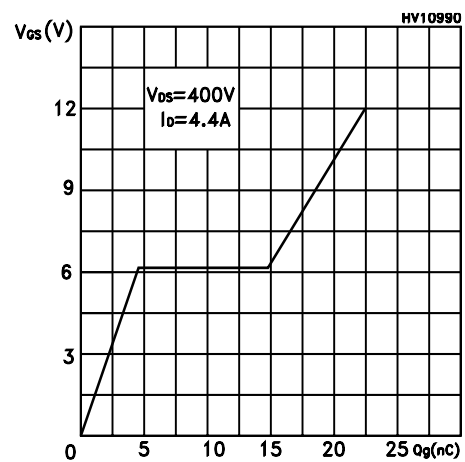
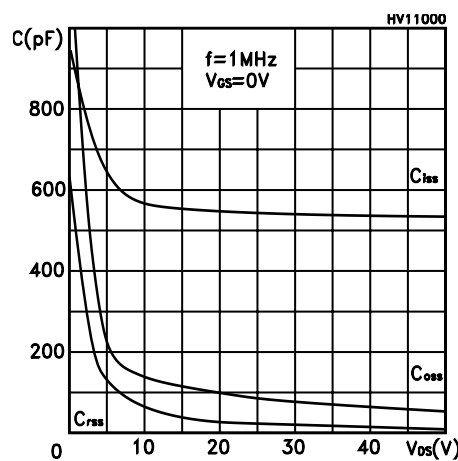
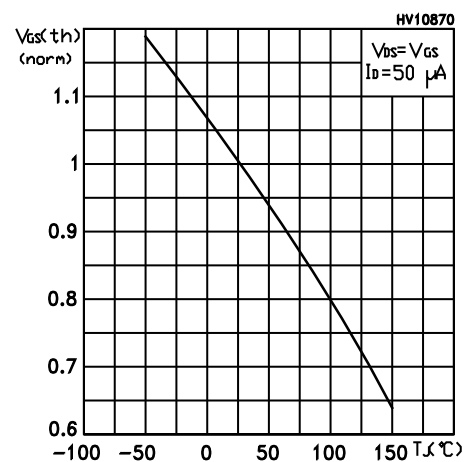
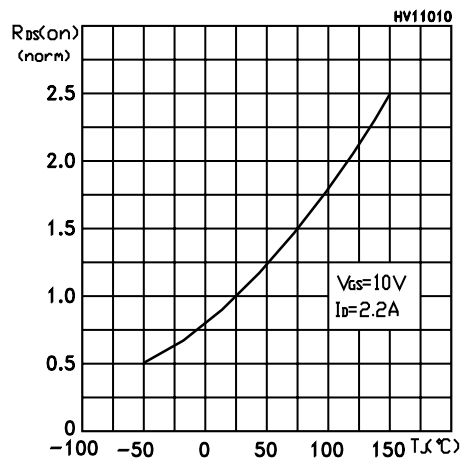
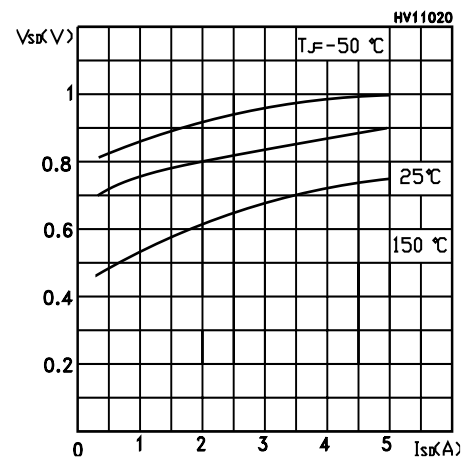
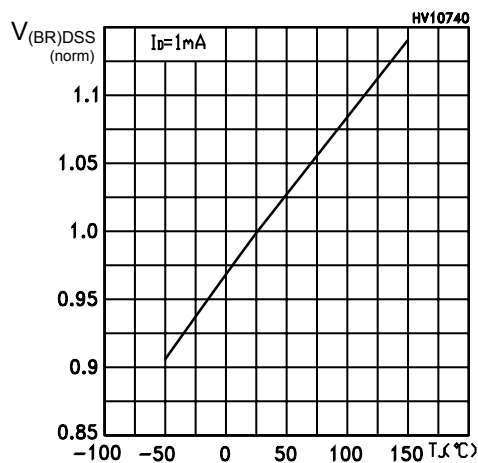
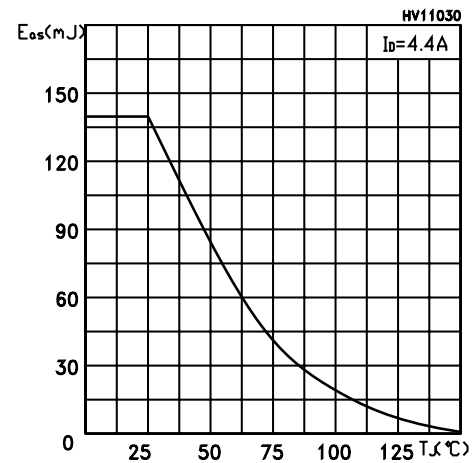
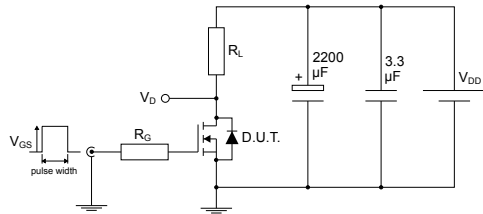
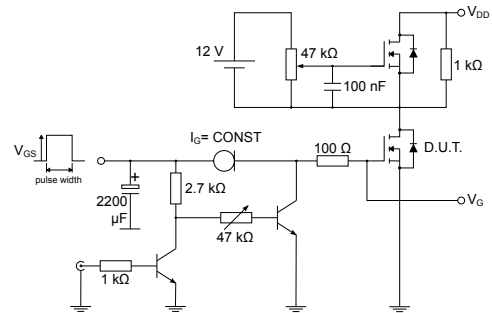
Figure 5. Output characteristics

Figure 6. Transfer characteristics

Figure 7. Static drain-source on resistance

Figure 8. Gate charge vs gate-source voltage

Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage vs temperature


Figure 11. Normalized on resistance vs temperature

Figure 12. Source-drain diode forward characteristic

Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

Figure 14. Maximum avalanche energy vs temperature


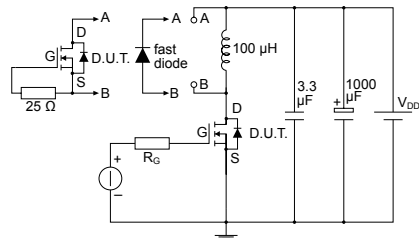
3 Test circuits

Figure 15. Test circuit for resistive load switching times


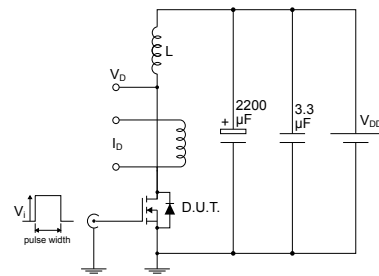
AM01468v1

Figure 16. Test circuit for gate charge behavior


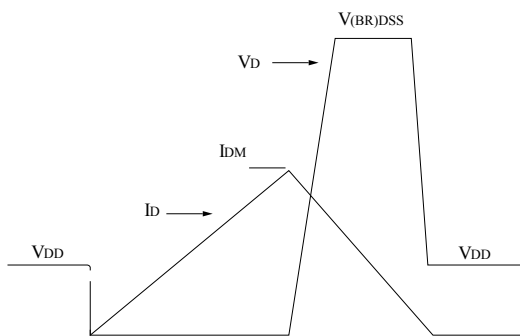
AM01469v1

Figure 17. Test circuit for inductive load switching and diode recovery times


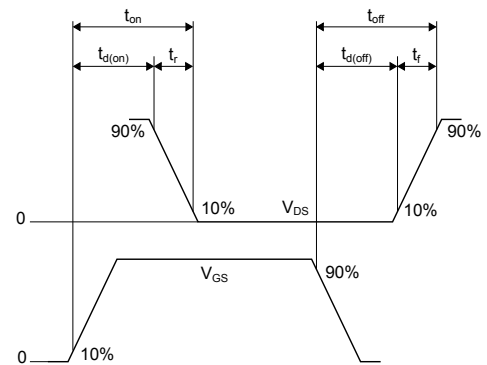
AM01470v1

Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


AM01472v1

Figure 20. Switching time waveform


AM01473v1

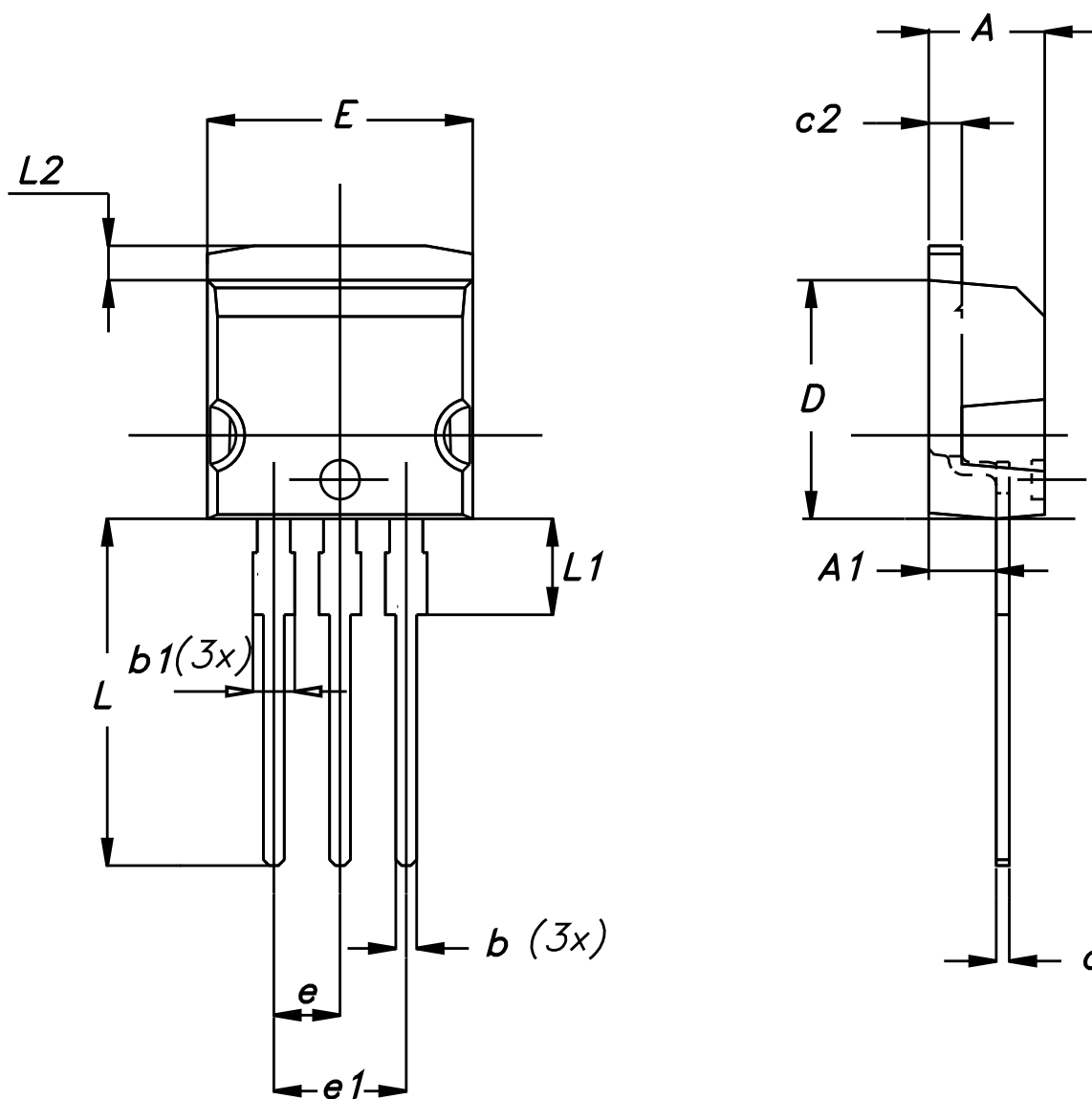


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 21. I²PAK package outline



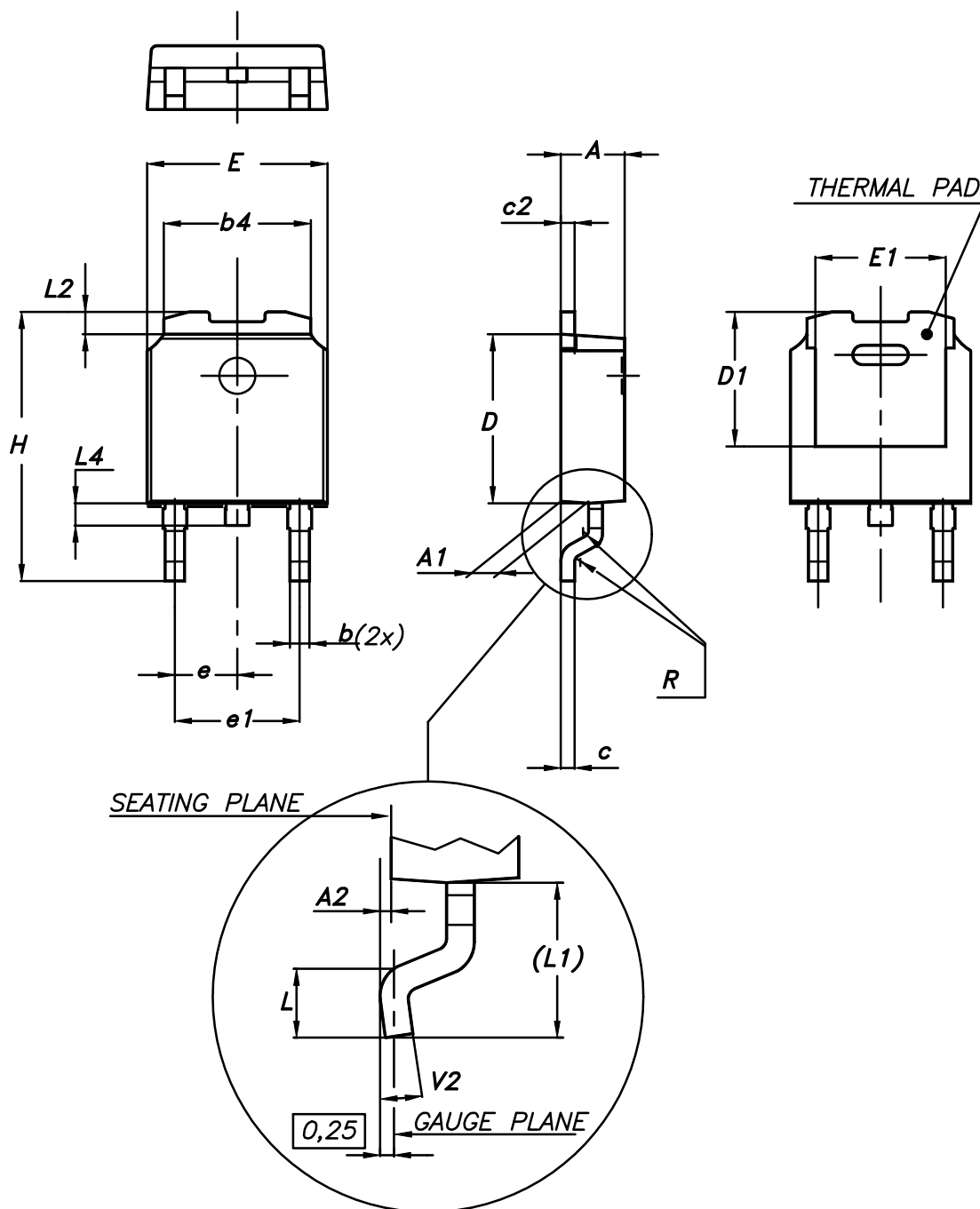
0004982_Rev_H

Table 9. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.2 DPAK (TO-252) type A package information

Figure 22. DPAK (TO-252) type A package outline



0068772_A_25

Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.3 DPAK (TO-252) type E package information

Figure 23. DPAK (TO-252) type E package outline

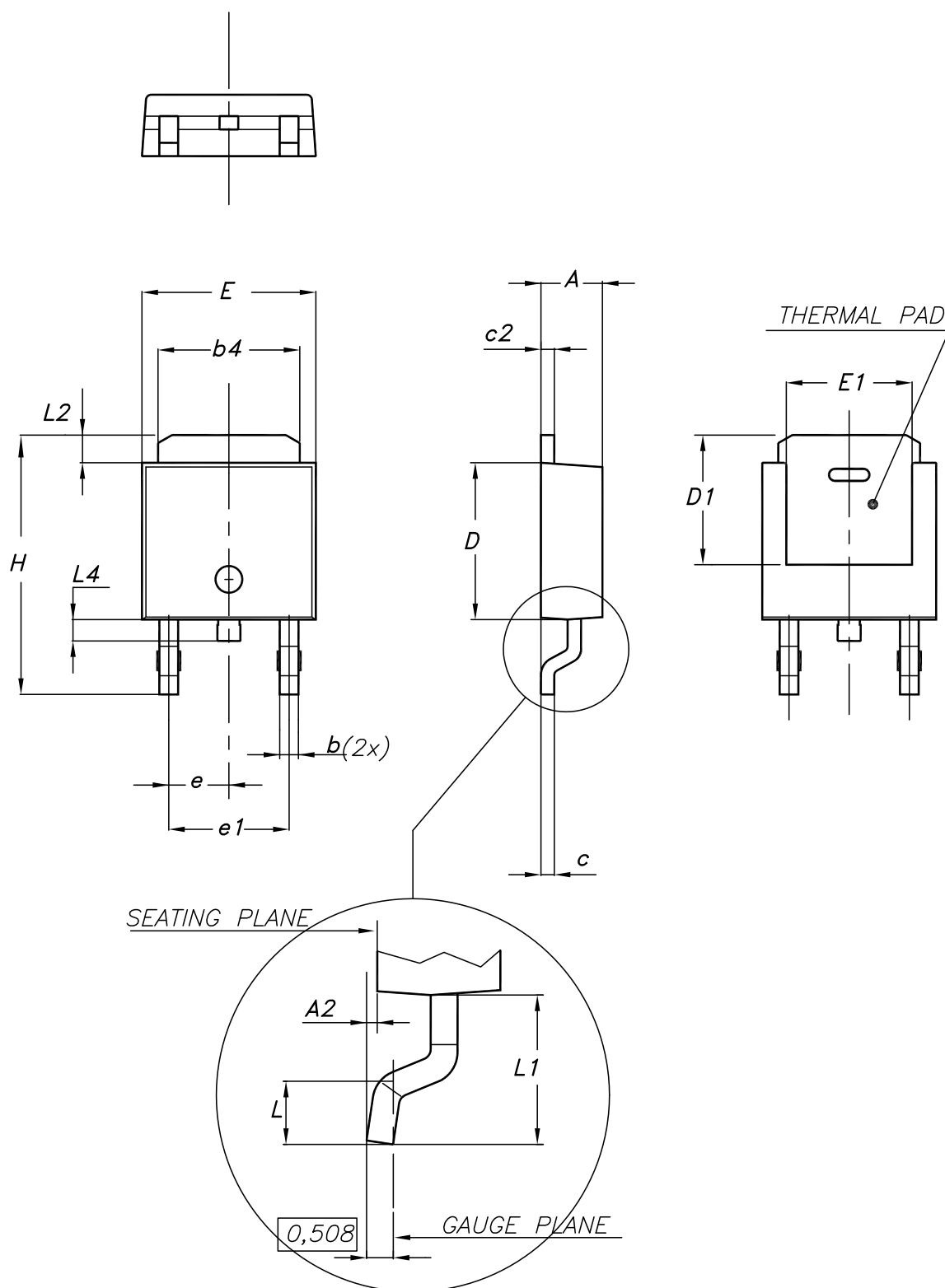
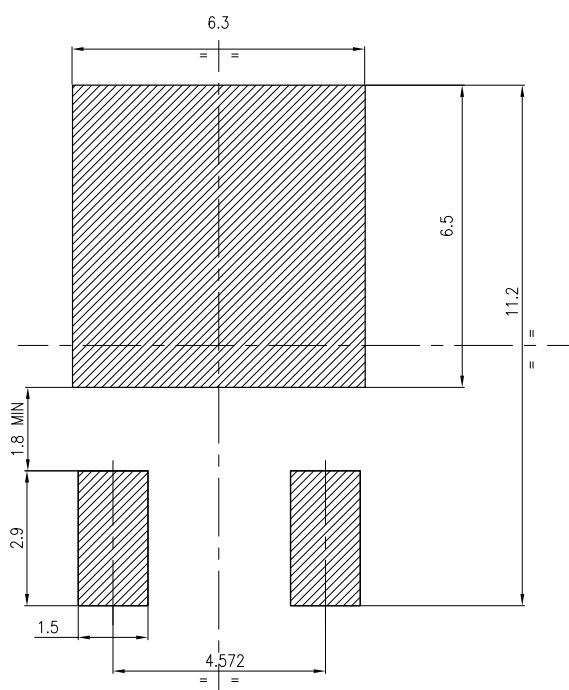


Table 11. DPAK (TO-252) type E mechanical data

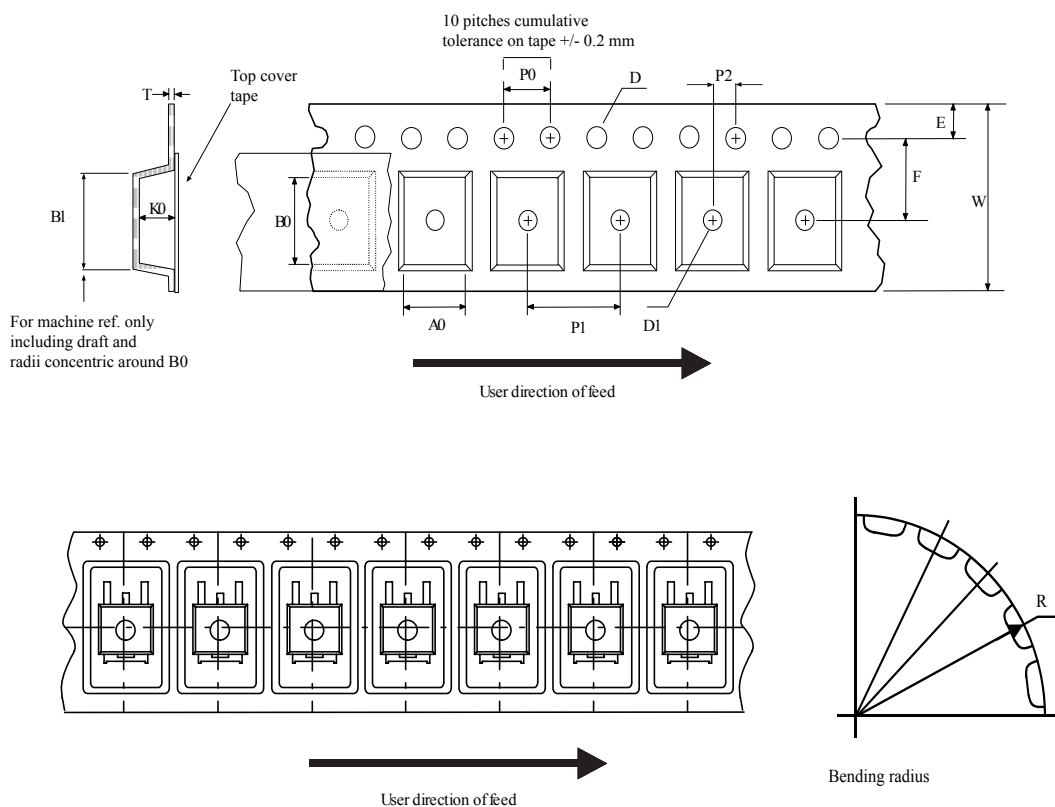
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)


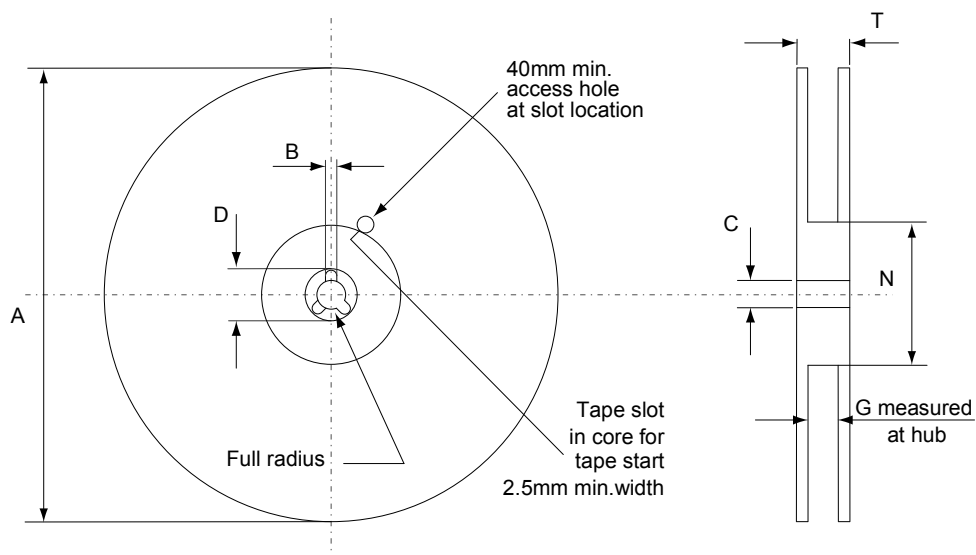
FP_0068772_25

4.4 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline



AM08852v1

Figure 26. DPAK (TO-252) reel outline


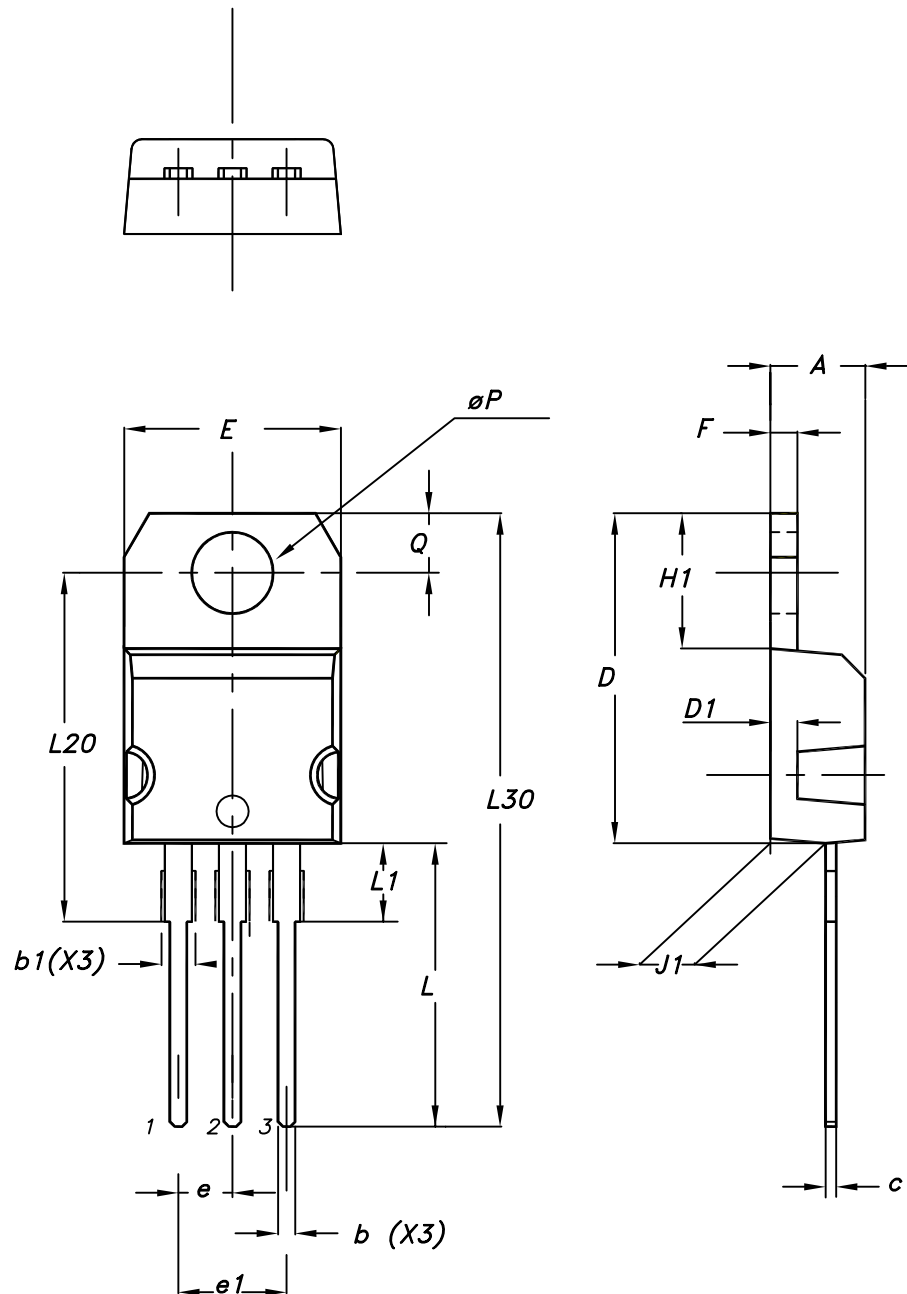
AM06038v1

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.5 TO-220 type A package information

Figure 27. TO-220 type A package outline



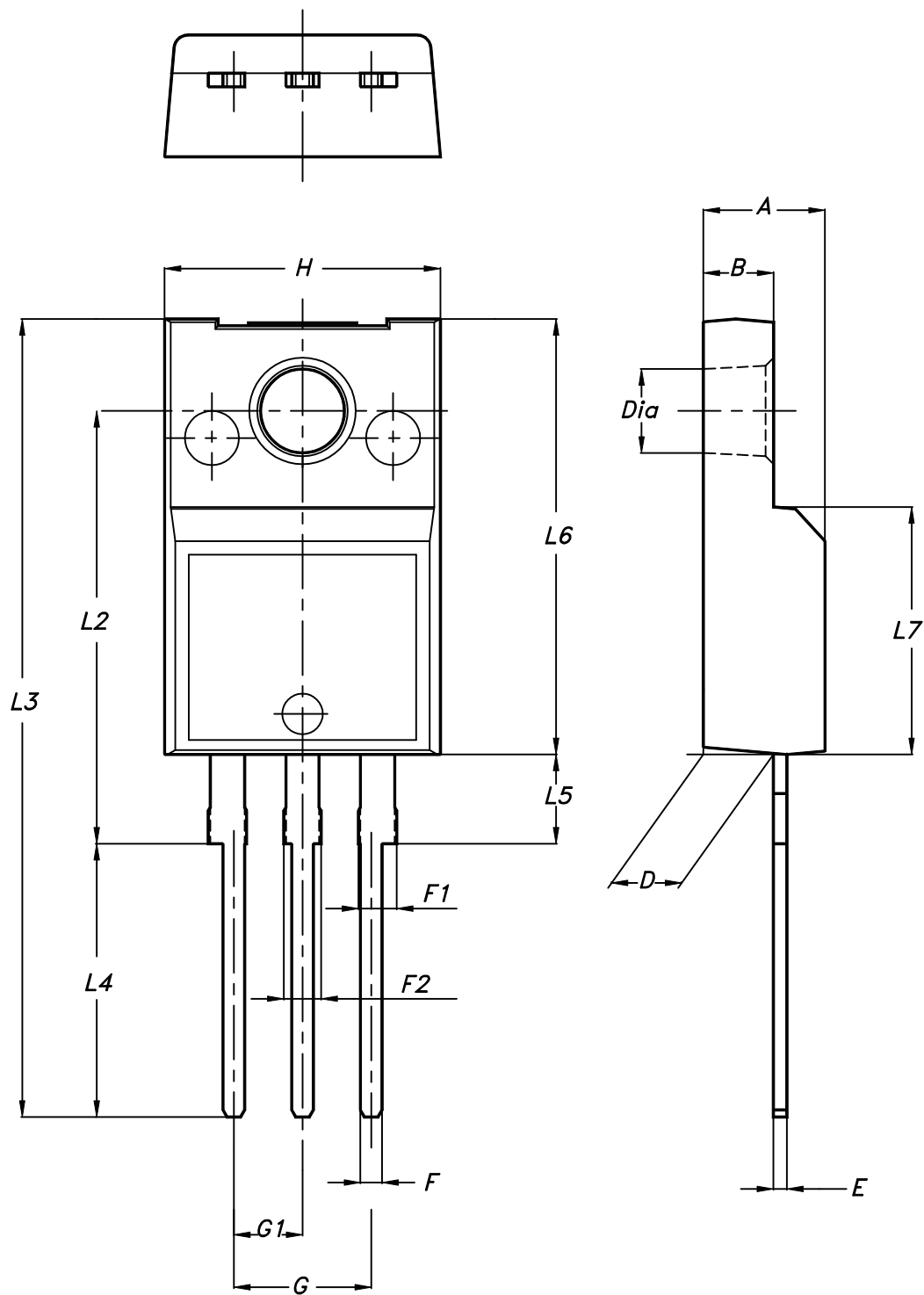
0015988_typeA_Rev_21

Table 13. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 TO-220FP package information

Figure 28. TO-220FP package outline



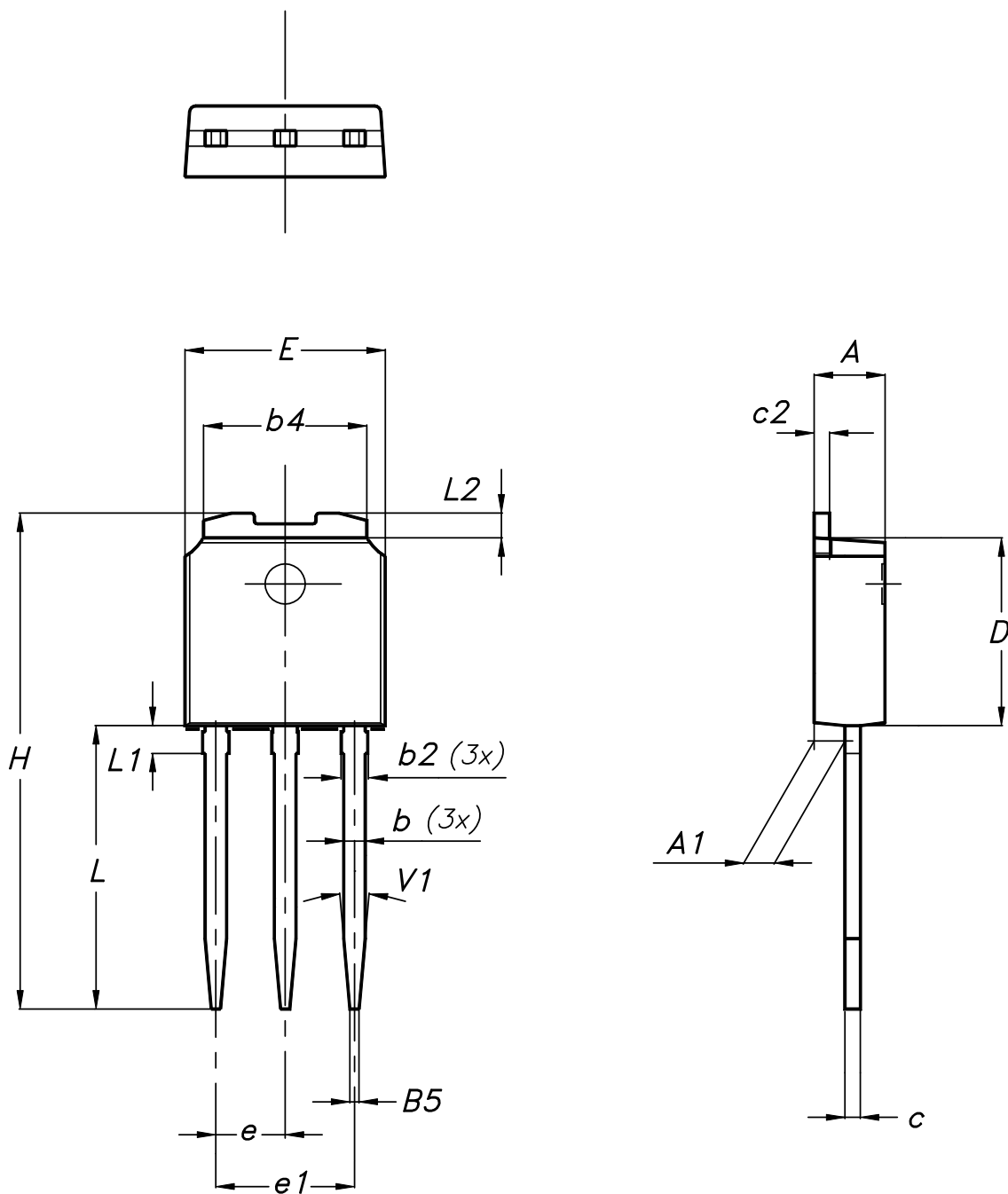
7012510_Rev_12_B

Table 14. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.7 IPAK (TO-251) type A package information

Figure 29. IPAK (TO-251) type A package outline



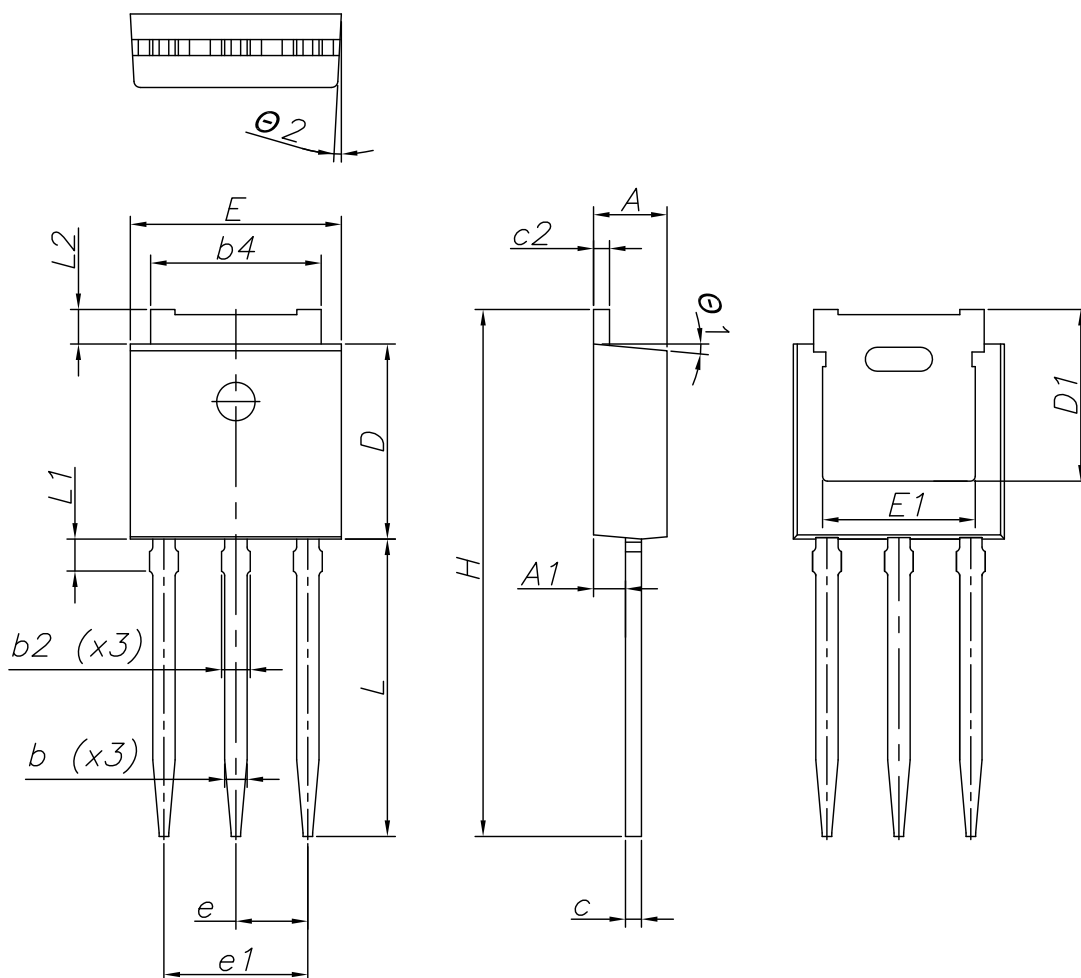
0068771_IK_typeA_rev14

Table 15. IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.8 IPAK (TO-251) type C package information

Figure 30. IPAK (TO-251) type C package outline



0068771_IK_typeC_rev14

Table 16. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Ordering information

Table 17. Order codes

Order code	Marking	Package	Packing
STB5NK50Z-1	B5NK50Z	I ² PAK	Tube
STD5NK50ZT4	D5NK50Z	DPAK	Tape and reel
STP5NK50Z	P5NK50Z	TO-220	Tube
STP5NK50ZFP	P5NK50ZFP	TO-220FP	Tube
STU5NK50Z	5NK50Z	IPAK	Tube

Revision history

Table 18. Document revision history

Date	Version	Changes
16-Jun-2004	4	D ² PAK Included. New Stylesheet.
06-Sep-2005	5	Inserted Ecopack indication
18-Sep-2018	6	The part number STB5NK50Z has been moved to a separate datasheet. Added part number STU5NK50Z. Updated Section 4 Package information .

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics curves	5
3	Test circuits	8
4	Package information.....	9
4.1	I ² PAK package information.	9
4.2	DPAK (TO-252) type A package information	11
4.3	DPAK (TO-252) type E package information	13
4.4	DPAK (TO-252) packing information.....	15
4.5	TO-220 type A package information	17
4.6	TO-220FP package information	19
4.7	IPAK (TO-251) type A package information	21
4.8	IPAK (TO-251) type C package information.....	23
5	Ordering information	26
	Revision history	27



IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved