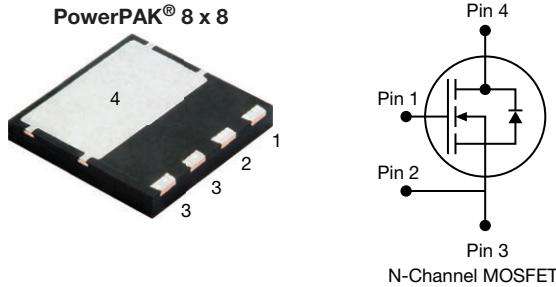


## E Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	650
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V 0.123
$Q_g$ max. (nC)	120
$Q_{gs}$ (nC)	16
$Q_{gd}$ (nC)	33
Configuration	Single



### FEATURES

- Completely lead (Pb)-free device
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### ORDERING INFORMATION

Package	PowerPAK 8 x 8
Lead (Pb)-free and Halogen-free	SiHH26N60EF-T1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	24	A
		15	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	67	
Linear Derating Factor		1.6	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	353	mJ
Maximum Power Dissipation	$P_D$	202	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C	70	V/ns
Reverse Diode dV/dt <sup>c</sup>			
		14	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$  Ω,  $I_{AS} = 5$  A.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/μs, starting  $T_J = 25$  °C.

**THERMAL RESISTANCE RATINGS**

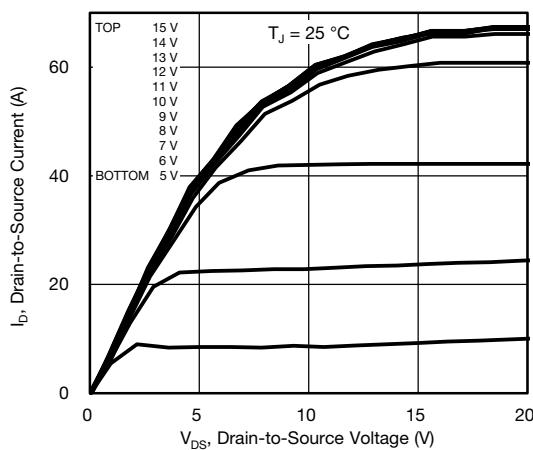
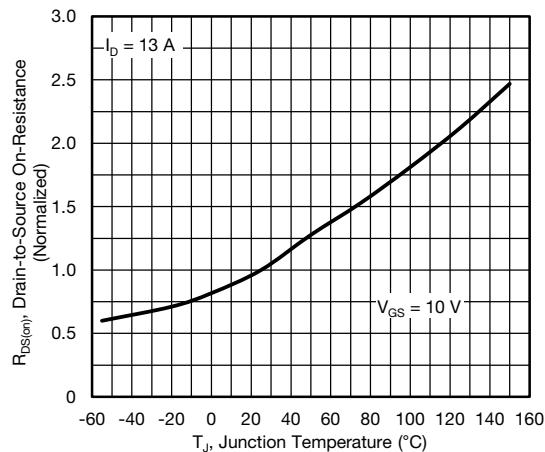
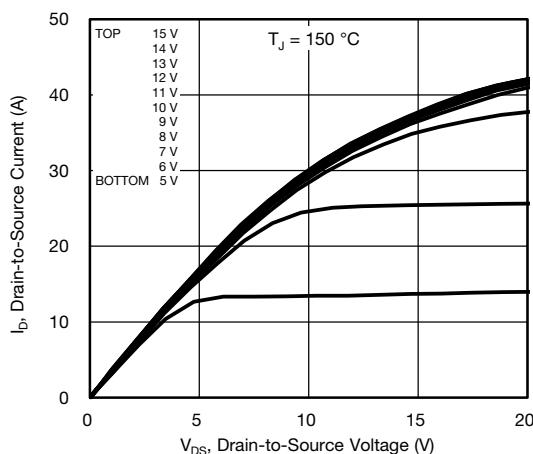
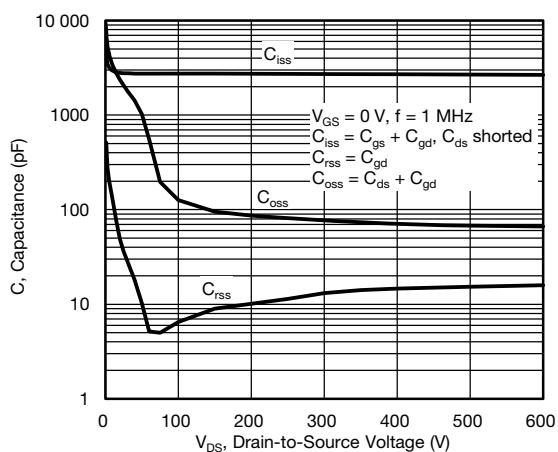
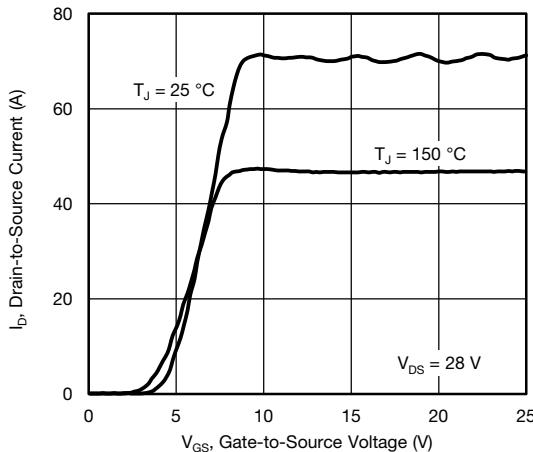
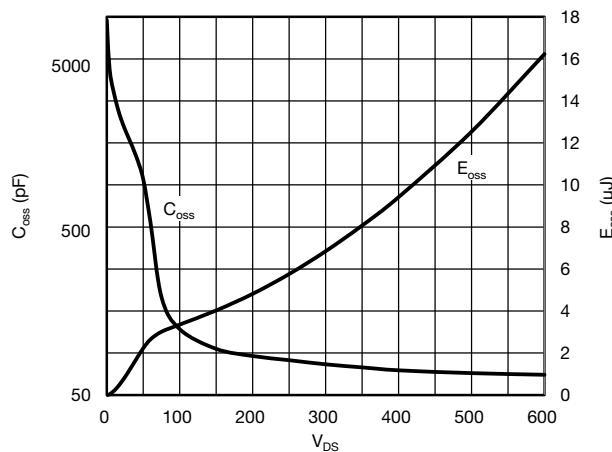
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	38	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.48	0.62	°C/W

**SPECIFICATIONS** ( $T_J = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 10$ mA		-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20$ V		-	-	± 100	nA
		$V_{GS} = \pm 30$ V		-	-	± 1	$\mu$ A
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 480$ V, $V_{GS} = 0$ V		-	-	1	
		$V_{DS} = 480$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	500	$\mu$ A
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 13$ A	-	0.123	0.141	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30$ V, $I_D = 13$ A		-	9.5	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0$ V, $V_{DS} = 100$ V, $f = 1$ MHz		-	2744	-	pF
Output Capacitance	$C_{oss}$			-	126	-	
Reverse Transfer Capacitance	$C_{rss}$			-	7	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0$ V to 480 V, $V_{GS} = 0$ V		-	82	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	357	-	
Total Gate Charge	$Q_g$			-	80	120	nC
Gate-Source Charge	$Q_{gs}$	$V_{GS} = 10$ V	$I_D = 13$ A, $V_{DS} = 480$ V	-	16	-	
Gate-Drain Charge	$Q_{gd}$			-	33	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480$ V, $I_D = 13$ A, $V_{GS} = 10$ V, $R_g = 9.1$ $\Omega$		-	25	50	ns
Rise Time	$t_r$			-	46	92	
Turn-Off Delay Time	$t_{d(off)}$			-	93	140	
Fall Time	$t_f$			-	56	84	
Gate Input Resistance	$R_g$	$f = 1$ MHz, open drain		0.3	0.6	1.2	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	24	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	67	
Diode Forward Voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 13$ A, $V_{GS} = 0$ V		-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25$ °C, $I_F = I_S = 13$ A, $dl/dt = 100$ A/ $\mu$ s, $V_R = 25$ V		-	146	292	ns
Reverse Recovery Charge	$Q_{rr}$			-	0.9	1.8	$\mu$ C
Reverse Recovery Current	$I_{RRM}$			-	12	-	A

**Notes**

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .  
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

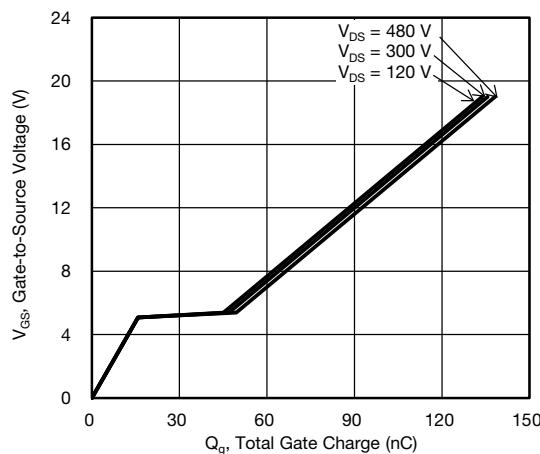


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

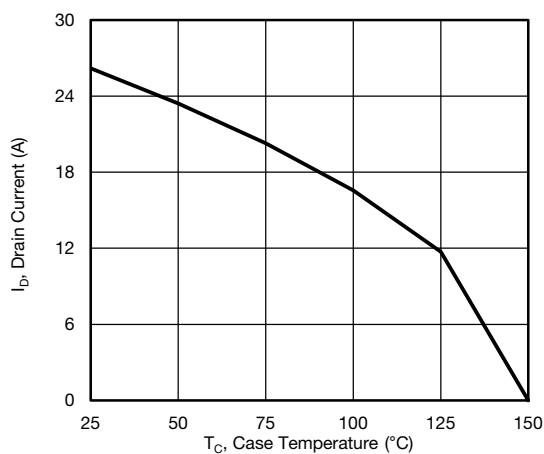


Fig. 10 - Maximum Drain Current vs. Case Temperature

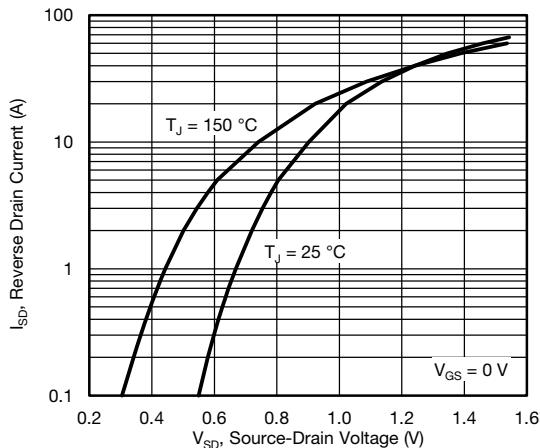


Fig. 8 - Typical Source-Drain Diode Forward Voltage

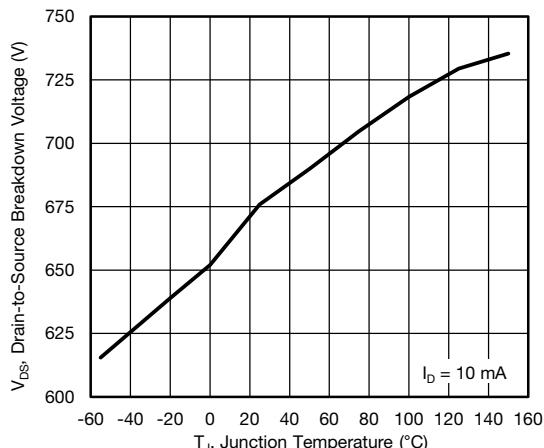


Fig. 11 - Temperature vs. Drain-to-Source Voltage

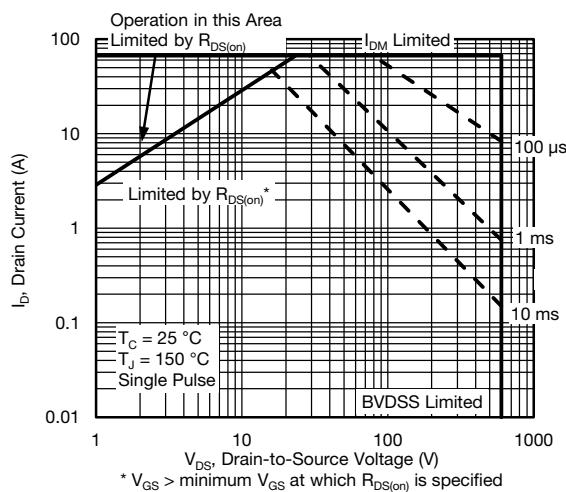
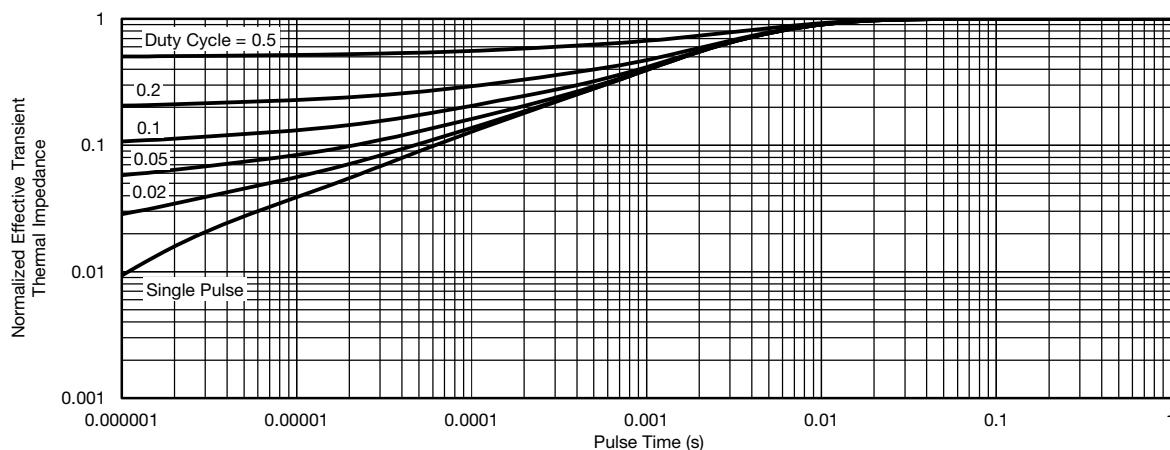
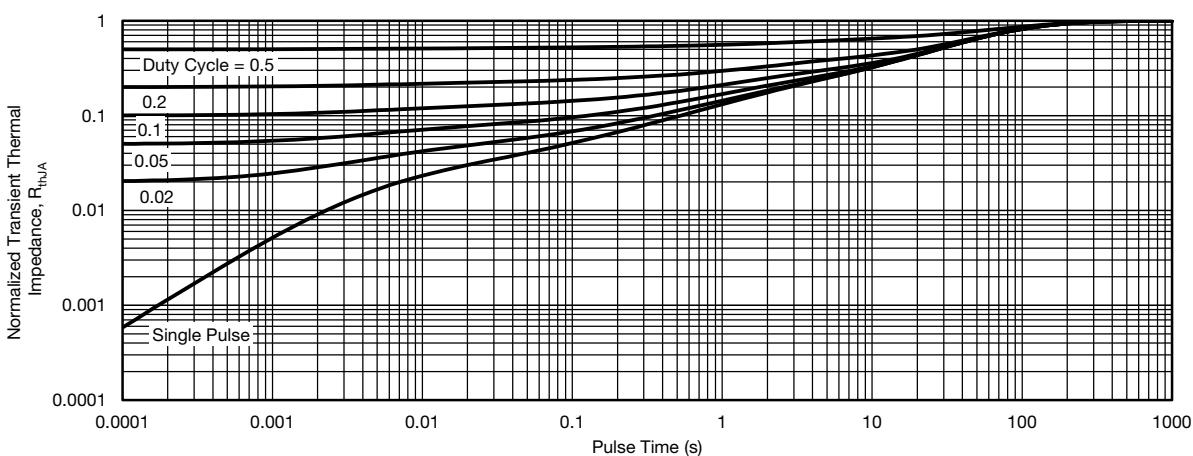


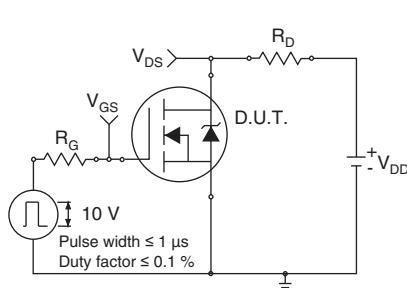
Fig. 9 - Maximum Safe Operating Area



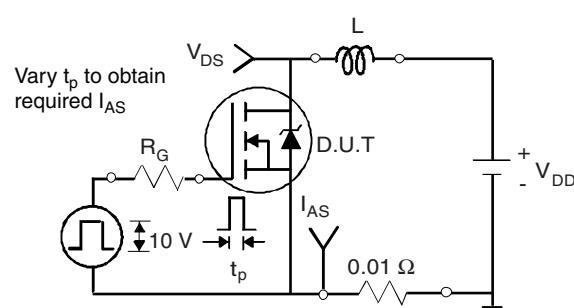
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



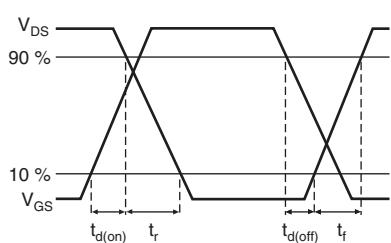
**Fig. 13 - Normalized Thermal Transient Impedance, Junction-to-Ambient**



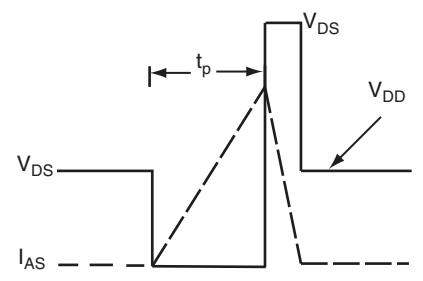
**Fig. 14 - Switching Time Test Circuit**



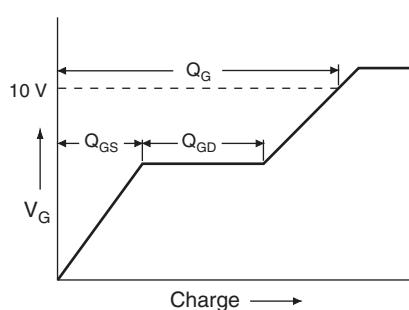
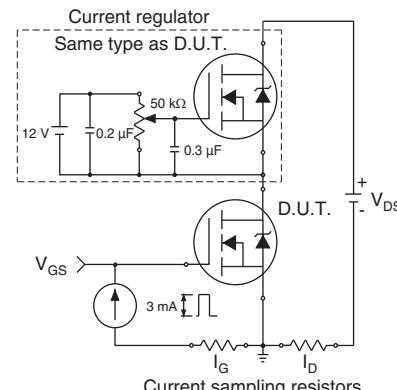
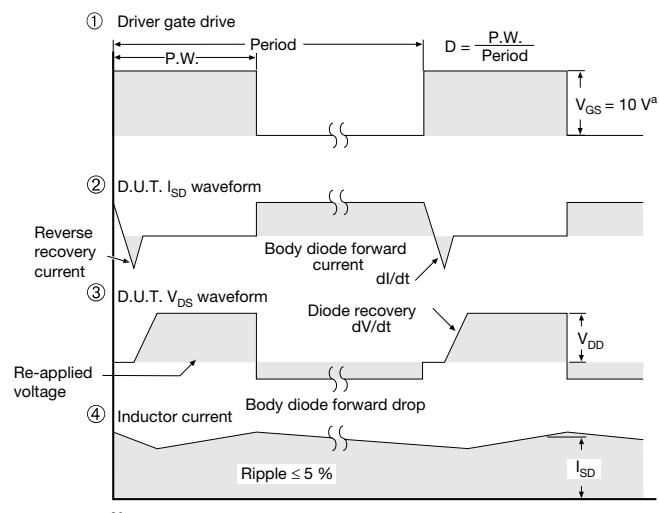
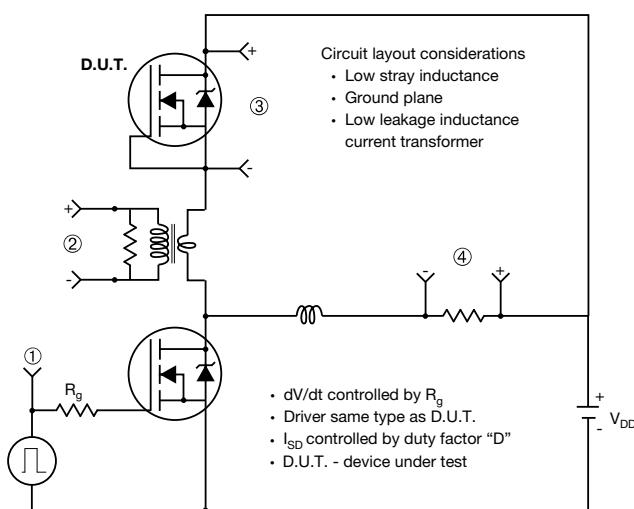
**Fig. 16 - Unclamped Inductive Test Circuit**



**Fig. 15 - Switching Time Waveforms**



**Fig. 17 - Unclamped Inductive Waveforms**

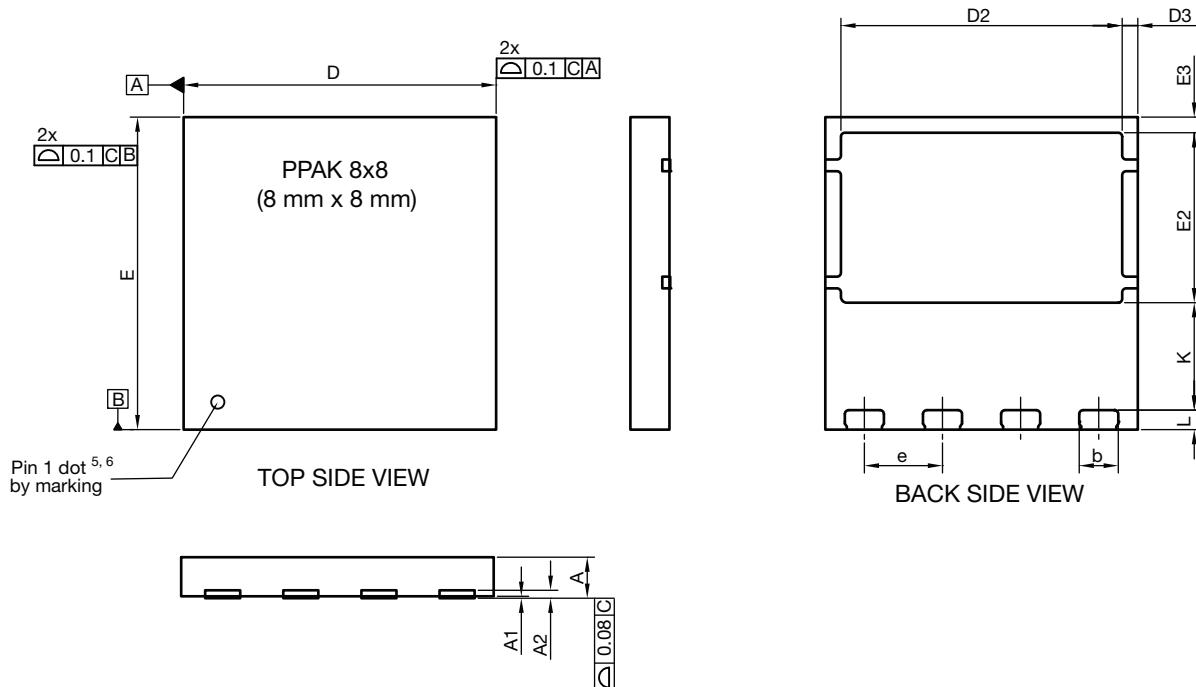

**Fig. 18 - Basic Gate Charge Waveform**

**Fig. 19 - Gate Charge Test Circuit**
**Peak Diode Recovery dV/dt Test Circuit**


Note  
a.  $V_{GS} = 5$  V for logic level devices

**Fig. 20 - For N-Channel**

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## PowerPAK® 8 x 8 Case Outline

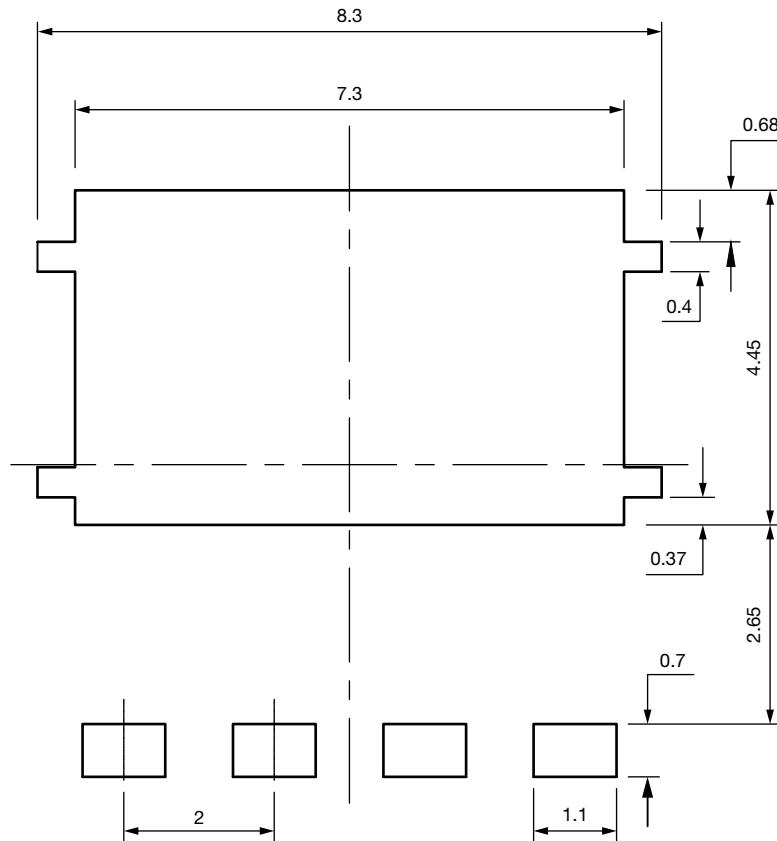


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A <sup>8</sup>	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b <sup>4</sup>	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N <sup>3</sup>	8			8		

**Notes**

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5 M - 1994.
3. N is the number of terminals.
4. Package warpage max. 0.08 mm.
5. The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.

ECN: T15-0225-Rev. A, 18-May-15  
 DWG: 6041

**Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm**

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