SPECTRUM DIGITAL INCORPORATED

eZdsp™ F2804x

Technical Reference

2006 ***DSP Development Systems***

eZdsp™ F2804x
Technical Reference

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About This Manual

This document describes board level operations of the eZdsp™ F2804x based on the Texas Instruments TMS320F2804x Digital Signal Processor.

The eZdsp™ F2804x is a stand-alone module permitting engineers and software developers evaluation of certain characteristics of the TMS320F2804x DSP to determine processor applicability to design requirements. Evaluators can create software to execute onboard or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The “eZdsp™ F2804x” will sometimes be referred to as the “eZdsp”.

“eZdsp” will include the socketed or unsocketed version

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320F28x DSP CPU and Instruction Set Reference Guide, literature #SPRU430
Texas Instruments TMS320F28x Assembly Language Tools Users Guide, literature #SPRU513
Texas Instruments TMS320F28x Optimizing C/C++ Compiler User’s Guide, literature #SPRU514
Texas Instruments Code Composer Studio Getting Started Guide, literature #SPRU509

Table 1: Manual History

Revision	History
A	Preliminary Release

Table 2: Board History

Revision	History
A	Prototype Release

Chapter 1

Introduction to the eZdsp™ F2804x

This chapter provides a description of the eZdsp™ for the TMS320F2804x Digital Signal Processor, key features, and block diagram of the circuit board.

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1.0 Overview of the eZdsp™ F2804x

The eZdsp™ F2804x is a stand-alone card--allowing evaluators to examine the TMS320F2804x digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F2804x processor.

The eZdsp™ F2804x is shipped with a TMS320F2804x DSP. The eZdsp™ F2804x allows full speed verification of F2804x code. Expansion connectors are provided for any necessary evaluation circuitry not provided on the as shipped configuration.

To simplify code development and shorten debugging time, a C2000 Tools Code Composer driver is provided. In addition, an onboard JTAG connector provides interface to emulators, operating with other debuggers to provide assembly language and ‘C’ high level language debug.

1.1 Key Features of the eZdsp™ F2804x

The eZdsp™ F2804x has the following features:

- TMS320F2804x Digital Signal Processor
- 100 MIPS operating speed
- 10K words on-chip zero wait state SARAM
- 128K words on-chip Flash memory
- 256K bits serial I^2C EEPROM memory
- 20 MHz. clock
- Expansion Connectors (analog, I/O)
- Onboard IEEE 1149.1 JTAG Controller
- 5-volt only operation with supplied AC adapter
- TI F28xx Code Composer Studio tools driver
- On board USB JTAG emulation connector
- 1 SCI UART channel

1.2 Functional Overview of the eZdsp™ F2804x

Figure 1-1 shows a block diagram of the basic configuration for the eZdsp™ F2804x. The major interfaces of the eZdsp are the JTAG interface, and expansion interface.

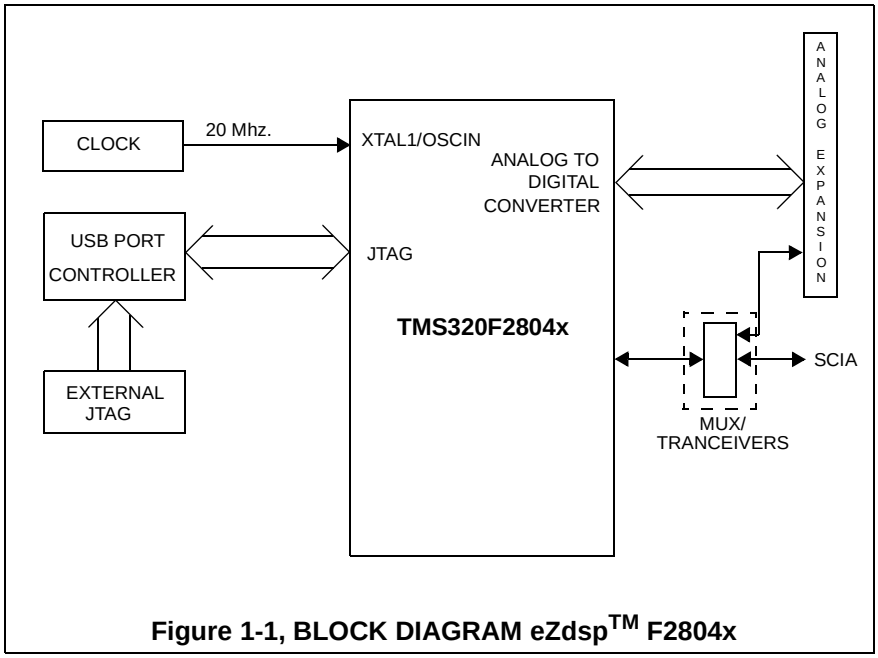

Figure 1-1, BLOCK DIAGRAM eZdsp™ F2804x

Chapter 2

Operation of the eZdsp™ F2804x

This chapter describes the operation of the eZdsp™ F2804x, key interfaces and includes a circuit board outline.

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2.0 The eZdsp™ F2804x Operation

This chapter describes the eZdsp™ F2804x, key components, and operation. Information on the eZdsp's various interfaces is also included. The eZdsp™ F2804x consists of four major blocks of logic:

- Analog Interface Connector
- I/O Interface Connector
- JTAG Interface
- USB Port JTAG Controller Interface

2.1 The eZdsp™ F2804x Board

The eZdsp™ F2804x is a 5.25 x 3.0 inch, multi-layered printed circuit board, powered by an external 5-Volt only power supply. Figure 2-1 shows the layout of the top side of the eZdsp™ F2804x.

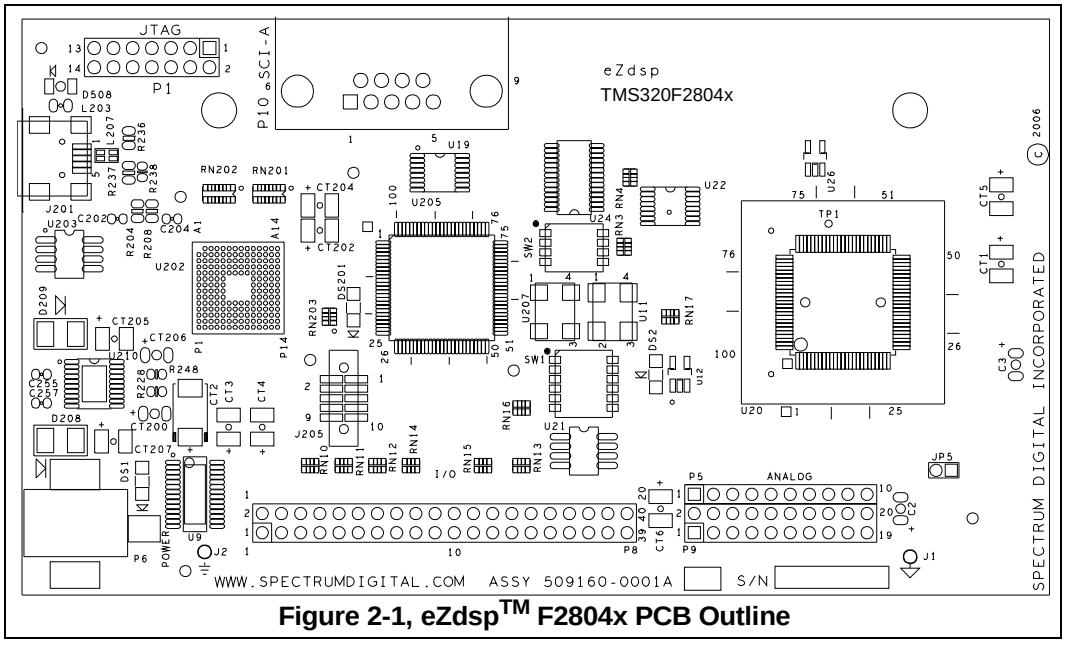


Figure 2-1, eZdsp™ F2804x PCB Outline

2.1.1 Power Connector

The eZdsp™ F2804x is powered by a 5-Volt only power supply, included with the unit. The unit requires 500mA. The power is supplied via connector P6. If expansion boards are connected to the eZdsp, a higher amperage power supply may be necessary. Section 2.3.6 provides more information on connector P6.

2.2 eZdsp™ F2804x Memory

The eZdsp includes the following on-chip memory:

- 2 blocks of 1K x 16 single access RAM (SARAM, M0,M1)
- 1 block of 8K x 16 SARAM (Lo,L1)

The eZdsp can load ram for debug, or Flash can be programmed and run. For larger software projects it is suggested to do a initial debug with on eZdsp F2804x module which supports a total RAM environment. With careful attention to the I/O mapping in the software the application code can easily be ported to the F2804x.

2.2.1 Memory Map

The figure below shows the memory map configuration on the eZdsp™ F2804x.

Block Start Address	F2804x	
	Data Space	Program Space
0x0000-0000	M0 SARAM	
0x0000-0400	M1 SARAM	
0x0000-0800	Peripheral Frame 0	Do Not Use !
0x0000-0D00	Pie Vector Table (256 x 16)	
0x0000-0E00		
0x0000-6000	Peripheral Frame 1	Do Not Use !
0x0000-7000	Peripheral Frame 2 (16 Bit access only)	
0x0000-8000	L0 SARAM	
0x0000-9000	L1 SARAM	
0x0000-A000		
0x003D-7800	OTP (Read Only)	
0x003D-7C00		
0x003D-8000	Flash (Read Only) (128K x 16)	
0x003F-8000	L0 SARAM Mirror	
0x003F-9000	L1 SARAM Mirror	
0x003F-A000		
0x003F-F000 0x003F-FFFF	Boot ROM (Read Only)	

Figure 2-2, eZdsp™ F2804x Memory Space

2.3 eZdsp™ F2804x Connectors

The eZdsp™ F2804x has five connectors. Pin 1 of each connector is identified by a square solder pad. The function of each connector is shown in the table below:

Table 1: eZdsp™ F2804x Connectors

Connector	Function
P1	JTAG Interface
P8	I/O Interface
P5/P9	Analog Interface
P6	Power Connector
P10	DB-9, RS-232
J201	USB Controller Interface

The diagram below shows the position of each connector

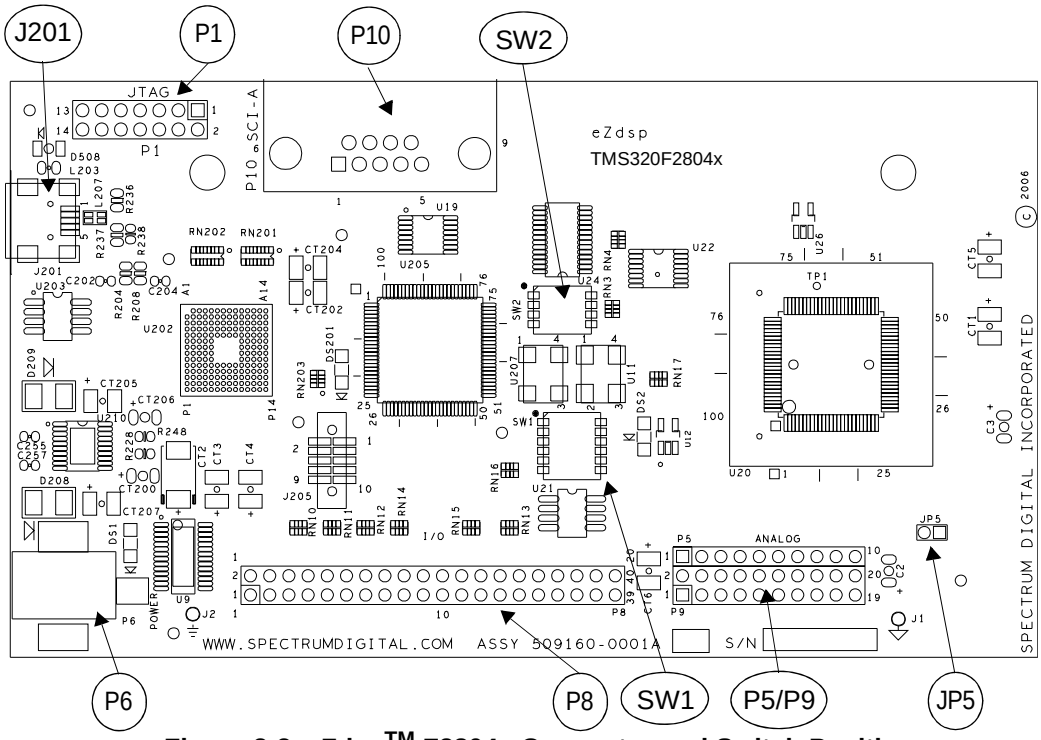


Figure 2-3, eZdsp^{TM} F2804x Connector and Switch Positions

2.3.1 P1, JTAG Interface

The eZdsp^{TM} F2804x is supplied with a 14-pin header interface, P1. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs.

The positions of the 14 pins on the P1 connector are shown in the diagram below as viewed from the top of the eZdsp.

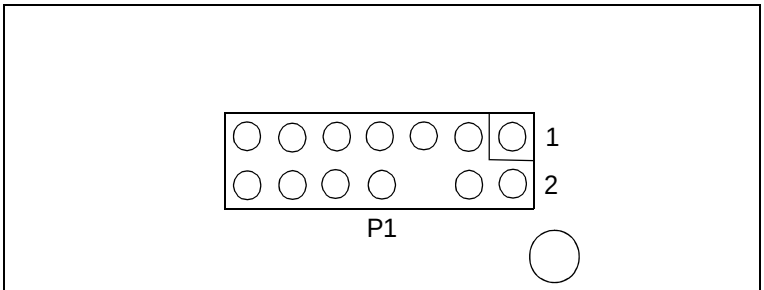


Fig 2-4, P1 Pin Locations

The definition of P1, which has the JTAG signals is shown below.

Table 2: P1, JTAG Interface Connector

Pin #	Signal	Pin #	Signal
1	TMS	2	TRST-
3	TDI	4	GND
5	PD (+5V)	6	**no pin**
7	TDO	8	GND
9	TCK-RET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

2.3.2 J201, USB Port/JTAG Interface

The eZdsp™ F2804x uses a custom USB port JTAG interface device. The device has direct access to the integrated JTAG interface. Drivers for C2000 Code Composer tools are shipped with the eZdsp™ modules

2.3.3 P8, I/O Interface

The connector P8 presents the I/O signals from the DSP. The layout of this connector is shown below.

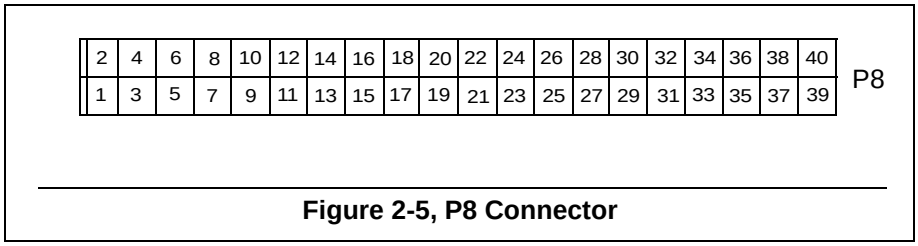


Figure 2-5, P8 Connector

The pin definition of P4/P8 connectors are shown in the table below.

Table 3: P4/P8, I/O Connectors

P8 Pin #	P8 Signal	P8 Pin #	P8 Signal
1	+3.3V/+5V/NC *	2	+3.3V/+5V/NC *
3	MUX_GPIO29	4	MUX_GPIO28
5	GPIO14	6	GPIO20
7	GPIO21	8	GPIO23
9	GPIO0	10	GPIO1
11	GPIO2	12	GPIO3
13	GPIO4	14	GPIO5
15	GPIO27	16	GPIO6
17	GPIO13	18	GPIO34
19	GND	20	GND
21	GPIO7	22	GPIO15
23	GPIO16	24	GPIO17
25	GPIO18	26	GPIO19
27	MUX_GPIO31	28	MUX_GPIO30
29	MUX_GPIO11	30	MUX_GPIO8
31	MUX_GPIO9	32	MUX_GPIO10
33	GPIO22/GPIO24	34	GPIO25
35	GPIO26	36	GPIO32
37	GPIO12	38	GPIO33
39	GND	40	GND

* Default is No Connect (NC). User can jumper to +3.3V or +5V on backside of eZdsp with JP4.

2.3.4 P5/P9, Analog Interface

The position of the 30 pins on the P5/P9 connectors are shown in the diagram below as viewed from the top of the eZdsp.

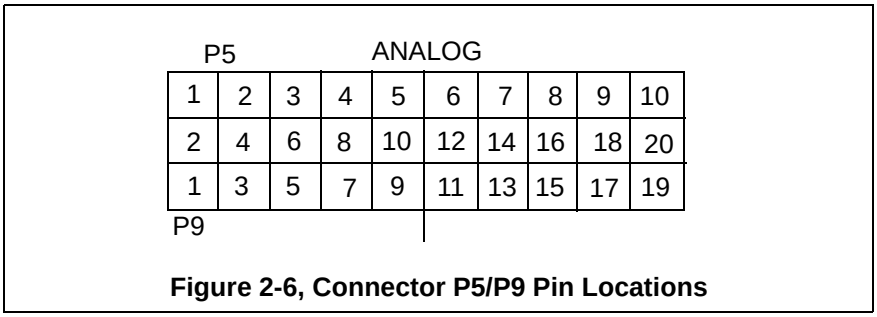


Figure 2-6, Connector P5/P9 Pin Locations

The definition of P5/P9 signals are shown in the table below.

Table 4: P5/P9, Analog Interface Connector

P5 Pin #	Signal	P9 Pin #	Signal	P9 Pin #	Signal
1	ADCINB0	1	GND	2	ADCINA0
2	ADCINB1	3	GND	4	ADCINA1
3	ADCINB2	5	GND	6	ADCINA2
4	ADCINB3	7	GND	8	ADCINA3
5	ADCINB4	9	GND	10	ADCINA4
6	ADCINB5	11	GND	12	ADCINA5
7	ADCINB6	13	GND	14	ADCINA6
8	ADCINB7	15	GND	16	ADCINA7
9	ADCREFM	17	GND	18	VREFLO *
10	ADCREFP	19	GND	20	No connect

* Connect VREFLO to AGND or VREFLO of target system for proper ADC operation.

2.3.5 P6, Power Connector

Power (5 volts) is brought onto the eZdsp^{TM} F2804x via the P6 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The position of the P6 connector is shown below.

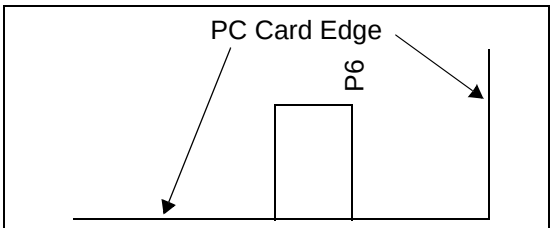


Figure 2-7, Connector P6 Location

The diagram of P6, which has the input power is shown below.

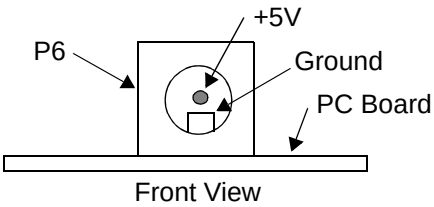


Figure 2-8, eZdsp^{TM} F2804x Power Connector

2.3.6 P10, RS-232 Connector

The eZdsp F2804x has an RS-232 connector which brings out the SCIA transmit and receive signals to be used as UART. This UART uses the MAX3238 RS-232 line driver and is routed to a male 9 pin D-connector, P10. The pin positions for the P10 connector as viewed from the edge of the printed circuit board are shown below.

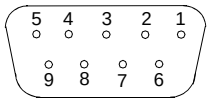


Figure 2-9, P10, DB9 Female Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 5: P10, RS-232 Pinout

Pin #	Signal Name	Direction
1	No Connect	
2	PCRXDA	Out
3	PCTXDA	In
4	No Connect	
5	GND	N/A
6	No Connect	
7	No Connect	
8	No Connect	
9	No Connect	

2.3.7 Connector Part Numbers

The table below shows the part numbers for connectors which can be used on the eZdsp™ F2804x. Part numbers from other manufacturers may also be used.

Table 6: eZdsp™ F2804x Suggested Connector Part Numbers

Connector	Male Part Numbers	Female Part Numbers
P1	SAMTEC TSW-1-10-07-G-T	SAMTEC SSW-1-10-01-G-T
P2	SAMTEC TSW-1-20-07-G-T	SAMTEC SSW-1-20-01-G-T

*SSW or SSQ Series can be used

2.4 eZdsp™ F2804x Jumpers

The eZdsp™ F2804x has 3 jumpers, JP4, JP5, and JP6. JP4 will allow power to be supplied to the expansion headers. Jumper JP5 selects the ACDREFIN voltage. The JP6 jumper selects which GPIO pin (22 or 24) goes to Pinn33 of P8. The table below lists the jumpers and their function. The following sections describe the use of each jumper.

Table 7: eZdsp™ F2804x Jumpers

Jumper #	Size	Function	Position As Shipped From Factory
JP4	1 x 3	+3.3/5 Volts to P8 Pin 1,2 and P4, Pin 1	Not connected
JP5	1 x 2	Selects ADCREFIN voltage	Not connected
JP6	1 x 3	Selects GPIO22 or GPIO24 to Pin 33, P8	2 - 3, GPIO24 to Pin 33, P8

2.4.1 JP4, Voltage Jumper, +3.3/5 Volts for P8, P4

Jumpers JP4 is an unpopulated jumper on the bottom side of the board that provide either +3.3 volts or +5 volts to pins on the expansion connector. This jumper is shipped uninstalled to prevent accidental damage by connecting wires or circuitry to the expansion connector. The user may connect the jumper by installing a jumper wire or zero ohm resistor. The position of this jumper is shown in the figure below.

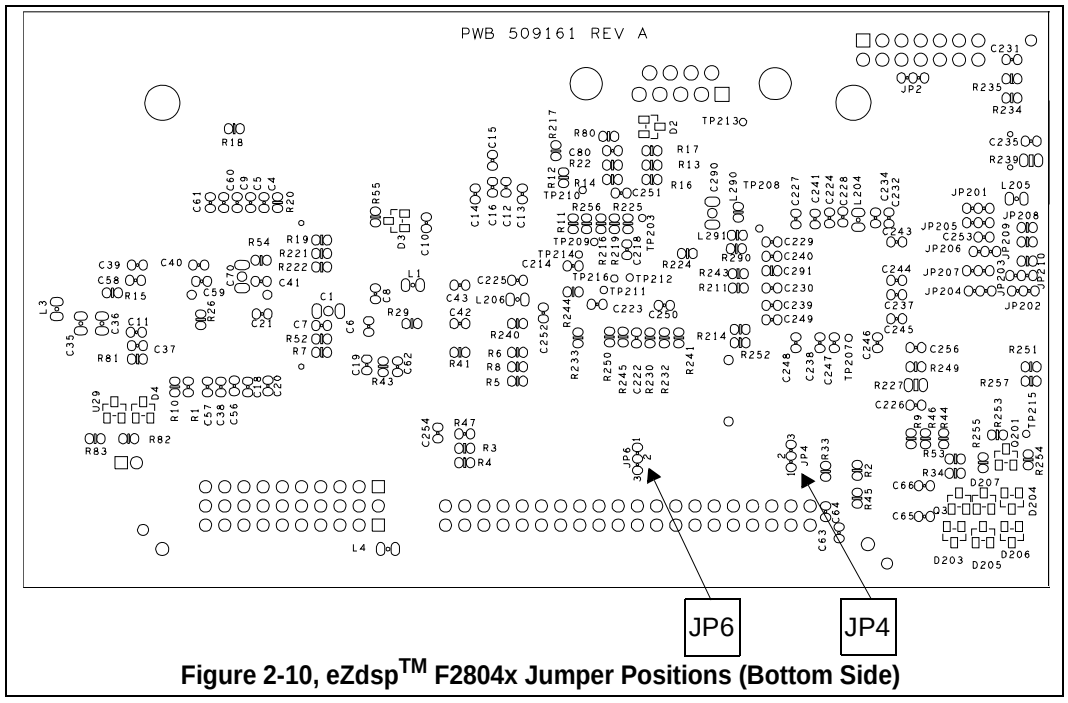


Figure 2-10, eZdsp™ F2804x Jumper Positions (Bottom Side)

Jumper JP4 allows the user to provide either +3.3 or +5 volts to pins 1 and 2 of expansion connector P8.

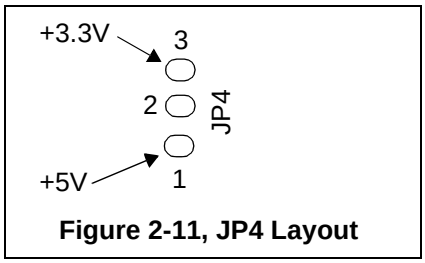


Figure 2-11, JP4 Layout

The table below shows the functions of the two positions of JP4.

Table 8: JP4, Voltage Jumper,+3.3/5 Volts for P8, P4

Position	Function
1 - 2	+5V connected to P8
2 - 3	+3.3 connected to P8

2.4.2 JP5, ADCREFIN Select

Jumper J5 is used to select ADCREFIN as the voltage reference for the analog to digital converter. When the jumper is shorted the +2.048 voltage level is routed to the ADCREFIN signal of the DSP. When the jumper is open the ADCREFIN floats.

2.4.3 JP6, GPIO22/GPIO24 Select

Jumper JP6 selects which signal, GPIO22 or GPIO24, to be routed to Pin 33, P8. When the 1-2 jumper position is selected GPIO22 is connected to pin 33, P8. The 2-3 selection will route GPIOI24 to Pin 33, P8. The figure below shows the connector layout on the bottom side of the board.

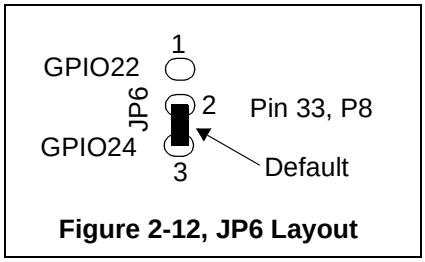


Figure 2-12, JP6 Layout

The table below shows the functions of the two positions of JP6.

Table 9: JP6, GPIO22/GPIO24 Select

Position	Function
1 - 2	GPIO22 connected to Pin 33, P8
2 - 3	GPIO24 connected to Pin 33, P8 *

* default

2.5 Switches

The eZdsp F2804x has 2 switches, SW1 and SW2, which are used to configure various functions on the board. The switches and their functionality are described in the following sections.

2.5.1 Switch SW1

The eZdsp F2804x has a 6 position switch, SW1, that allows the user to configure the board for their application. The function of each position on SW1 is shown in the table below.

Table 10: SW1 Switch Positions

Position	Function
1-3	Boot Mode Select
4	Serial EEPROM WP
5	Serial EEPROM Pullups
6	Serial EEPROM - A1

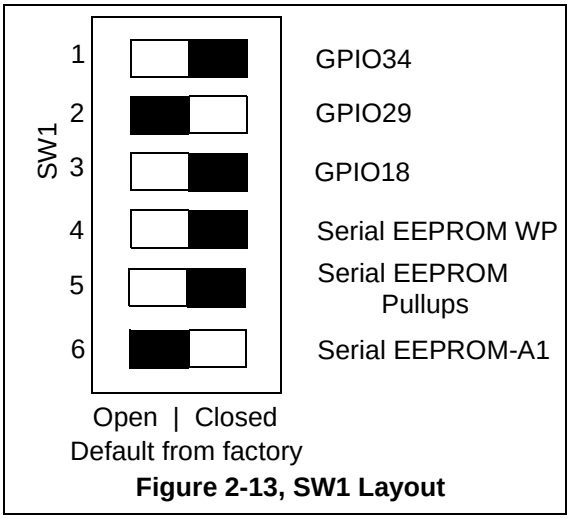


Figure 2-13, SW1 Layout

2.5.1.1 Switch SW1, Positions 1-3, Boot Mode Select

Positions 1-3 on switch SW1 are used to determine what mode the DSP will use for bootloading on power up. The options are shown in the table below.

Table 11: SW1, Positions 1-3

Position 3 GPIO18	Position 2 GPIO29	Position 1 GPIO34	Boot Mode
Open-1	Open-1	Open-1	Flash
Open-1	Open-1	Closed-0	SCI-A
Open-1	Closed-0	Open-1	SPI-A
Open-1	Closed-0	Closed-0	I^2C-A
Closed-0	Open-1	Open-1	Reserved
Closed-0	Open-1	Closed-0	M0 SARAM *
Closed-0	Closed-0	Open-1	OTP
Closed-0	Closed-0	Closed-0	I/O

* factory default

2.5.1.2 Switch SW1, Position 4, EEPROM Write Enable/Disable

Position 4 on switch SW1 is used to enable or disable the Write Enable for the EEPROM. When position 4 is in the “Closed” state the Write Protect to the EEPROM is disabled, therefore allowing the EEPROM to be written. When position 4 is in the “Open” state the EEPROM Write Protect is enabled, not allowing the EEPROM to be written. These positions are shown in the table below.

Table 12: SW1, Position 4

Position	Function
Closed-0 *****	EEPROM WP Disabled (EEPROM can be written to) *****
Open-1	EEPROM WP Enabled (EEPROM cannot be written to)

* factory default

2.5.1.3 Switch SW1, Position 5, Serial EEPROM Pull-ups

Position 5 on switch SW1 are used to select if the EEPROM is using pull up resistors. When position 5 is in the “Closed” state pull up resistors are used. When position 5 is in the “Open” state the pull-up resistors are not used. These positions are shown in the table below.

Table 13: SW1, Position 5

Position	Function
Closed-1 *	Pull up resistors used *
Open-0	Pull up resistors not used

* factory default

2.5.1.4 Switch SW1, Position 6, Serial EEPROM Address A1

Position 6 on switch SW1 are used to select if the address line A1 to the serial EEPROM is pulled high or low. When position 6 is in the “Closed” state A1 equals 1. When position 6 is in the “Open” state A1 equals 0. These positions are shown in the table below.

Table 14: SW1, Position 6

Position	Function
Closed-1	A1 = 1
Open-0	A1 = 0 *

* factory default

2.5.2 Switch SW2

Switch SW2 on the eZdsp F2804x has 4 positions that allow the user to configure the SCI MUX. The function of each position is shown in the table below.

Table 15: SW2 Switch Positions

Position	Function	Settings
1	SCIA/GPIO MUX Control	Open/High GPIO28, GPIO29 to expansion connector P8 Closed/Low GPIO28, GPIO29 to SCIA/CANA transceivers
2	SCIA/GPIO MUX Enable	Open/High GPIO28, GPIO29 isolated Closed/Low GPIO28, GPIO29 not isolated

The layout of switch SW2 is shown in the figure below.

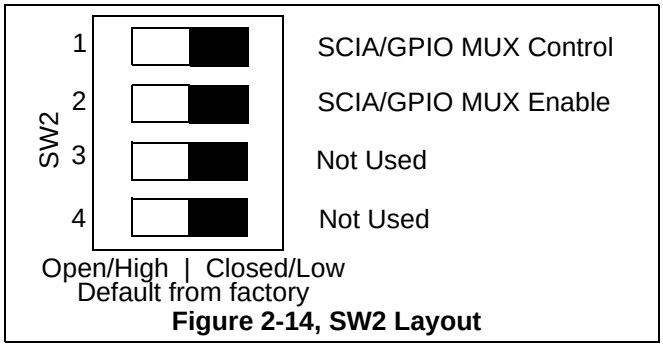


Figure 2-14, SW2 Layout

2.6 LEDs

The eZdsp^{TM} F2804x has two light-emitting diodes. DS1 indicates the presence of +5 volts and is normally ‘on’ when power is applied to the board. DS2 is under software control and is tied to the GPIO34 pin on the DSP through a buffer. These are shown in the table below.

Table 16: LEDs

LED #	Color	Controlling Signal
DS1	Green	+5 Volts
DS2	Green	GPIO34 bit (GPIO34 high = on)

2.7 Test Points

The eZdsp™ F2804x has two test points. The signals they are tied to are shown in the table below.

Table 17: Test Points

Test Point	Signal
J1	Analog Ground
J2	Ground

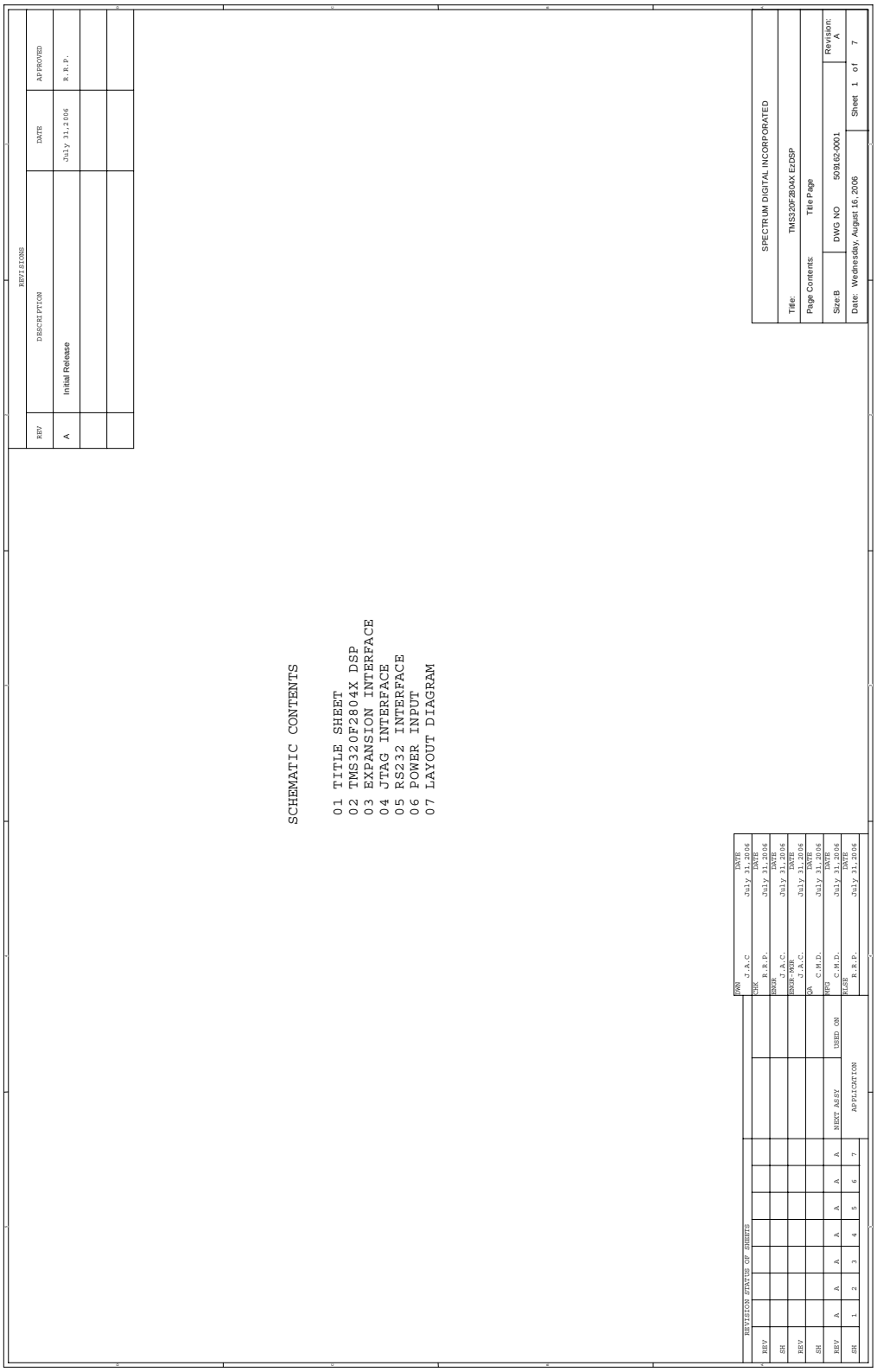
Appendix A

eZdsp™ F2804x Schematics

The schematics for the eZdsp™ F2804x can be found on the CD-ROM that accompanies this board. The schematics were drawn on ORCAD.

WARNING !

The TMS320F2804x supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F2804x. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent lactchup conditions.


REVISIONS
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Initial Release
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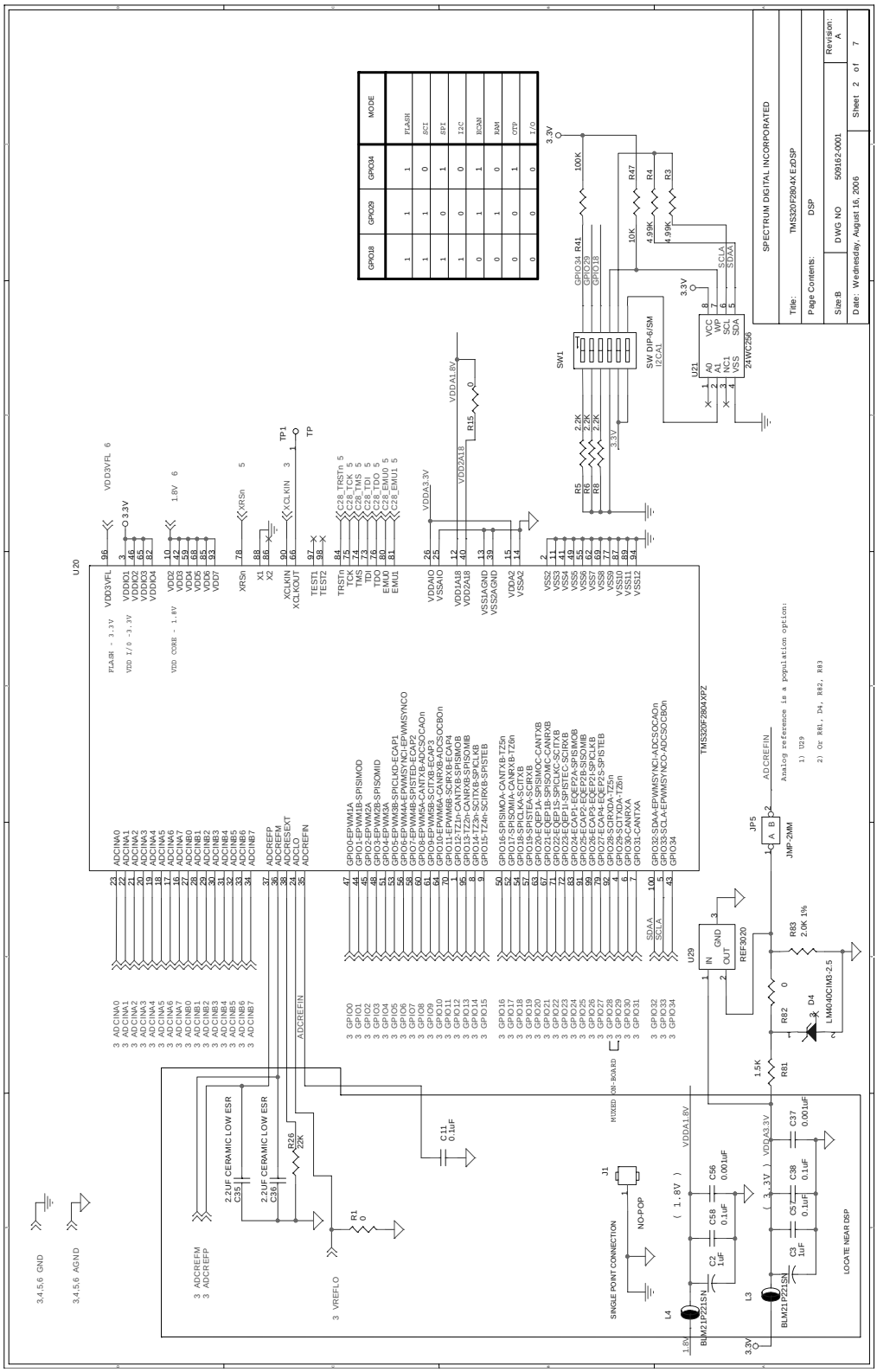
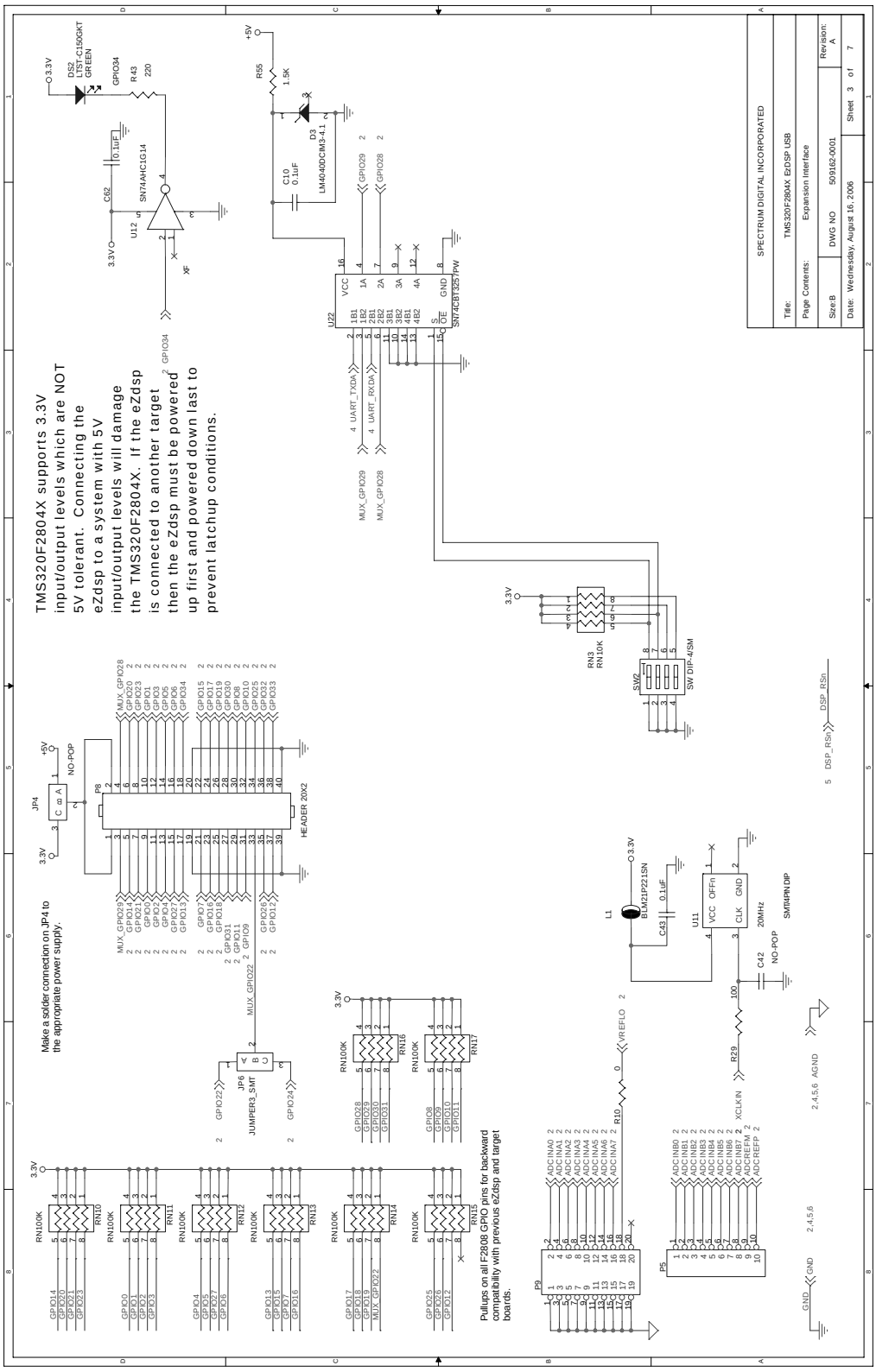
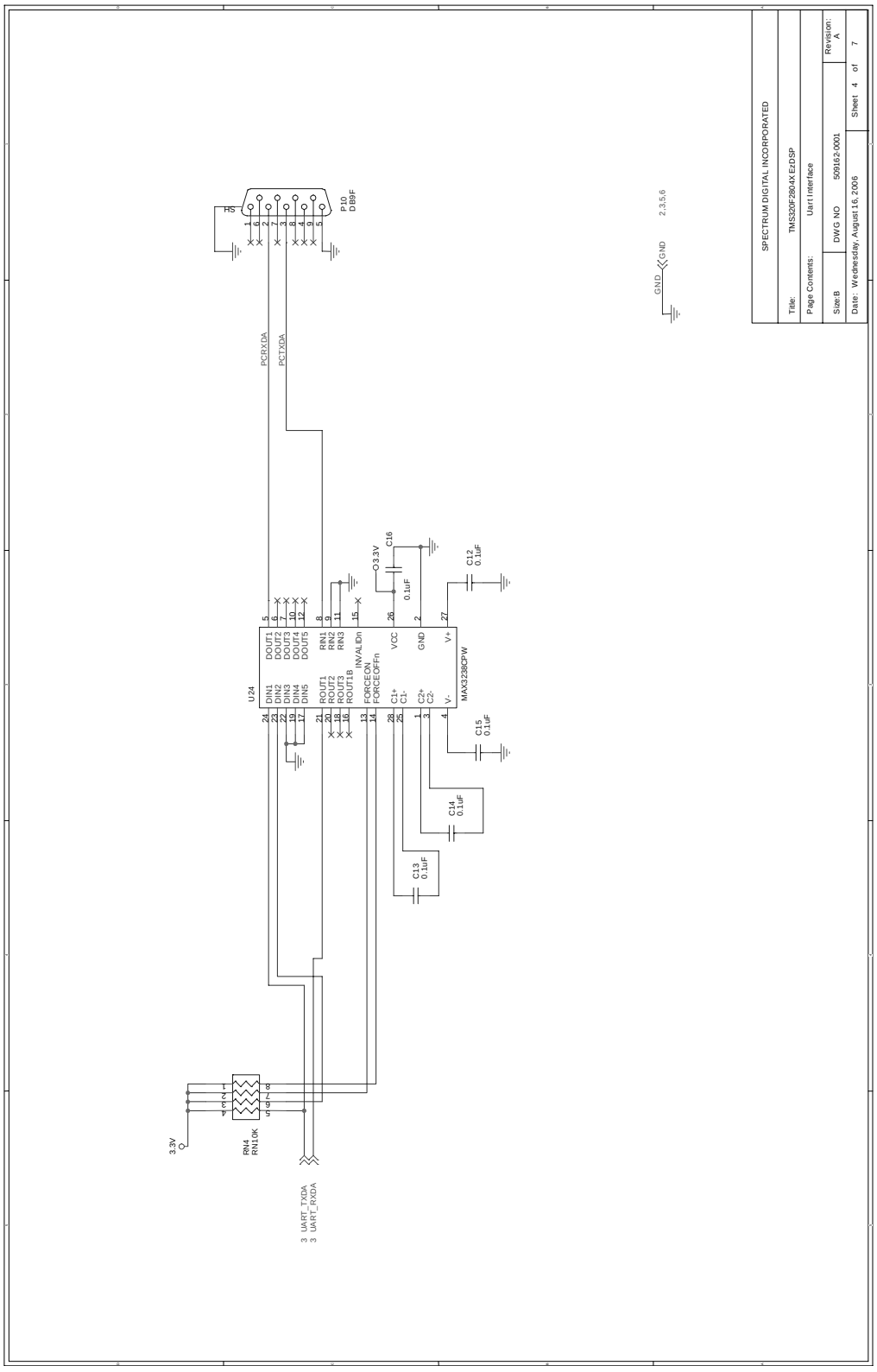
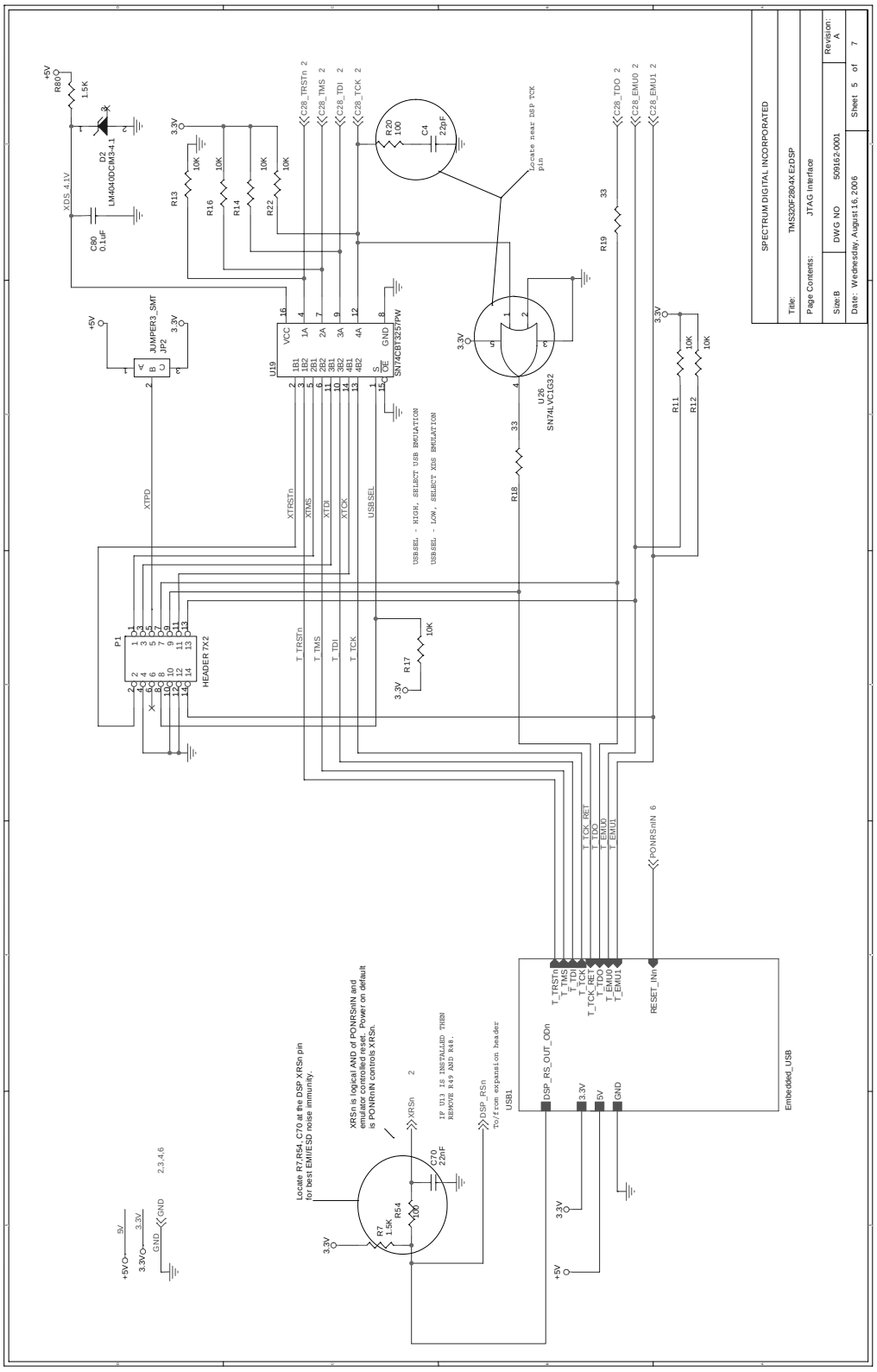
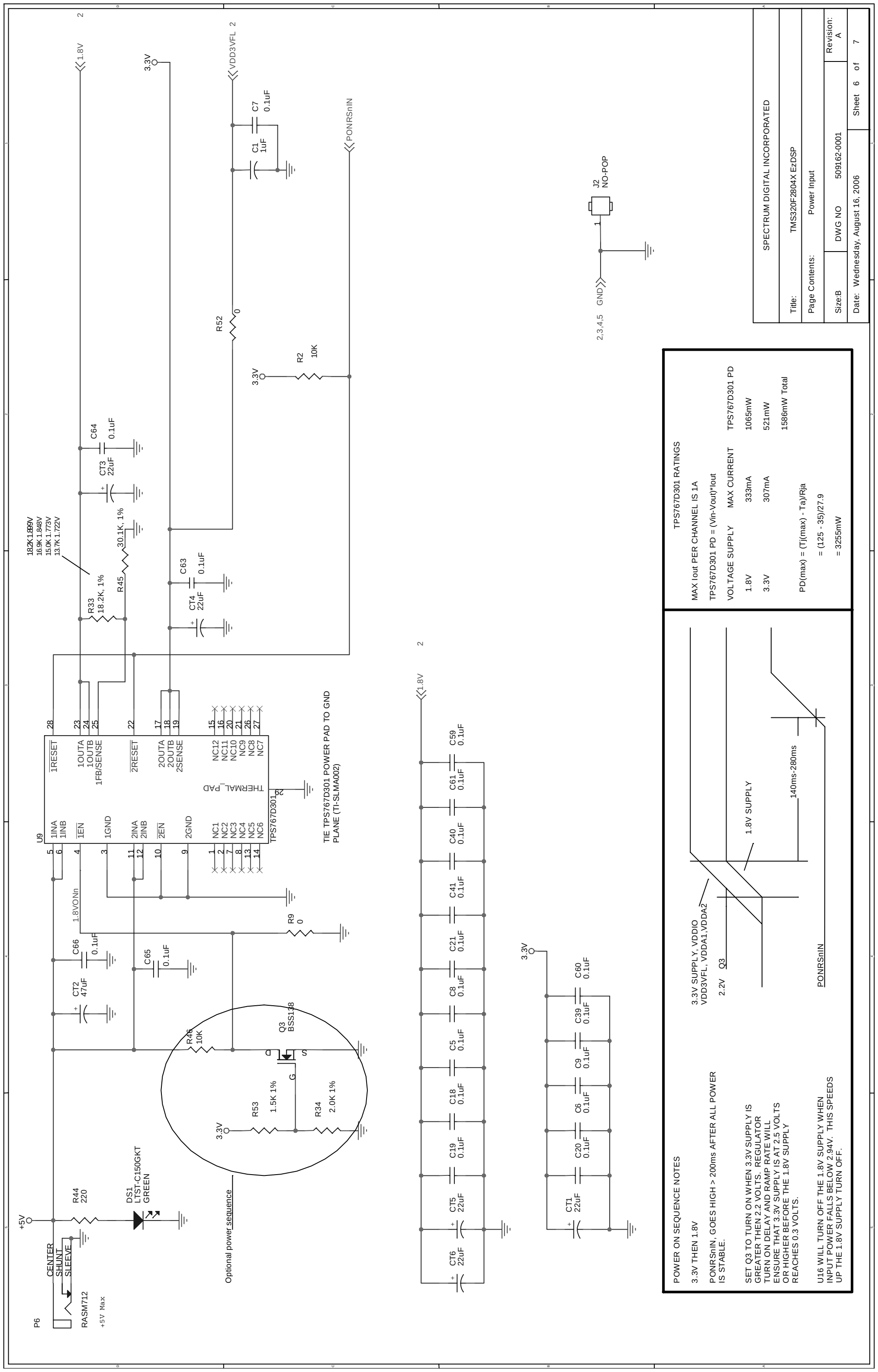
06 POWER INPUT
07 LAYOUT DIAGRAM
REVISION STATUS OF SHEETS
APPLICATION
NEXT ASSY
USED ON
DWN J.A.C. July 31,2006
CHK R.R.P. July 31,2006
ENGR J.A.C. July 31,2006
ENGR-MGR J.A.C. July 31,2006
QA C.M.D. July 31,2006
MFG C.M.D. July 31,2006
PLANT R.R.P. July 31,2006
SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP
Page Contents: Title Page
Size:B
DWG NO 5091162-0001
Revision: A
Date: Wednesday, August 16, 2006
Sheet 1 of 7


U20
TMS320F2804XPZ
U29
REF3020
U21
24WC256
SW1
SW DIP-6/SM
I2CA1
JP5
JMP-2MM
J1
SINGLE POINT CONNECTION
NO-POP
LOCATE NEAR DSP
MUXED CON-BOARD
SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP
Page Contents: DSP
Size:B
DWG NO 509162-0001
Revision: A
Date: Wednesday, August 16, 2006
Sheet 2 of 7

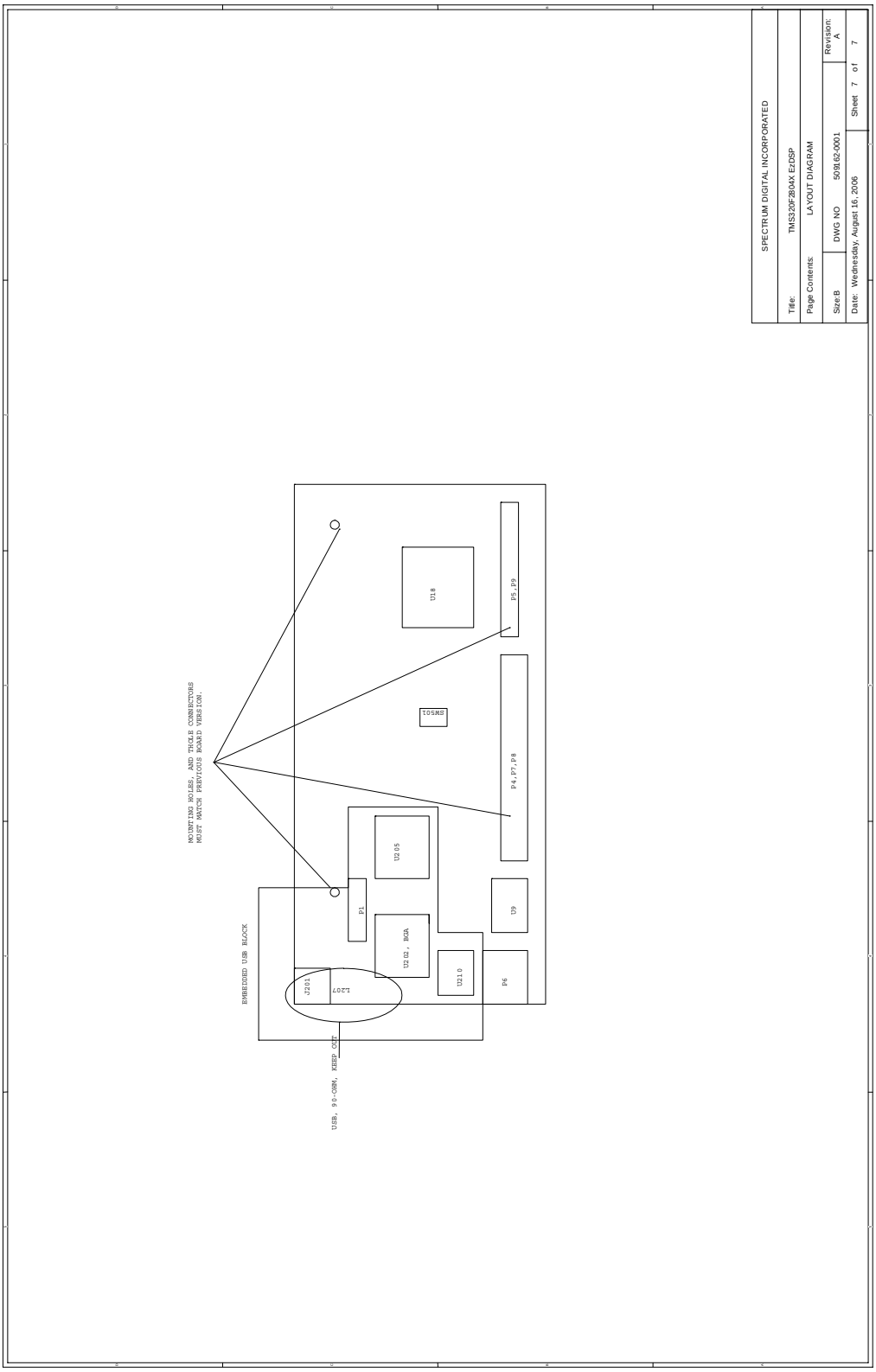

TMS320F2804X supports 3.3V input/output levels which are NOT 5V tolerant. Connecting the eZdsp to a system with 5V input/output levels will damage the TMS320F2804X. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent latchup conditions.
Make a solder connection on JP4 to the appropriate power supply.
Pullups on all F2808 GPIO pins for backward compatibility with previous eZdsp and target boards.
SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP USB
Page Contents: Expansion Interface
Size:B DWG NO 5091b2-0001 Revision: A
Date: Wednesday, August 16, 2006 Sheet 3 of 7


SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP
Page Contents: Uart Interface
Size:B
DWG NO 509162-0001
Revision: A
Date: Wednesday, August 16, 2006
Sheet 4 of 7
P10
DB9F
PCRXDA
PCTXDA
GND
2,3,5,6
U24
MAX3238CPW
DOUT1
DOUT2
DOUT3
DOUT4
DOUT5
DIN1
DIN2
DIN3
DIN4
DIN5
RIN1
RIN2
RIN3
ROUT1B
INVALIDn
FORCEON
FORCEOFFn
VCC
GND
V+
V-
C1+
C1-
C2+
C2-
3.3V
C16
0.1uF
C12
0.1uF
C15
0.1uF
C14
0.1uF
C13
0.1uF
RN4
RN10K
UART_TXDA
UART_RXDA


SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP
Page Contents: JTAG Interface
Size:B
DWG NO 509162-0001
Revision: A
Date: Wednesday, August 16, 2006
Sheet 5 of 7
HEADER 7X2
SN74CBT3257PW
SN74LVC1G32
JUMPER3_SMT
LM4040DCIM3-4.1
USB1
Embedded_USB
Locate R7,R54, C70 at the DSP XRSn pin for best EMI/ESD noise immunity.
XRSn is logical AND of PONRSnIN and emulator controlled reset. Power on default is PONRSnIN controls XRSn.
IF U13 IS INSTALLED THEN REMOVE R49 AND R46.
Locate near DSP TCK pin
USB.SEL - HIGH, SELECT USB EMULATION
USB.SEL - LOW, SELECT XDS EMULATION
To/from expansion header



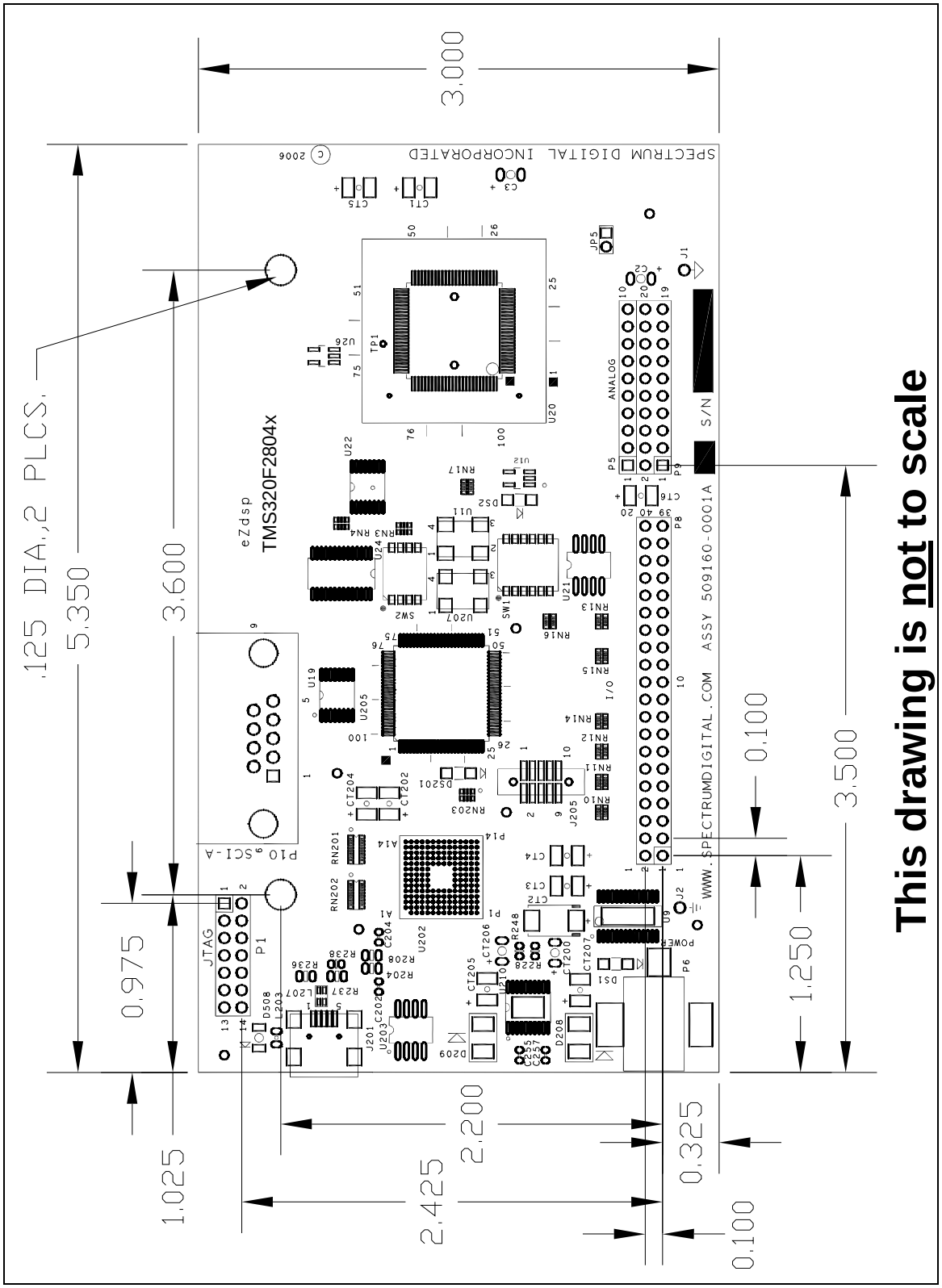
POWER ON SEQUENCE NOTES
3.3V THEN 1.8V
PONRSnIN, GOES HIGH > 200ms AFTER ALL POWER IS STABLE.
SET Q3 TO TURN ON WHEN 3.3V SUPPLY IS GREATER THEN 2.2 VOLTS. REGULATOR TURN ON DELAY AND RAMP RATE WILL ENSURE THAT 3.3V SUPPLY IS AT 2.5 VOLTS OR HIGHER BEFORE THE 1.8V SUPPLY REACHES 0.3 VOLTS.
U16 WILL TURN OFF THE 1.8V SUPPLY WHEN INPUT POWER FALLS BELOW 2.94V. THIS SPEEDS UP THE 1.8V SUPPLY TURN OFF.
3.3V SUPPLY, VDDIO
VDD3VFL, VDDA1,VDDA2
2.2V
Q3
1.8V SUPPLY
140ms-280ms
PONRSnIN
TPS767D301 RATINGS
MAX Iout PER CHANNEL IS 1A
TPS767D301 PD = (Vin-Vout)*Iout
VOLTAGE SUPPLY
MAX CURRENT
TPS767D301 PD
1.8V
333mA
1065mW
3.3V
307mA
521mW
1586mW Total
PD(max) = (Tj(max) - Ta)/Rja
= (125 - 35)/27.9
= 3255mW
SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP
Page Contents: Power Input
Size:B
DWG NO 509162-0001
Revision: A
Date: Wednesday, August 16, 2006
Sheet 6 of 7
TIE TPS767D301 POWER PAD TO GND PLANE (TI-SLMA002)
Optional power sequence
U9
TPS767D301
THERMAL_PAD
P6
RASM712
+5V Max
CENTER
SHUNT
SLEEVE
DS1
LTST-C150GKT
GREEN
Q3
BSS138
J2
NO-POP


SPECTRUM DIGITAL INCORPORATED
Title: TMS320F2804X EzDSP
Page Contents: LAYOUT DIAGRAM
Size:B
DWG NO 5081624-0001
Revision: A
Date: Wednesday, August 16, 2006
Sheet 7 of 7
MOUNTING HOLES, AND TRGLR CONNECTORS MUST MATCH PREVIOUS BOARD VERSION.
EMBEDDED USB BLOCK
USB, 90-OHM, KEEP OUT
U18
P5,P9
SW501
P4,P7,P8
U205
P1
U9
U202, BGA
U210
P6
J201
L201

Appendix B

eZdsp™ F2804x Mechanical Information

This appendix contains the mechanical information about the socketed and unsocketed versions of the eZdsp™ F2804x.


3.000
.125 DIA.,2 PLCS.
5.350
3.600
0.975
1.025
2.200
2.425
0.325
0.100
0.100
1.250
3.500
This drawing is not to scale
SPECTRUM DIGITAL INCORPORATED
eZdsp
TMS320F2804x
WWW.SPECTRUMDIGITAL.COM ASSY 509160-0001A
S/N
ANALOG
I/O
JTAG
P10 9 SCI-A

[redacted]

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