AD73360 Rev. 1

Errata Document

A. This document details the limitations of the cascading option of the AD73360 due to a bug in the current silicon.

B. Analog Devices Inc. is committed, through future silicon revisions to continuously improve silicon functionality.

Analog Devices Inc. will use its best endeavors to ensure that these future silicon revisions remain compatible with your present software/systems implementing the recommended work-arounds outlined in this document.

Background

The AD73360 has the option of being cascaded allowing additional analog input channels to be easily be added as required. Due to a bug in the present silicon there are limitations on how many devices can be cascaded together and is also dependent on the sample rate and serial clock rate used.

Issue Description

When a number of AD73360s are cascaded together they each output ADC channel data in a time-division multiplexed (TDM) format. For a cascade of N devices with all channels enabled the output sequence read by a DSP or Micro-controller would be

Device N – Channel 1, Device N-1 - Channel 1... Device 1 - Channel 1,

Device N - Channel 2, Device N-1 – Channel 2 ... Device 1 – Channel 2...,

...,

Device N – Channel 6, Device N-1 – Channel6 ..., Device 1 – Channel 6

As each device is programmed with the number of devices in the cascade it should therefore allow sufficient SCLKs for all other devices to transmit the ADC result of one channel before starting to transmit the next. For example in a cascade of two devices, Device 1 will transmit its Channel 1 result to Device 2 in 16 SCLK cycles. At the same time Device 2 is transmitting its Channel 1 result to the DSP or Microcontroller. Device 1 will then allow 16 SCLKs, when it does not transmit anything, allowing Device 2 to transmit the Channel 1 data from Device 1 to the DSP. An additional SCLK cycle is added to allow the next channels data to begin being transmitted on the falling edge of the SDOFS pulse. Figure 1 shows the timing for a two device cascade.

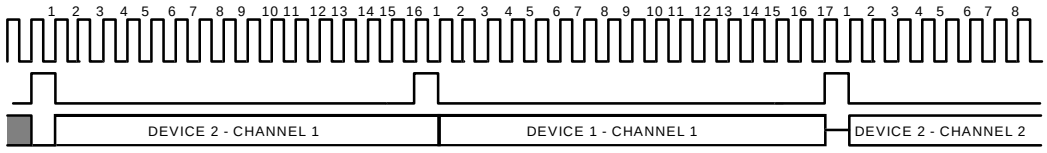

Figure 1. Cascade Timing for a Two-Device Cascade

For cascades of more than two devices the AD73360 will leave too many SCLKs between transmitting channel information. This increases the time it takes to transmit the ADC data and since a DSP or microcontroller must read data from all the ADCs in the cascade in one sample period the number of devices which can be cascaded will be limited. Figure 2 shows the effect the additional SCLKs have on a cascade of three devices.

Rev.A 6-2000

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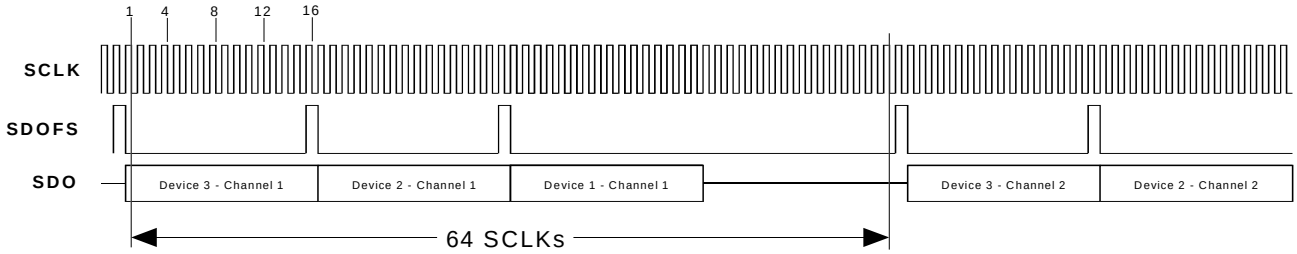

Figure 2. Cascade Timing for a Three-Device Cascade

Choosing SCLK rate and Sample Period

For a cascade of a given length, the SCLK rate and Sample Period will determine if the cascade can be used successfully. A low sample rate will allow more time for the ADC data to be read. Similarly a high SCLK rate will transmit the data in a shorter time. Since both the SCLK rate and Sample Rate are derived from the same DMCLK the number of combinations is limited. As most applications will require a predetermined sample rate, the SCLK speed will be the limitating factor in the cascade length that can be used. Table I shows the maximum cascade length for a given SCLK and Sample Rate. The table assumes that a MCLK of 16.384MHz is used.

Table I. Maximum Cascade Length with Various SCLK and Sample Rates

SCLK (MHz)	Max. Number of Devices	Sample Rate (KHz)
16.384	2	64
	3	32
	4	16
	5	8
8.192	1	64
	2	32
	3	16
	4	8
4.096	1	32
	2	16
	3	8
2.048	1	16
	2	8