

## Brief Description

The ZSSC3135 is a member of the ZSSC313x family of CMOS integrated circuits designed for automotive/industrial sensor applications. All family members are well suited for highly accurate amplification and sensor-specific correction of resistive bridge sensor signals. An internal 16-bit RISC microcontroller running a correction algorithm compensates sensor offset, sensitivity, temperature drift, and non-linearity of the connected sensor element. The required calibration coefficients are stored by the one-pass calibration procedure in an on-chip EEPROM.

The ZSSC3135 is specially designed for piezoresistive bridge sensor elements. The amplification stage with an analog gain of 105 in combination with optional temperature compensation via an external temperature sensor meets or exceeds the requirements of piezoresistive sensor applications.

## Features

- Adjustable to nearly all resistive bridge sensor types: analog gain of up to 105, maximum overall gain of 420
- Sample rate up to 200 Hz
- ADC resolution 13/14 bit
- Safety functionality sensor connection
- External temperature sensor
- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Output options: ratiometric analog voltage output (5 - 95% maximum, 12.4 bit resolution) or ZACwire™ (digital One-Wire Interface (OWI))
- Sensor biasing by voltage
- High voltage protection up to 33 V
- Supply current: max. 5.5mA
- Reverse polarity and short circuit protection
- Wide operation temperature range: -40 to +150°C
- Traceability by user-defined EEPROM entries

\* Note: I<sup>2</sup>C™ is a trademark of NXP.

\*\* FSO = Full Scale Output.

## Benefits

- Family approach offers the best fitting IC selection to build cost-optimized applications
- No external trimming components required
- Low number of external components needed
- PC-controlled configuration and one-pass/end-of-line calibration via I<sup>2</sup>C™\* or ZACwire™ interface: simple, cost-efficient, quick, and precise
- High accuracy: 0.25% FSO\*\* @ -25 to +85°C; 0.5% FSO @ -40 to +125°C
- Optimized for automotive/industrial environments due to robust protection circuitries, excellent electromagnetic compatibility and AEC-Q100 qualification

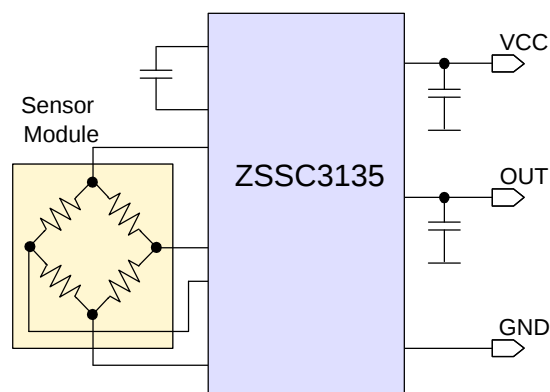
## Available Support

- Evaluation Kits
- Application Notes
- Mass Calibration System

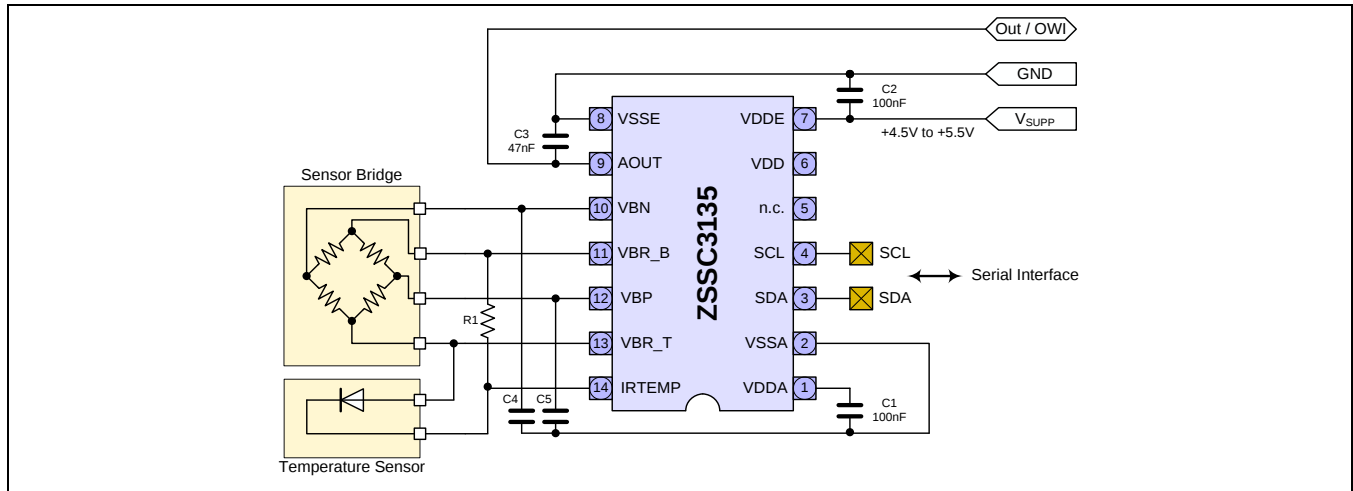
## Physical Characteristics

- Supply voltage: 4.5 to 5.5 V
- Operation temperature: -40°C to +125°C (-40°C to +150°C extended temperature range depending on product version)
- Available in RoHS-compliant JEDEC-SSOP14 package or delivery as die

## ZSSC3135 Minimum Application Requirements



## ZSSC3135 Application Example



## Ordering Information *(See data sheet section 8 for complete delivery options.)*

| Product Sales Code                    | Description                                                                                                                                                                                                         | Package                                                                    |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|
| ZSSC3135BE1                           | ZSSC3135 die – tested; temperature range -40 to +150°C                                                                                                                                                              | Unsawn wafer: add “B” to sales code<br>Die on frame: add “C” to sales code |
| ZSSC3135BA1                           | ZSSC3135 die – tested; temperature range -40 to +125°C                                                                                                                                                              | Unsawn wafer: add “B” to sales code<br>Die on frame: add “C” to sales code |
| ZSSC3135BE2                           | ZSSC3135 SSOP14 – temperature range -40 to +150°C                                                                                                                                                                   | Tube: add “T” to sales code<br>Tape & Reel: add “R”                        |
| ZSSC3135BA2                           | ZSSC3135 SSOP14 – temperature range -40 to +125°C                                                                                                                                                                   | Tube: add “T” to sales code<br>Tape & Reel: add “R”                        |
| ZSSC313xKITV1.1                       | ZSSC313x Evaluation Kit, revision 1.1 including Evaluation Board, ZSSC3135 IC samples, USB cable (software can be downloaded from the product page <a href="http://www.IDT.com/ZSSC3135">www.IDT.com/ZSSC3135</a> ) | Kit                                                                        |
| ZSSC313x Mass Calibration System V1.1 | Modular Mass Calibration System (MCS) for ZSSC313x including MCS boards, cable, connectors (software can be downloaded from the product page <a href="http://www.IDT.com/ZSSC3135">www.IDT.com/ZSSC3135</a> )       | Kit                                                                        |

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# 1 Electrical Characteristics

## 1.1. Absolute Maximum Ratings

**Note:** The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

Parameters apply in operation temperature range and without time limitations.

**Table 1.1 Absolute Maximum Ratings**

| No.   | Parameter                                 | Symbol                                 | Conditions                                           | Min  | Max        | Unit |
|-------|-------------------------------------------|----------------------------------------|------------------------------------------------------|------|------------|------|
| 1.1.1 | Supply voltage <sup>1)</sup>              | VDDE <sub>AMR</sub>                    | To VSSE, refer to section 3 for application circuits | -33  | 33         | VDC  |
| 1.1.2 | Potential at AOUT pin <sup>1)</sup>       | V <sub>OUT</sub>                       | Referenced to VSSE                                   | -33  | 33         | VDC  |
| 1.1.3 | Analog supply voltage <sup>1)</sup>       | VDDA <sub>AMR</sub>                    | Referenced to VSSA, VDDE - VDDA < 0.35V              | -0.3 | 6.5        | VDC  |
| 1.1.4 | Voltage at all analog and digital IO pins | V <sub>A_IO</sub><br>V <sub>D_IO</sub> | Referenced to VSSA                                   | -0.3 | VDDA + 0.3 | VDC  |
| 1.1.5 | Storage temperature                       | T <sub>STG</sub>                       |                                                      | -55  | 150        | °C   |

<sup>1)</sup> Refer to the ZSSC313x *High Voltage Protection Description* for specification and detailed conditions.

## 1.2. Operating Conditions

All voltages are referenced to VSSA.

**Table 1.2 Operating Conditions**

| No.   | Parameter                            | Symbol               | Conditions                                   | Min | Typ | Max | Unit |
|-------|--------------------------------------|----------------------|----------------------------------------------|-----|-----|-----|------|
| 1.2.1 | Ambient temperature <sup>1) 2)</sup> | T <sub>AMB_TQE</sub> | Extended Temperature Range (TQE)             | -40 |     | 150 | °C   |
|       |                                      | T <sub>AMB_TQA</sub> | Advanced-Performance Temperature Range (TQA) | -40 |     | 125 | °C   |
|       |                                      | T <sub>AMB_TQI</sub> | Best-Performance Temperature Range (TQI)     | -25 |     | 85  | °C   |
| 1.2.2 | Supply voltage                       | VDDE                 |                                              | 4.5 | 5.0 | 5.5 | VDC  |
| 1.2.3 | Bridge resistance <sup>3) 4)</sup>   | R <sub>BR</sub>      |                                              | 2   |     | 25  | kΩ   |

<sup>1)</sup> Maximum operation temperature range depends on product version (refer to section 8).  
<sup>2)</sup> See the temperature profile description in the ZSSC313x *Technical Note—Die & Package Dimensions*.  
<sup>3)</sup> No measurement in mass production; parameter is guaranteed by design and/or quality observation.  
<sup>4)</sup> Symmetric behavior and identical electrical properties (especially the low pass characteristic) of both sensor inputs of the ZSSC3135 are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins of the ZSSC3135 can generate a failure in signal operation.

### 1.3. Electrical Parameters

All parameter values are valid under the operating conditions specified in section 1.2 (special definitions excluded). All voltages referenced to VSSA.

Note: See important notes at the end of Table 1.3.

**Table 1.3 Electrical Parameters**

| No.                                                          | Parameter                                                 | Symbol        | Conditions                                                          | Min  | Typ | Max  | Unit            |
|--------------------------------------------------------------|-----------------------------------------------------------|---------------|---------------------------------------------------------------------|------|-----|------|-----------------|
| <b>1.3.1. Supply Current and System Operation Conditions</b> |                                                           |               |                                                                     |      |     |      |                 |
| 1.3.1.1                                                      | Supply current                                            | $I_S$         | Without bridge and load current, $f_{OSC} \leq 3$ MHz               |      |     | 5.5  | mA              |
| 1.3.1.2                                                      | Oscillator frequency <sup>1)</sup>                        | $f_{OSC}$     | Adjustment guaranteed for full temperature range ( $T_{AMB\_TQE}$ ) | 2    | 3   | 4    | MHz             |
| <b>1.3.2. Analog Front-End (AFE) Characteristics</b>         |                                                           |               |                                                                     |      |     |      |                 |
| 1.3.2.1                                                      | Input span                                                | $V_{IN\_SP}$  | Analog gain: 105 to 2.8                                             | 8    |     | 275  | mV/V            |
| 1.3.2.2                                                      | Parasitic differential input offset current <sup>1)</sup> | $I_{IN\_OFF}$ | Temperature range $T_{AMB\_TQE}$                                    | -10  |     | 10   | nA              |
|                                                              |                                                           |               | Temperature range $T_{AMB\_TQI}$                                    | -2   |     | 2    | nA              |
| 1.3.2.3                                                      | Common mode input range                                   | $V_{IN\_CM}$  | Depends on gain adjustment; see section 2.3.1                       | 0.29 |     | 0.65 | VDDA            |
| <b>1.3.3. Temperature Measurement<sup>2)</sup></b>           |                                                           |               |                                                                     |      |     |      |                 |
| 1.3.3.1                                                      | Internal temperature diode sensitivity                    | $ST_{TSI}$    | Raw values, without conditioning                                    | 700  |     | 2700 | ppm FS / K      |
| 1.3.3.2                                                      | External temperature diode channel gain                   | $AT_{SED}$    |                                                                     | 300  |     | 1300 | ppm FS / (mV/V) |
| 1.3.3.3                                                      | External temperature diode bias current                   | $IT_{SED}$    |                                                                     | 6    | 10  | 20   | $\mu$ A         |
| 1.3.3.4                                                      | External temperature diode input range <sup>1)</sup>      | $VT_{SED}$    |                                                                     | 0    |     | 1.5  | V               |
| 1.3.3.5                                                      | External temperature resistor channel gain                | $AT_{SER}$    |                                                                     | 1200 |     | 3500 | ppm FS / (mV/V) |
| 1.3.3.6                                                      | External temperature resistor input range <sup>1)</sup>   | $VT_{SER}$    |                                                                     | 0    |     | 600  | mV/V            |

| No.                                 | Parameter                                  | Symbol              | Conditions                                                                                                                            | Min  | Typ | Max  | Unit             |
|-------------------------------------|--------------------------------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|------------------|
| <b>1.3.4. A/D Conversion</b>        |                                            |                     |                                                                                                                                       |      |     |      |                  |
| 1.3.4.1                             | A/D resolution <sup>1)</sup>               | $r_{ADC}$           |                                                                                                                                       | 13   |     | 14   | Bit              |
| 1.3.4.2                             | DNL <sup>1)</sup>                          | $DNL_{ADC}$         | $r_{ADC}=13\text{bit}$ , $f_{OSC}=3\text{MHz}$ , best fit, complete AFE, range according to 1.3.4.5                                   |      |     | 0.95 | LSB              |
| 1.3.4.3                             | INL TQA                                    | $INL_{ADC}$         | $r_{ADC}=13\text{bit}$ , $f_{OSC}=3\text{MHz}$ , best fit, complete AFE, range according to 1.3.4.5                                   |      |     | 4    | LSB              |
| 1.3.4.4                             | INL TQE                                    | $INL_{ADC\_TQE}$    | $r_{ADC}=13\text{bit}$ , $f_{OSC}=3\text{MHz}$ , best fit, complete AFE, range according to 1.3.4.5, temperature range $T_{AMB\_TQE}$ |      |     | 5    | LSB              |
| 1.3.4.5                             | ADC input range                            | $V_{ADC\_IN}$       |                                                                                                                                       | 0.1  |     | 0.9  | VDDA             |
| <b>1.3.5. Sensor Check</b>          |                                            |                     |                                                                                                                                       |      |     |      |                  |
| 1.3.5.1                             | Sensor connection loss                     | $R_{SCC\_min}$      | Detection threshold                                                                                                                   | 100  |     |      | k $\Omega$       |
| 1.3.5.2                             | Sensor input short                         | $R_{SSC\_short}$    | Short detection guaranteed                                                                                                            | 0    |     | 50   | $\Omega$         |
| 1.3.5.3                             | Sensor input no short                      | $R_{SSC\_pass}$     | Corresponds with minimum sensor output resistance                                                                                     | 1000 |     |      | $\Omega$         |
| <b>1.3.6. DAC and Analog Output</b> |                                            |                     |                                                                                                                                       |      |     |      |                  |
| 1.3.6.1                             | D/A resolution                             | $r_{DAC}$           | Analog output, 10-90%                                                                                                                 |      | 12  |      | Bit              |
| 1.3.6.2                             | Output current sink and source for VDDE=5V | $I_{OUT\_SRC/SINK}$ | $V_{OUT}$ : 5-95%, $R_{LOAD} \geq 2\text{k}\Omega$                                                                                    |      |     | 2.5  | mA               |
|                                     |                                            |                     | $V_{OUT}$ : 10-90%, $R_{LOAD} \geq 1\text{k}\Omega$                                                                                   |      |     | 5    | mA               |
| 1.3.6.3                             | Short circuit current                      | $I_{OUT\_max}$      | To VDDE or VSSE <sup>3)</sup>                                                                                                         | -25  |     | 25   | mA               |
| 1.3.6.4                             | Output signal range                        | $V_{OUT\_RANGE}$    | With $R_{LOAD} \geq 2\text{k}\Omega$                                                                                                  | 0.05 |     | 0.95 | VDDE             |
|                                     |                                            |                     | With $R_{LOAD} \geq 1\text{k}\Omega$                                                                                                  | 0.1  |     | 0.90 | VDDE             |
| 1.3.6.5                             | Output slew rate <sup>1)</sup>             | $SR_{OUT}$          | $C_{LOAD} < 50\text{nF}$                                                                                                              | 0.1  |     |      | V/ $\mu\text{s}$ |
| 1.3.6.6                             | Output resistance in diagnostic mode       | $R_{OUT\_DM}$       | Diagnostic range:<br><4 to 96>%, $R_{LOAD} \geq 2\text{k}\Omega$<br><8 to 92>%, $R_{LOAD} \geq 1\text{k}\Omega$                       |      |     | 82   | $\Omega$         |
| 1.3.6.7                             | Load capacitance <sup>1)</sup>             | $C_{LOAD}$          | $C3 + C_{LOAD}$<br>(refer to section 3)                                                                                               |      |     | 150  | nF               |
| 1.3.6.8                             | DNL                                        | $DNL_{OUT}$         |                                                                                                                                       | -1.5 |     | 1.5  | LSB              |
| 1.3.6.9                             | INL TQA                                    | $INL_{OUT}$         | Best fit, $r_{DAC}=12\text{bit}$                                                                                                      | -5   |     | 5    | LSB              |
| 1.3.6.10                            | INL TQE                                    | $INL_{OUT\_TQE}$    | Best fit, $r_{DAC}=12\text{bit}$ ,<br>temperature range $T_{AMB\_TQE}$                                                                | -8   |     | 8    | LSB              |
| 1.3.6.11                            | Output leakage current at 150°C            | $I_{OUT\_LEAK}$     | In case of power or ground loss                                                                                                       | -25  |     | 25   | $\mu\text{A}$    |

| No.                                                                                                                                                                                                                                                                                                                                   | Parameter                                                                                                                                                                          | Symbol                   | Conditions                                                                                 | Min | Typ           | Max  | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------------------------------------------------------------------------------------|-----|---------------|------|------|
| 1.3.7. System Response                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                    |                          |                                                                                            |     |               |      |      |
| 1.3.7.1                                                                                                                                                                                                                                                                                                                               | Startup time <sup>1) 4)</sup><br>(To 1 <sup>st</sup> output, ROM check disabled)                                                                                                   | t <sub>STARTUP</sub>     | 1-step ADC, f <sub>OSC</sub> =3MHz<br>r <sub>ADC</sub> =14bit)                             |     |               | 35   | ms   |
| 1.3.7.2                                                                                                                                                                                                                                                                                                                               | Response time <sup>1)</sup><br>(100% input step; refer to Table 2.2)                                                                                                               | t <sub>RESPONSE</sub>    | 1-step ADC, f <sub>OSC</sub> =4MHz,<br>r <sub>ADC</sub> =13bit                             | 8.7 | 13.1          | 17.4 | ms   |
| 1.3.7.3                                                                                                                                                                                                                                                                                                                               | Bandwidth <sup>1)</sup><br>(In comparison to an equivalent analog SSC. Refer to Table 2.2)                                                                                         | BW                       | 1-step ADC                                                                                 |     |               | 200  | Hz   |
| 1.3.7.4                                                                                                                                                                                                                                                                                                                               | Analog output noise peak-to-peak <sup>1)</sup>                                                                                                                                     | V <sub>NOISE_PP</sub>    | Shorted inputs<br>bandwidth ≤ 10kHz                                                        |     |               | 10   | mV   |
| 1.3.7.5                                                                                                                                                                                                                                                                                                                               | Analog output noise RMS <sup>1)</sup>                                                                                                                                              | V <sub>NOISE_RMS</sub>   | Shorted inputs<br>bandwidth ≤ 10kHz                                                        |     |               | 3    | mV   |
| 1.3.7.6                                                                                                                                                                                                                                                                                                                               | Ratiometricity error                                                                                                                                                               | RE                       | Maximum error for<br>VDDE=5V to 4.5/5.5V                                                   |     |               | 1000 | ppm  |
| 1.3.7.7                                                                                                                                                                                                                                                                                                                               | Overall failure<br>Deviation from ideal line including INL, gain, offset and temperature errors.<br>No sensor-caused effects.<br>Failure for digital readout shown in parenthesis. | F <sub>OVERALL_TQI</sub> | f <sub>OSC</sub> ≤3MHz, r <sub>ADC</sub> =13bit,<br>temperature range T <sub>AMB_TQI</sub> |     | 0.25<br>(0.1) |      | % FS |
|                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                    | F <sub>OVERALL_TQA</sub> | f <sub>OSC</sub> ≤3MHz, r <sub>ADC</sub> =13bit,<br>temperature range T <sub>AMB_TQA</sub> |     | 0.5<br>(0.25) |      | % FS |
|                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                    | F <sub>OVERALL_TQE</sub> | f <sub>OSC</sub> ≤3MHz, r <sub>ADC</sub> =13bit,<br>temperature range T <sub>AMB_TQE</sub> |     | 1.0<br>(0.5)  |      | % FS |
| 1) No measurement in mass production; parameter is guaranteed by design and/or quality observation.<br>2) Refer to section 2.4 for important details.<br>3) Minimum output voltage to VDDE or maximum output voltage to VSSE.<br>4) Depends on resolution and configuration. Start routine begins approximately 0.8ms after power on. |                                                                                                                                                                                    |                          |                                                                                            |     |               |      |      |

## 1.4. Interface Characteristics and EEPROM

**Table 1.4** *Interface Characteristics and EEPROM*

| No.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Parameter                                                | Symbol                              | Conditions                                                                     | Min  | Typ | Max                 | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------------------------------------|--------------------------------------------------------------------------------|------|-----|---------------------|------|
| <b>1.4.1. I<sup>2</sup>C™ Interface</b> <sup>1)</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                          |                                     |                                                                                |      |     |                     |      |
| 1.4.1.1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | I <sup>2</sup> C™ voltage level HIGH                     | V <sub>I<sup>2</sup>C,HIGH</sub>    |                                                                                | 0.8  |     |                     | VDDA |
| 1.4.1.2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | I <sup>2</sup> C™ voltage level LOW <sup>2)</sup>        | V <sub>I<sup>2</sup>C,LOW</sub>     |                                                                                |      |     | 0.2                 | VDDA |
| 1.4.1.3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Slave output level LOW <sup>2)</sup>                     | V <sub>I<sup>2</sup>C,LOW_OUT</sub> | Open drain, I <sub>OL</sub> <2mA                                               |      |     | 0.15                | VDDA |
| 1.4.1.4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | SDA load capacitance <sup>2)</sup>                       | C <sub>SDA</sub>                    |                                                                                |      |     | 400                 | pF   |
| 1.4.1.5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | SCL clock frequency <sup>2)</sup>                        | f <sub>I<sup>2</sup>C</sub>         | f <sub>OSC</sub> ≥2MHz                                                         |      |     | 400                 | kHz  |
| 1.4.1.6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Internal pull-up resistor <sup>2)</sup>                  | R <sub>I<sup>2</sup>C,PULLUP</sub>  |                                                                                | 25   |     | 100                 | kΩ   |
| <b>1.4.2. ZACwire™ One-Wire Interface (OWI)</b> <sup>1)</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                          |                                     |                                                                                |      |     |                     |      |
| 1.4.2.1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | OWI voltage level HIGH <sup>2)</sup>                     | V <sub>OWI,HIGH</sub>               |                                                                                | 0.75 |     |                     | VDDA |
| 1.4.2.2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | OWI voltage level LOW <sup>2)</sup>                      | V <sub>OWI,LOW</sub>                |                                                                                |      |     | 0.2                 | VDDA |
| 1.4.2.3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Slave output level LOW <sup>2)</sup>                     | V <sub>OWI,LOW_OUT</sub>            | Open drain, I <sub>OL</sub> <2mA                                               |      |     | 0.15                | VDDA |
| 1.4.2.4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Start window <sup>2)</sup>                               | t <sub>OWI,STARTWIN</sub>           | At f <sub>OSC</sub> =3MHz                                                      | 96   | 175 | 455                 | ms   |
| <b>1.4.3. EEPROM</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                          |                                     |                                                                                |      |     |                     |      |
| 1.4.3.1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Ambient temperature for EEPROM programming <sup>2)</sup> | T <sub>AMB_EEP</sub>                |                                                                                | -40  |     | 150                 | °C   |
| 1.4.3.2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Write cycles <sup>2)</sup>                               | n <sub>EEP_WRI</sub>                | Write ≤ 85°C                                                                   |      |     | 100 000             |      |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                          |                                     | Write up to 150°C                                                              |      |     | 100                 |      |
| 1.4.3.3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Read cycles <sup>2) 3)</sup>                             | n <sub>EEP_READ</sub>               | ≤175°C                                                                         |      |     | 8 * 10 <sup>8</sup> |      |
| 1.4.3.4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Data retention <sup>2) 4)</sup>                          | t <sub>EEP_RETENTION</sub>          | 1300h at 175°C<br>(= 3000h at 150°C<br>+ 27000h at 125°C<br>+ 100000h at 55°C) |      |     | 15                  | a    |
| 1.4.3.5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Programming time <sup>2)</sup>                           | t <sub>EEP_WRI</sub>                | Per written word                                                               |      | 12  |                     | ms   |
| <sup>1)</sup> Refer to the ZSSC313x <i>Functional Description</i> for timing details.<br><sup>2)</sup> No measurement in mass production, parameter is guaranteed by design and/or quality observation.<br><sup>3)</sup> Valid for the dice. Note that the package and the temperature version cause additional restrictions.<br><sup>4)</sup> Over lifetime and valid for the dice. Use the calculation sheet <i>IDT Temperature Profile Calculation Sheet</i> for temperature stress calculation. Note that the package and the temperature version cause additional restrictions. |                                                          |                                     |                                                                                |      |     |                     |      |

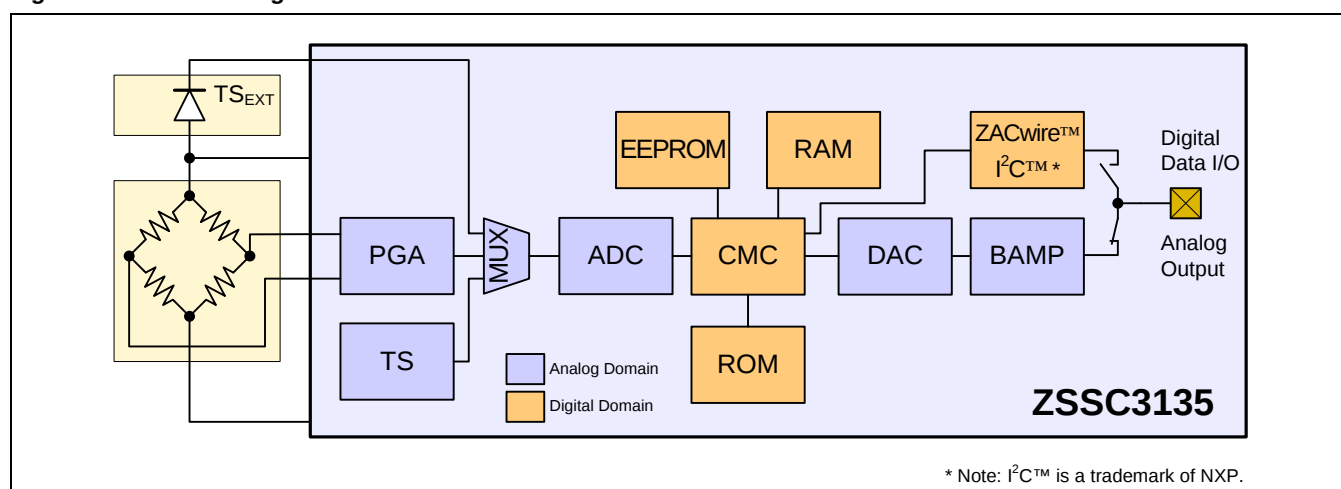
## 2 Circuit Description

### 2.1. Signal Flow

The ZSSC3135's signal path is partly analog and partly digital. The analog section is differential – this means the differential bridge sensor signal is internally handled via two signal lines that are rejected symmetrically around an internal common mode potential (analog ground =  $V_{DDA}/2$ ).

As a result of the differential design, it is possible to amplify positive and negative input signals that are within the common mode range of the signal input.

**Figure 2.1 Block Diagram of the ZSSC3135**



|                   |                                                                  |
|-------------------|------------------------------------------------------------------|
| PGA               | Programmable Gain Amplifier                                      |
| TS                | On-Chip Temperature Sensor (pn-junction)                         |
| TS <sub>EXT</sub> | External Temperature Sensor (pn-junction)                        |
| MUX               | Multiplexer                                                      |
| ADC               | Analog-to-Digital Converter                                      |
| CMC               | Calibration Microcontroller                                      |
| ROM               | Read-Only Memory for Correction Formula and Algorithm            |
| RAM               | Volatile Memory for Calibration Parameters and Configuration     |
| EEPROM            | Non-volatile Memory for Calibration Parameters and Configuration |
| DAC               | Digital-to-Analog Converter                                      |
| BAMP              | Output Buffer Amplifier                                          |

The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The multiplexer (MUX) transmits the signals from either the bridge sensor or the internal or external temperature sensor to the analog-to-digital converter (ADC) in a specific sequence. The ADC converts these signals into digital values.

The digital signal conditioning is processed by the calibration microcontroller (CMC). It is based on a correction formula that uses sensor-specific coefficients determined during calibration. The formula is located in ROM, and the sensor-specific coefficients are stored in EEPROM. Depending on the programmed output configuration, the conditioned sensor signal is output as an analog signal or alternatively can be readout via a digital serial interface (I<sup>2</sup>C™ or ZACwire™). The configuration data and the correction parameters must also be programmed into the EEPROM via the digital interfaces.

## 2.2. Application Modes

For each application, a configuration set must be established by programming the on-chip EEPROM for the following modes:

- Sensor channel
  - Input range: The gain adjustment of the analog front-end (AFE) with respect to the maximum sensor signal span and the zero point of the A/D conversion must be selected.
  - Resolution/response time: The A/D converter must be configured for resolution. These settings influence the sampling rate and the signal integration time, and thus, the noise immunity.
- Temperature
  - Temperature measurement: Select the internal or external temperature sensor.

## 2.3. Analog Front-End (AFE)

The analog front-end (AFE) consists of the three-stage programmable gain amplifier (PGA), the multiplexer (MUX), and the analog-to-digital converter (ADC).

### 2.3.1. Programmable Gain Amplifier (PGA)

Table 2.1 shows the adjustable gains, the sensor signal spans, and the valid common mode range.

**Table 2.1 Adjustable Gains, Resulting Sensor Signal Spans and Common Mode Ranges**

| PGA Gain<br>$a_{IN}$                                                                                                                                                                 | Maximum Span<br>$V_{IN\_SP}$ [mV/V] <sup>1)</sup> | Input Common Mode Range<br>$V_{IN\_CM}$ [% VDDA] |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|--------------------------------------------------|
| 105                                                                                                                                                                                  | 7.1                                               | 29 to 65                                         |
| 70                                                                                                                                                                                   | 10.7                                              | 29 to 65                                         |
| 52.5                                                                                                                                                                                 | 14.3                                              | 29 to 65                                         |
| 35                                                                                                                                                                                   | 21.4                                              | 29 to 65                                         |
| 26.3                                                                                                                                                                                 | 28.5                                              | 29 to 65                                         |
| 14                                                                                                                                                                                   | 53.75                                             | 29 to 65                                         |
| 9.3                                                                                                                                                                                  | 80                                                | 29 to 65                                         |
| 7                                                                                                                                                                                    | 107                                               | 29 to 65                                         |
| 2.8                                                                                                                                                                                  | 267                                               | 32 to 57                                         |
| <sup>1)</sup> Recommended maximum internal signal range is 75% of the supply voltage.<br>Span is calculated by the following formula: $Span = 0.75 (V_{BR\_T} - V_{BR\_B}) / Gain$ . |                                                   |                                                  |

### 2.3.2. Offset Compensation

The ZSSC3135 processes a sensor-offset correction during the digital signal conditioning by the calibration microcontroller (CMC).

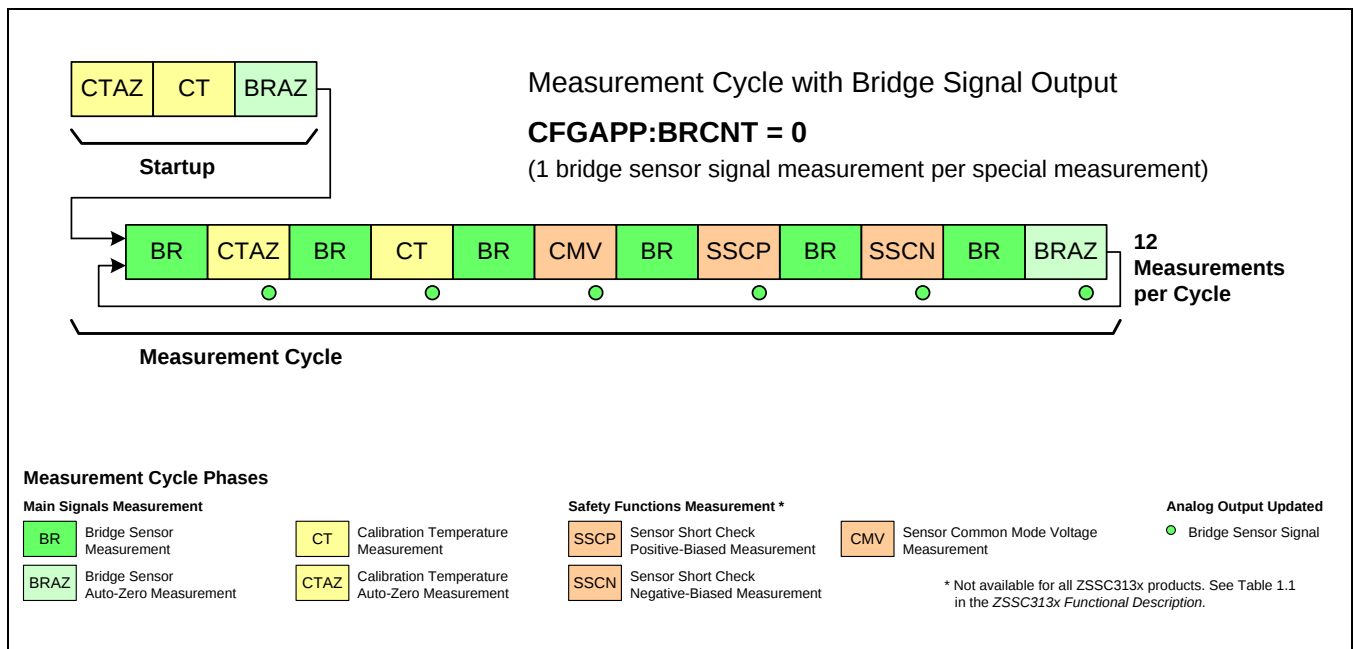
### 2.3.3. Measurement Cycle

The measurement cycle is controlled by the CMC. Depending on EEPROM settings, the multiplexer (MUX) selects the following input signals in a defined sequence:

- Pre-amplified bridge sensor signal
- Temperature sensor signal
- Internal offset of the input channel ( $V_{OFF}$ )

The cycle diagram in Figure 2.2 shows the basic structure of the measurement cycle. After power-on, the startup routine is processed, which performs all required measurements to expedite acquiring an initial valid conditioned sensor output. After the startup routine, the normal measurement cycle runs.

**Figure 2.2 Measurement Cycle with 1 Bridge Sensor Signal Measurement per Special Measurement**



### 2.3.4. Analog-to-Digital Converter

The A/D converter is implemented using full-differential switched-capacitor technique.

Programmable ADC resolutions are  $r_{ADC} = \{13, 14\}$  bit.

The A/D conversion is integrating, inherently monotone, and insensitive to short and long term instability of the clock frequency. The conversion time  $t_{ADC}$  depends on the desired resolution and can be roughly calculated by equation (1):

$$t_{ADC} = \frac{2^{r_{ADC}}}{\left(\frac{f_{OSC}}{2}\right)} \quad (1)$$

Where

|           |                                                   |
|-----------|---------------------------------------------------|
| $r_{ADC}$ | Resolution of A/D conversion                      |
| $f_{OSC}$ | Frequency of internal oscillator (refer to 1.3.1) |

Refer to the *ZSSC313x Bandwidth Calculation Sheet* for a detailed calculation of sampling time and bandwidth.

The result of the A/D conversion is a relative counter result Z corresponding to the following equation:

$$Z = 2^{r_{ADC}} \cdot \left( \frac{V_{ADC\_DIFF}}{V_{ADC\_REF}} - RS \right) \quad (2)$$

Where

|                 |                                                                                                                                                                               |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $r_{ADC}$       | Resolution of A/D conversion                                                                                                                                                  |
| $V_{ADC\_DIFF}$ | Differential ADC input voltage                                                                                                                                                |
| $V_{ADC\_REF}$  | ADC reference voltage as selected by the BRREF bits in the EEPROM configuration word CFGAPP ( $V_{VBR\_T} - V_{VBR\_B}$ if BRREF= 0) or ( $V_{VDDA} - V_{VSSA}$ if BRREF=1) * |
| RS              | Digital ADC Range Shift (RS = 1/16, 1/8, 1/4, or 1/2; controlled by the ADCRS bits in the EEPROM configuration word CFGAFE) *                                                 |

With the RS value, a sensor input signal can be shifted in the optimal input range of the ADC.

The condition required for ensuring the specified accuracy, stability, and non-linearity parameters of the analog front-end is that the differential ADC input voltage  $V_{ADC\_DIFF}$  does not exceed the range of 10% to 90% of the ADC reference voltage  $V_{ADC\_REF}$ . This requirement must be met for the whole temperature range and for all sensor tolerances.

\* Refer to the *ZSSC313x Functional Description* for more information on EEPROM contents.

**Table 2.2 ADC Resolution versus Output Resolution and Sample Rate**

| ADC Adjustment                                                                                                                                                                                                                                                                                                                  | Output Resolution <sup>1)</sup> |              | Sample Rate <sup>2)</sup>   |                             | Averaged Bandwidth <sup>2)</sup> |                             |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|--------------|-----------------------------|-----------------------------|----------------------------------|-----------------------------|
|                                                                                                                                                                                                                                                                                                                                 | Digital [bit]                   | Analog [bit] | f <sub>osc</sub> =3MHz [Hz] | f <sub>osc</sub> =4MHz [Hz] | f <sub>osc</sub> =3MHz [Hz]      | f <sub>osc</sub> =4MHz [Hz] |
| 13                                                                                                                                                                                                                                                                                                                              | 13                              | 12           | 345                         | 460                         | 130                              | 172                         |
| 14                                                                                                                                                                                                                                                                                                                              | 14                              | 12           | 178                         | 237                         | 67                               | 89                          |
| 1) Output resolution does not exceed ADC resolution. PGA gain should be such that the differential ADC input signal uses at least 50% of the ADC input range to ensure maximum achievable output resolution.<br>2) Refer to the ZSSC313x Bandwidth Calculation Sheet for a detailed calculation of sampling time and bandwidth. |                                 |              |                             |                             |                                  |                             |

## 2.4. Temperature Measurement

The ZSSC3135 supports different methods for acquiring temperature data needed for conditioning of the sensor signal. Temperature data can be acquired using

- an internal pn-junction temperature sensor,
- an external pn-junction temperature sensor connected to the sensor top potential ( $V_{BR\_T}$ ), or
- an external resistive half bridge temperature sensor.

Refer to the ZSSC313x *Functional Description* for a detailed explanation of temperature sensor adaptation and adjustment.

## 2.5. System Control and Conditioning Calculation

The system control supports the following tasks/features:

- Managing the startup sequence
- Controlling the measurement cycle regarding to the EEPROM-stored configuration data
- Sensor signal conditioning (calculation of the 16-bit correction for each measurement signal using the EEPROM-stored conditioning coefficients and the ROM-based formulas)
- Processing communication requests received via the digital interfaces
- Performing failsafe tasks and message detected errors by setting diagnostic states

### 2.5.1. General Working Modes

ZSSC3135 supports three different working modes:

- Normal Operation Mode (NOM) – for continuous processing of signal conditioning
- Command Mode (CM) – for calibration and access to all internal registers
- Diagnostic Mode (DM) – for failure messages

### 2.5.2. Startup Phase \*

After power-on, the startup phase is processed, which includes

- Internal supply voltage settling including reset of the circuitry by the power-on reset block (POR). Refer to the ZSSC313x *High Voltage Protection Description* for power-on/off thresholds. Duration (beginning with  $V_{VDDA}-V_{VSSA}=0V$ ): 500μs to 2ms; AOUT: high impedance.

\* All timing values are roughly estimated for an oscillator frequency  $f_{osc}=3MHz$  and are proportional to that frequency.

- System start and configuration, EEPROM readout, and signature check.  
Duration: ~200 $\mu$ s; AOUT: lower diagnostic range (LDR).
- Processing the measurement cycle start routine.  
Duration: 5x A/D conversion time; AOUT behavior depends on configured one-wire communication mode (refer to section 2.6):
  - OWIANA or OWIDIS → AOUT: lower diagnostic range (LDR)
  - OWIWIN or OWIENA → AOUT: tri-state

If an error is detected during the startup phase, the Diagnostic Mode (DM) is activated and the analog output at the AOUT pin remains in the lower diagnostic range.

After the startup phase, the continuous running measurement and sensor signal conditioning cycle is started, and analog or digital output of the conditioned sensor signal is activated. If the one-wire communication mode OWIWIN is selected, the OWI startup window expires before analog output is available.

### 2.5.3. Conditioning Calculation

The digitalized value for the bridge signal is processed with a conditioning formula to remove offset and temperature dependency and to compensate nonlinearity up to 3<sup>rd</sup> order. The result is a non-negative 15-bit value for the measured bridge sensor signal in the range [0; 1). This value is available for readout via I<sup>2</sup>C™ or OWI communication. For the analog output, the value is clipped to the programmed output limits.

**Note:** The extent of signal deviation that can be compensated by the conditioning calculation depends on the specific sensor signal characteristics. For a rough estimation, assume the following: offset compensation and gain correction are not limited. Note that resolution of the digitally gained signal is determined by the ADC resolution in respect to the dynamic input range used. The temperature correction includes first and second order terms and should be adequate for practically all relevant cases. The non-linearity correction of the sensor signal is possible for second-order up to approximately 30% FS regarding ideal fit and for third-order up to about 20% FS. Overall, the conditioning formula applied is able to reduce the non-linearity of the sensor signal by a factor of 10.

## 2.6. Analog or Digital Output

The AOUT pin is used for analog output and for one-wire communication (OWI). The latter can be used for digital readout of the conditioned sensor signal and for end-of-line sensor module calibration. The ZSSC3135 supports different modes for the analog output in interaction with OWI communication as selected by EEPROM configuration or by command:

- OWIENA: Analog output is deactivated; OWI readout of the signal data is enabled.
- OWIWIN: Analog output starts after the startup phase and after the OWI startup window if OWI communication is not initiated; OWI communication for configuration or for end-of-line calibration can be started during the OWI startup window (maximum ~500ms) by sending the START\_CM command.
- OWIANA: Analog output starts after the startup phase; OWI communication for configuration or for end-of-line calibration can be started during the OWI startup window (maximum ~500ms) by sending the START\_CM command; for command transmission, the analog output driven at the AOUT pin must be overwritten by the external communication master (AOUT drive capability is current-limited).
- OWIDIS: Analog output starts after the startup phase; OWI readout of the signal data is disabled.

The analog output signal is driven by an offset compensated, rail-to-rail output buffer that is current-limited to prevent damage to the ZSSC3135 in the event of a short circuit between the analog output and power supply or ground. Output resolution of at least 12-bit in the range of 10% to 90% FS is ensured by a 12.4-bit resistor string DAC.

## 2.7. Serial Digital Interface

The ZSSC3135 includes a serial digital I<sup>2</sup>C™ interface and a ZACwire™ interface for one-wire communication (OWI). The digital interfaces allow configuration and calibration of the sensor module. OWI communication can be used to perform an end-of-line calibration via the analog output pin AOUT of a completely assembled sensor module. The interfaces also provide the readout of the conditioned sensor signal data during normal operation.

Refer to the *ZSSC313x Functional Description* for a detailed description of the serial interfaces and the communication protocols.

## 2.8. Failsafe Features

The ZSSC3135 detects various failures. When a failure is detected, Diagnostic Mode (DM) is activated. DM is indicated by setting the output pin AOUT to the Lower Diagnostic Range (LDR). When using digital serial communication protocols (I<sup>2</sup>C™ or OWI) to read conditioning results data, the error status is indicated by a specific error code.

A watchdog timer controls the proper operation of the microcontroller. The operation of the internal oscillator is monitored by an oscillator-failure detection circuit. EEPROM and RAM content are checked when accessed. Control registers are parity protected.

The sensor connection is checked with regard to broken wires or short circuits (sensor connection check, sensor short check).

The connection of an external temperature sensor can be monitored by the temperature sensor check.

Refer to the *ZSSC313x Functional Description* for a detailed description of failsafe features and methods of error indication.

## 2.9. High Voltage, Reverse Polarity, and Short Circuit Protection

The ZSSC3135 is designed for 5V power supply operation.

The ZSSC3135 and the connected sensor are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected (short circuit, overvoltage, and reverse polarity) with all potentials in the protection range under all potential conditions at the pins VDDE and VSSE.

To guarantee this operation, all external components (see application circuit in section 3) are required. The protection is not time-limited.

Refer to the *ZSSC313x High Voltage Protection Description* for a detailed description of protection cases and conditions.

### 3 Application Circuit Examples

The application circuits contain external components that are needed for overvoltage, reverse polarity, and short circuit protection.

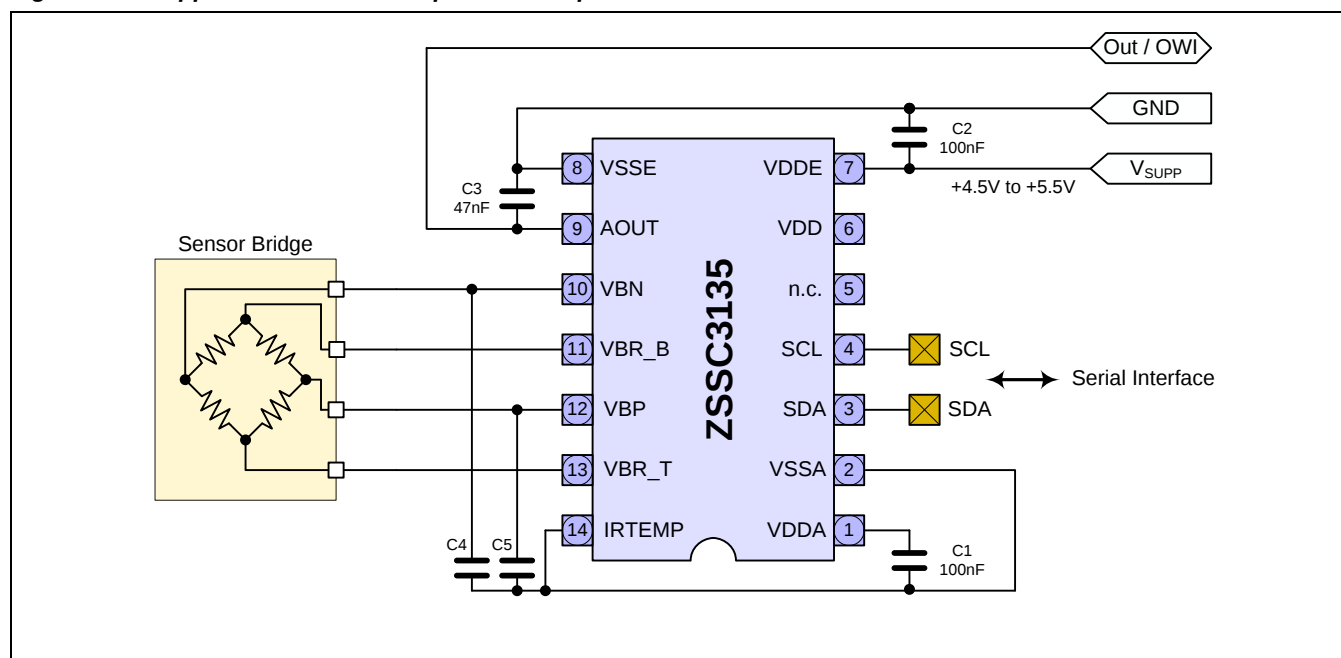
**Note:** Also refer to *ZSSC313x Technical Note—EMC Design Guidelines* and other ZSSC313x application notes available on the ZSSC3135 product web page ([www.IDT.com/zssc3135](http://www.IDT.com/zssc3135)) for additional application examples and board layout recommendations.

**Table 3.1 External Components for Application Circuit Examples**

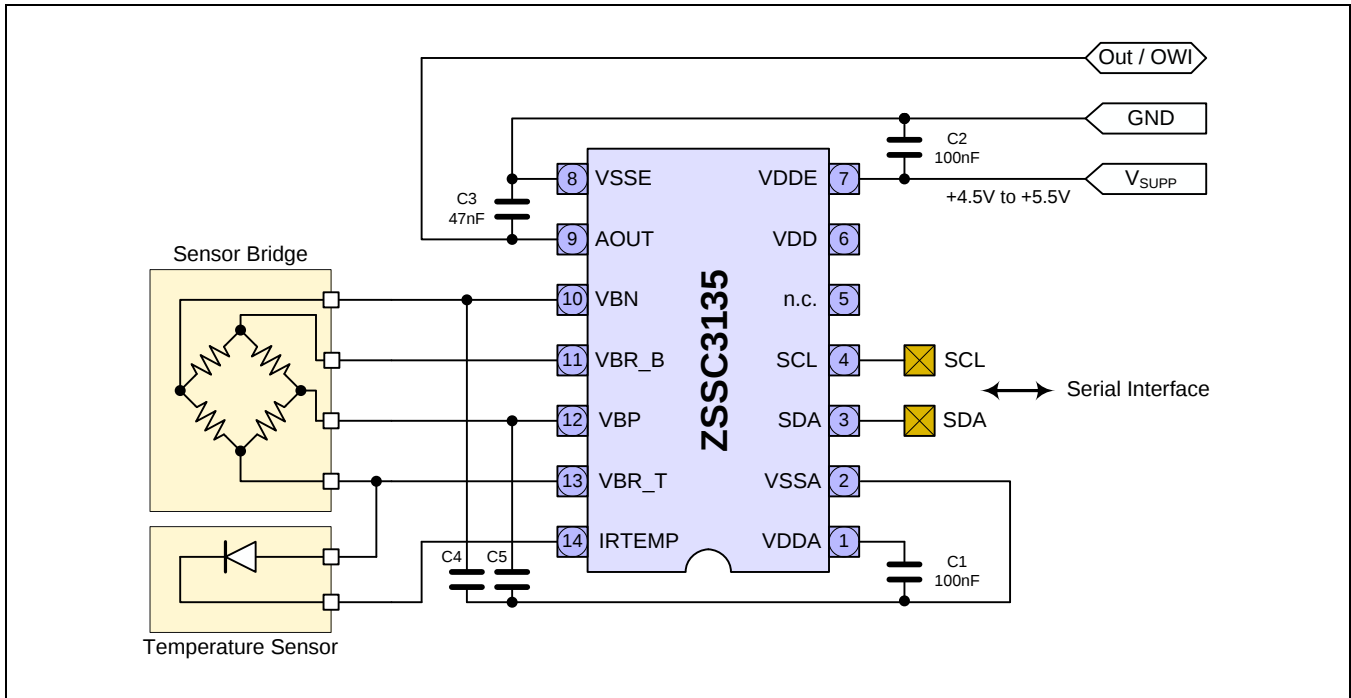
| Symbol                      | Component | Min | Typ <sup>2)</sup> | Max | Unit | Remarks                                                                                                                         |
|-----------------------------|-----------|-----|-------------------|-----|------|---------------------------------------------------------------------------------------------------------------------------------|
| <b>C1</b>                   | Capacitor | 100 |                   | 470 | nF   |                                                                                                                                 |
| <b>C2</b>                   | Capacitor | 100 |                   |     | nF   |                                                                                                                                 |
| <b>C3 <sup>1)</sup></b>     | Capacitor | 4   | 47                | 160 | nF   | Value includes the load capacitor C3 and the capacitance of the connection cable.                                               |
| <b>C4, C5 <sup>1)</sup></b> | Capacitor | 0   |                   | 10  | nF   | Recommended to increase EMI immunity. Value includes the filter capacitor C4 and C5 and the sensor connection line capacitance. |
| <b>R1</b>                   | Resistor  |     | 10                |     | kΩ   | See Figure 3.3 for location.                                                                                                    |

1) Increasing capacitors C3, C4, and C5 increases EMI immunity.  
2) Dimensioning is only for example and must be adapted to the requirements of the application.

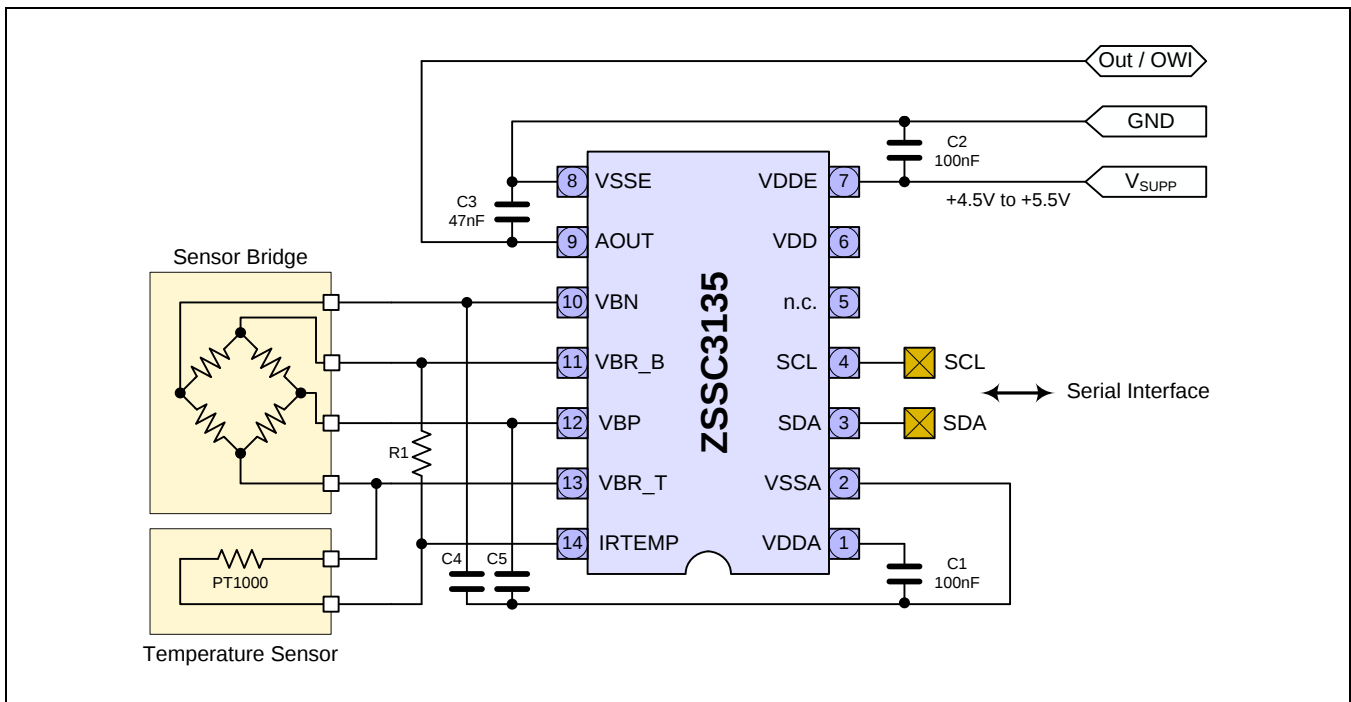
**Figure 3.1 Application with On-Chip Diode Temperature Sensor**



**Figure 3.2 Application with External Diode Temperature Sensor**



**Figure 3.3 Application with External Thermistor**



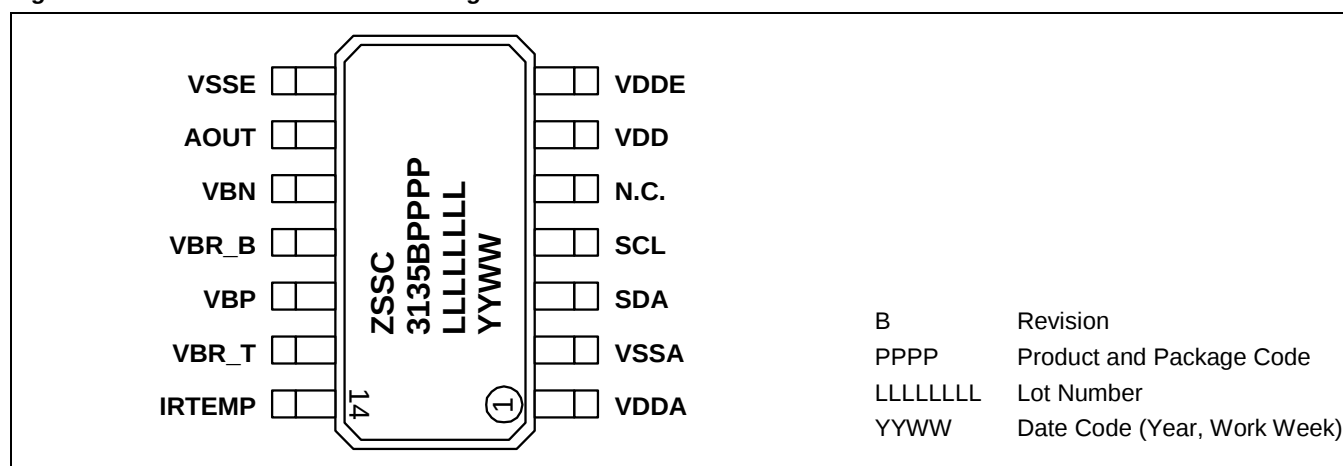
## 4 Pin Configuration and Package

**Table 4.1** Pin Configuration and Definition

| Pin No | Pin Name | Description                            | Remarks                                                       |
|--------|----------|----------------------------------------|---------------------------------------------------------------|
| 1      | VDDA     | Positive Analog Supply Voltage         | Internal analog supply                                        |
| 2      | VSSA     | Negative Analog Supply Voltage         | Internal analog ground                                        |
| 3      | SDA      | I <sup>2</sup> C™ Serial Data          | Digital I/O; internal pull-up to VDDA                         |
| 4      | SCL      | I <sup>2</sup> C™ Clock                | Digital input; internal pull-up to VDDA                       |
| 5      | N.C.     | Not connected                          |                                                               |
| 6      | VDD      | Positive Digital Supply Voltage        | Internal digital supply                                       |
| 7      | VDDE     | Positive External Supply Voltage       | High voltage analog supply                                    |
| 8      | VSSE     | Negative External Supply Voltage       | Ground                                                        |
| 9      | AOUT     | Analog Output and ZACwire™ Serial Data | High voltage analog I/O                                       |
| 10     | VBN      | Negative Input from Sensor Bridge      | Analog input                                                  |
| 11     | VBR_B    | Negative Sensor Bridge Supply Voltage  | Analog I/O<br>Depending on application circuit, short to VSSA |
| 12     | VBP      | Positive Input from Sensor Bridge      | Analog input                                                  |
| 13     | VBR_T    | Positive Sensor Bridge Supply Voltage  | Analog I/O<br>Depending on application circuit, short to VDDA |
| 14     | IRTEMP   | External Temperature Sensor            | Analog I/O                                                    |

The standard package of the ZSSC3135 is an RoHS-compliant SSOP14 “green” package (5.3mm body width) with a lead pitch of 0.65 mm.

**Figure 4.1** ZSSC3135 SSOP14 Pin Diagram



## 5 ESD Protection

All pins have an ESD protection of >2000V according to the Human Body Model (HBM). The pins VDDE, VSSE and AOUT have an additional ESD protection of >4000V (HBM).

ESD protection is tested with devices in SSOP14 packages during product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

## 6 Quality and Reliability

The ZSSC3135 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

A fit rate <5fit (T=55°C, S=60%) is guaranteed. A typical fit rate of the semiconductor technology used is 2.5fit.

## 7 Customization

For high-volume applications that require an upgraded or downgraded functionality compared to the ZSSC3135, IDT can customize the circuit design by adding or removing certain functional blocks.

Please contact IDT for further information.

## 8 Ordering Information

| Product Sales Code                    | Description                                                                                                                                                                                                          | Package                     |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| ZSSC3135BA2T                          | ZSSC3135 SSOP14 – temperature range -40 to +125°C                                                                                                                                                                    | Tube                        |
| ZSSC3135BA2R                          | ZSSC3135 SSOP14 – temperature range -40 to +125°C                                                                                                                                                                    | Reel                        |
| ZSSC3135BA1B                          | ZSSC3135 die – temperature range -40 to +125°C                                                                                                                                                                       | Tested dice on unsawn wafer |
| ZSSC3135BA1C                          | ZSSC3135 die – temperature range -40 to +125°C                                                                                                                                                                       | Tested dice on frame        |
| ZSSC3135BE2T                          | ZSSC3135 SSOP14 – temperature range -40 to +150°C                                                                                                                                                                    | Tube                        |
| ZSSC3135BE2R                          | ZSSC3135 SSOP14 – temperature range -40 to +150°C                                                                                                                                                                    | Reel                        |
| ZSSC3135BE1B                          | ZSSC3135 die – temperature range -40 to +150°C                                                                                                                                                                       | Tested dice on unsawn wafer |
| ZSSC3135BE1C                          | ZSSC3135 die – temperature range -40 to +150°C                                                                                                                                                                       | Tested dice on frame        |
| ZSSC313xKITV1.1                       | ZSSC313x Evaluation Kit, revision 1.1, including Evaluation Board, ZSSC3135 IC samples, USB cable (software can be downloaded from the product page <a href="http://www.IDT.com/ZSSC3135">www.IDT.com/ZSSC3135</a> ) | Kit                         |
| ZSSC313x Mass Calibration System V1.1 | Modular Mass Calibration System (MSC) for ZSSC313x including MCS boards, cable, connectors (software can be downloaded from the product page <a href="http://www.IDT.com/ZSSC3135">www.IDT.com/ZSSC3135</a> )        | Kit                         |

## 9 Related Documents

| Document                                                      |
|---------------------------------------------------------------|
| <i>ZSSC3135 Feature Sheet</i>                                 |
| <i>ZSSC313x Functional Description</i>                        |
| <i>ZSSC313x Evaluation Kit Description</i>                    |
| <i>ZSSC313x Technical Note—EMC Design Guidelines*</i>         |
| <i>ZSSC313x Technical Note—High Voltage Protection*</i>       |
| <i>ZSSC313x Technical Note Die &amp; Package Dimensions**</i> |
| <i>IDT Wafer Dicing Guidelines</i>                            |
| <i>ZSSC313x Temperature Profile Calculation Spread Sheet</i>  |
| <i>ZSSC313x Bandwidth Calculation Spread Sheet**</i>          |

Visit the ZSSC3135 product page ([www.IDT.com/ZSSC3135](http://www.IDT.com/ZSSC3135)) or contact your nearest sales office for the latest version of these documents.

\* Documents marked with an asterisk (\*) require a login account for access on the web.

\*\* Documents marked with a double asterisk (\*\*) are available only on request.

## 10 Glossary

| Term   | Description                                         |
|--------|-----------------------------------------------------|
| ADC    | Analog-to-Digital Converter                         |
| AEC    | Automotive Electronics Council                      |
| AFE    | Analog Front-end                                    |
| AOUT   | Analog Output                                       |
| BAMP   | Buffer Amplifier                                    |
| BR     | Bridge Sensor Signal                                |
| CM     | Command Mode                                        |
| CMC    | Calibration Microcontroller                         |
| CMOS   | Complementary Metal Oxide Semiconductor             |
| DAC    | Digital-to-Analog Converter                         |
| DM     | Diagnostic Mode                                     |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| ESD    | Electrostatic Device                                |

| Term | Description                                                           |
|------|-----------------------------------------------------------------------|
| LDR  | Lower Diagnostic Range                                                |
| MUX  | Multiplexer                                                           |
| NOM  | Normal Operation Mode                                                 |
| OWI  | One-Wire Communication                                                |
| PGA  | Programmable Gain Amplifier                                           |
| POR  | Power-on Reset                                                        |
| RAM  | Random-Access Memory                                                  |
| RISC | Reduced Instruction Set Computer                                      |
| ROM  | Read-Only Memory                                                      |
| SCC  | Sensor Connection Check                                               |
| SSC  | Sensor Signal Conditioner or Sensor Short Check depending on context. |
| T    | Temperature Sensor Signal                                             |
| TS   | Temperature Sensor                                                    |

## 11 Document Revision History

| Revision | Date               | Description                                                                                                                                                                                                                                                                          |
|----------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.00     | October 18, 2011   | First released revision.                                                                                                                                                                                                                                                             |
| 1.10     | January 20, 2012   | Full revision.                                                                                                                                                                                                                                                                       |
| 1.20     | September 25, 2012 | Minor edits. Update for IDT contact information.                                                                                                                                                                                                                                     |
| 1.21     | February 15, 2013  | Updates to specifications in section 1.3.7.<br>Addition of RS factor (ADC Range Shift) to equation (2).<br>Minor edits. Update for ZMD America contact information.                                                                                                                  |
| 1.22     | October 21, 2013   | Update for available part codes.<br>Update for contact information and imagery for cover and header.<br>Update for related documents.<br>Minor edits for clarity.                                                                                                                    |
| 1.23     | April 21, 2014     | Update to description for kits: software is no longer included in kits. It is downloaded from the product page <a href="http://www.IDT.com/ZSSC3135">www.IDT.com/ZSSC3135</a> .<br>Update for kit revision.<br>Update for cover imagery, contact information, and related documents. |
| 1.24     | April 10, 2015     | Update for contact information.                                                                                                                                                                                                                                                      |
|          | January 27, 2016   | Changed to IDT branding.                                                                                                                                                                                                                                                             |



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