

NTMFS4C05N

MOSFET – Power, Single, N-Channel, SO-8 FL 30 V, 78 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	21.7	A
		$T_A = 80^{\circ}\text{C}$		16.3	
Power Dissipation $R_{\theta JA}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	2.57	W
Continuous Drain Current $R_{\theta JA} \leq 10\text{ s}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	I_D	34.8	A
		$T_A = 80^{\circ}\text{C}$		26.0	
Power Dissipation $R_{\theta JA} \leq 10\text{ s}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	P_D	6.6	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	I_D	11.9	A
		$T_A = 80^{\circ}\text{C}$		8.9	
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	P_D	0.77	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	I_D	78	A
		$T_C = 80^{\circ}\text{C}$		58	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	P_D	33	W
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}, t_p = 10\text{ }\mu\text{s}$	I_{DM}	174	A	
Current Limited by Package		$T_A = 25^{\circ}\text{C}$	I_{Dmax}	80	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	30	A
Drain to Source dV/dt			dV/dt	7.0	V/ns
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^{\circ}\text{C}, V_{GS} = 20\text{ V}, I_L = 41\text{ A}_{pk}, L = 0.1\text{ mH}, R_{GS} = 25\text{ }\Omega$) (Note 3)			E_{AS}	84	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

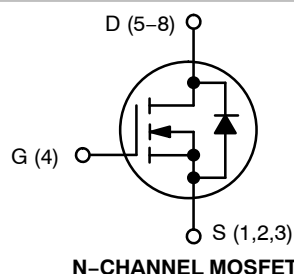
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.



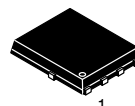
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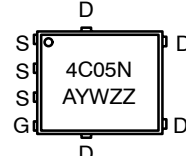
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	3.4 m Ω @ 10 V	78 A
	5.0 m Ω @ 4.5 V	



MARKING DIAGRAMS



**SO-8 FLAT LEAD
CASE 488AA
STYLE 1**



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4C05NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4C05NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFS4C05N

- Surface-mounted on FR4 board using the minimum recommended pad size.
- This is the absolute maximum ratings. Parts are 100% tested at $T_J = 25^\circ\text{C}$, $V_{GS} = 20\text{ V}$, $I_L = 29\text{ A}$, $E_{AS} = 42\text{ mJ}$.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.8	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	48.6	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	161.7	
Junction-to-Ambient – ($t \leq 10\text{ s}$) (Note 4)	$R_{\theta JA}$	19	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSS(t)}$	$V_{GS} = 0\text{ V}$, $I_{D(aval)} = 12.6\text{ A}$, $T_{case} = 25^\circ\text{C}$, $t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			12		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$		1.0 10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.3		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.1		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 30\text{ A}$		2.7 4.0	3.4 5.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}$, $I_D = 15\text{ A}$		68		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$	0.3	1.0	2.0	Ω

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$, $V_{DS} = 15\text{ V}$		1972		pF
Output Capacitance	C_{OSS}			1215		
Reverse Transfer Capacitance	C_{RSS}			59		
Capacitance Ratio	C_{RSS}/C_{ISS}	$V_{GS} = 0\text{ V}$, $V_{DS} = 15\text{ V}$, $f = 1\text{ MHz}$		0.030		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}$, $V_{DS} = 15\text{ V}$; $I_D = 30\text{ A}$		14		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.3		
Gate-to-Source Charge	Q_{GS}			6.0		
Gate-to-Drain Charge	Q_{GD}			5.0		
Gate Plateau Voltage	V_{GP}			3.1		V
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 15\text{ V}$; $I_D = 30\text{ A}$		30		nC

SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}$, $V_{DS} = 15\text{ V}$, $I_D = 15\text{ A}$, $R_G = 3.0\text{ }\Omega$		11		ns
Rise Time	t_r			32		
Turn-Off Delay Time	$t_{d(OFF)}$			21		
Fall Time	t_f			7.0		

NTMFS4C05N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.0		ns
Rise Time	t_r			26		
Turn-Off Delay Time	$t_{d(OFF)}$			26		
Fall Time	t_f			5.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.77	1.1	V
			$T_J = 125^\circ\text{C}$		0.62		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			40.2		ns
Charge Time	t_a				20.3		
Discharge Time	t_b				19.9		
Reverse Recovery Charge	Q_{RR}				30.2		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

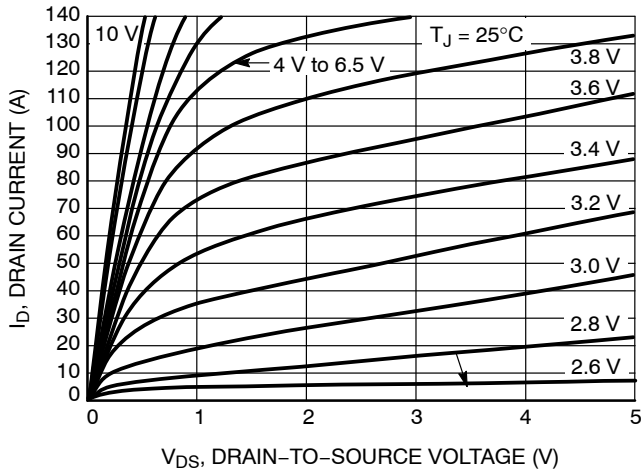


Figure 1. On-Region Characteristics

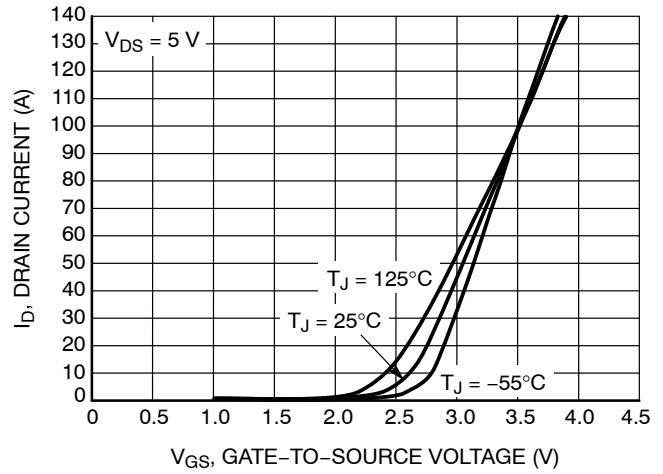


Figure 2. Transfer Characteristics

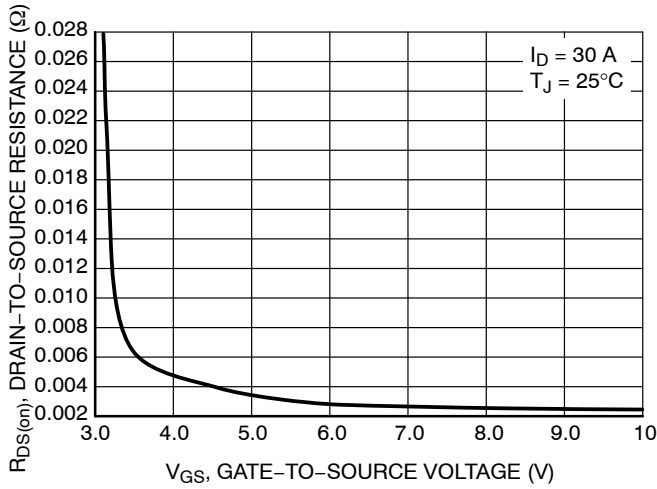


Figure 3. On-Resistance vs. V_{GS}

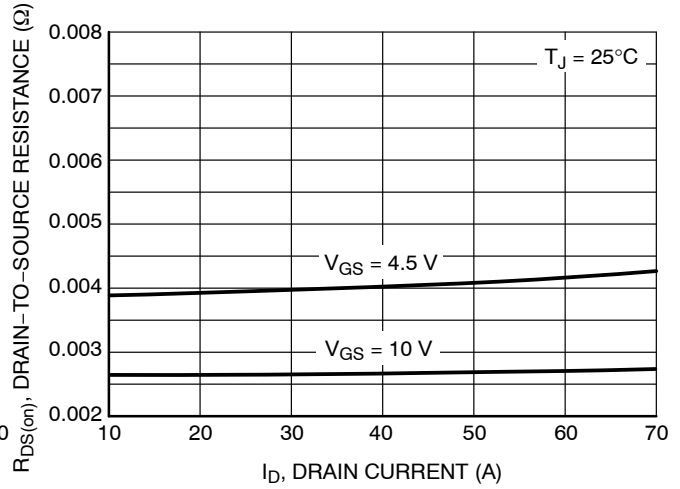


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

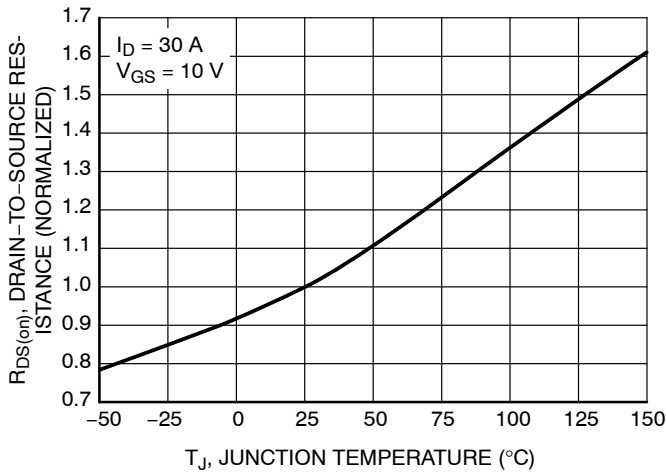


Figure 5. On-Resistance Variation with Temperature

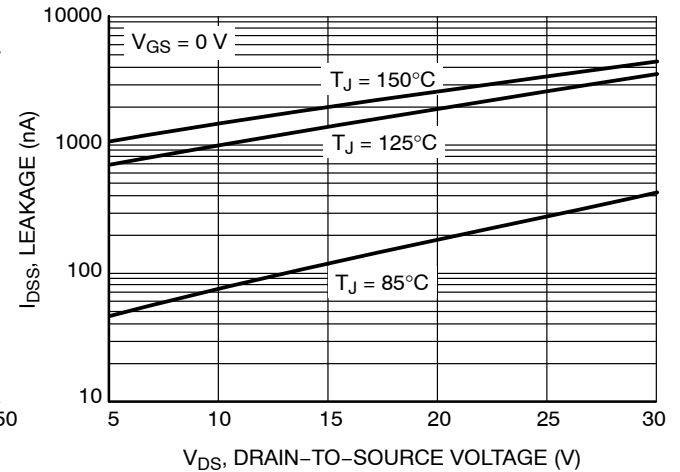


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

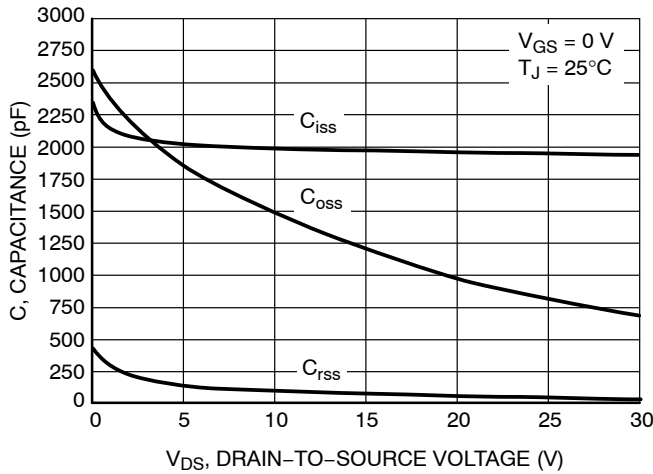


Figure 7. Capacitance Variation

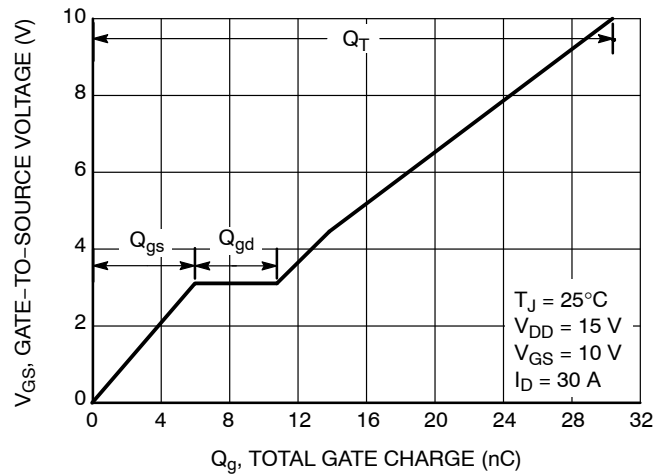


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

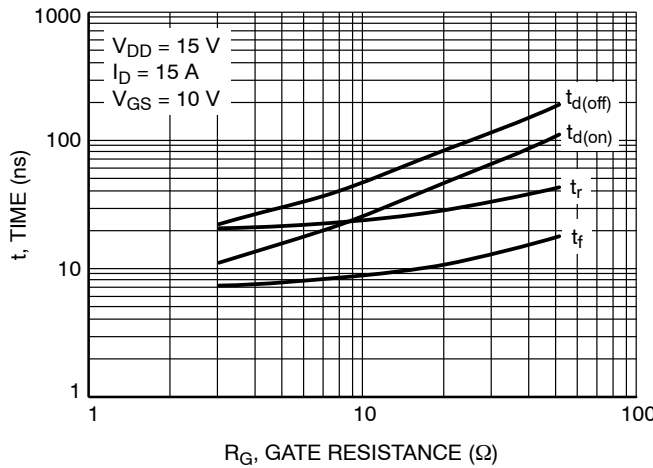


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

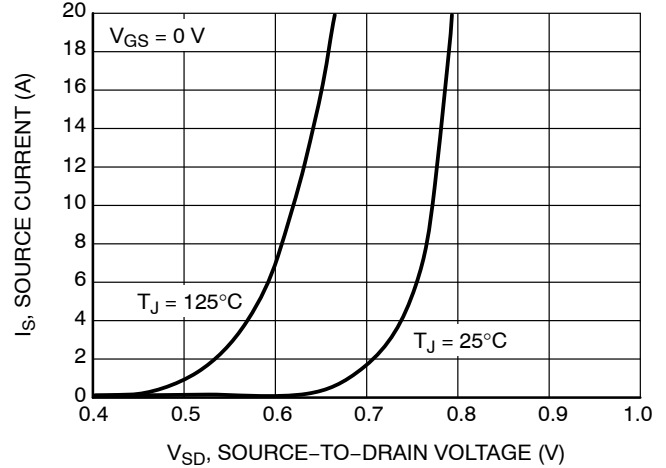


Figure 10. Diode Forward Voltage vs. Current

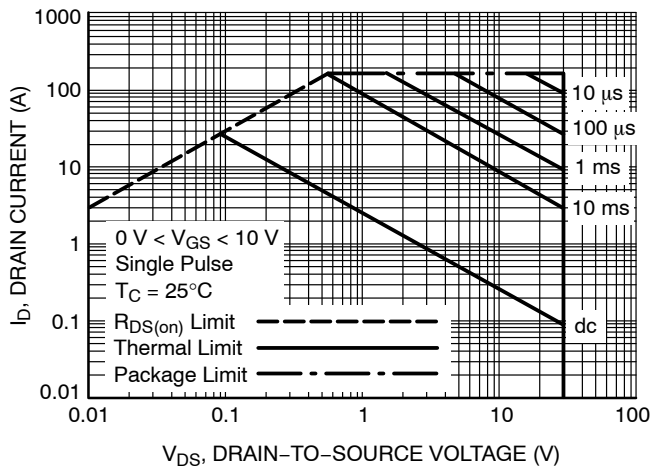


Figure 11. Maximum Rated Forward Biased Safe Operating Area

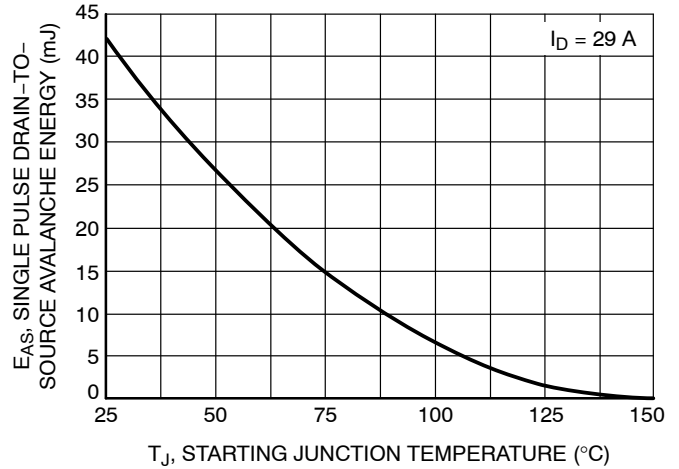


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMFS4C05N

TYPICAL CHARACTERISTICS

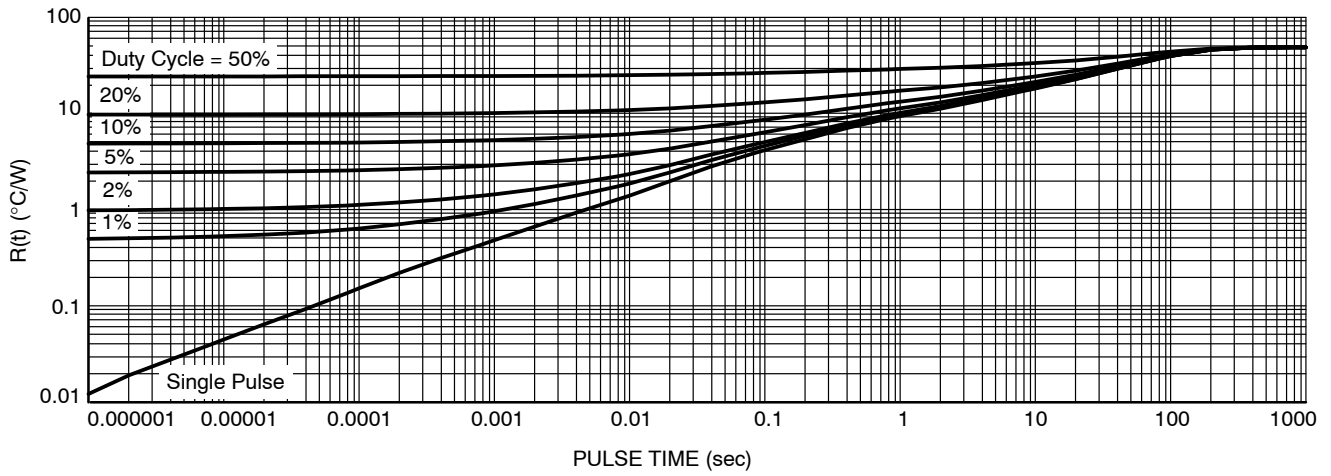


Figure 13. Thermal Response

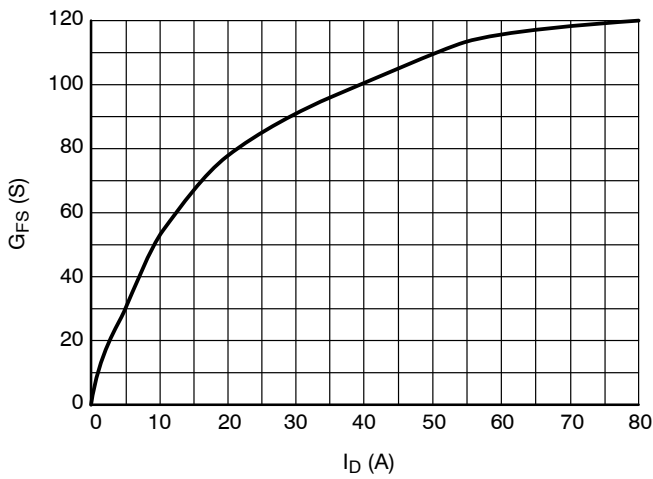


Figure 14. G_{FS} vs. I_D

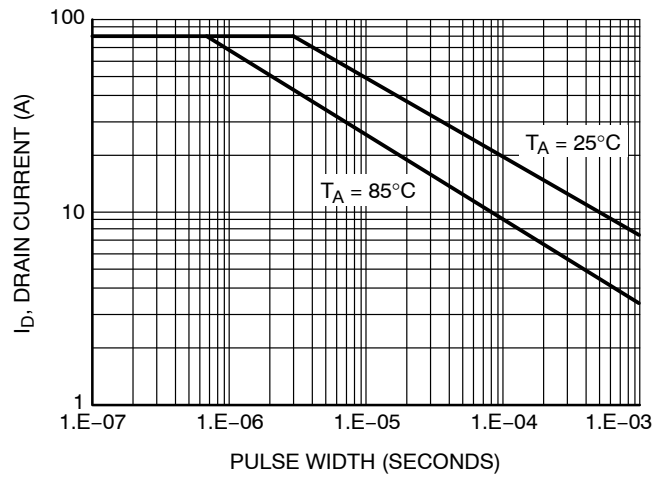
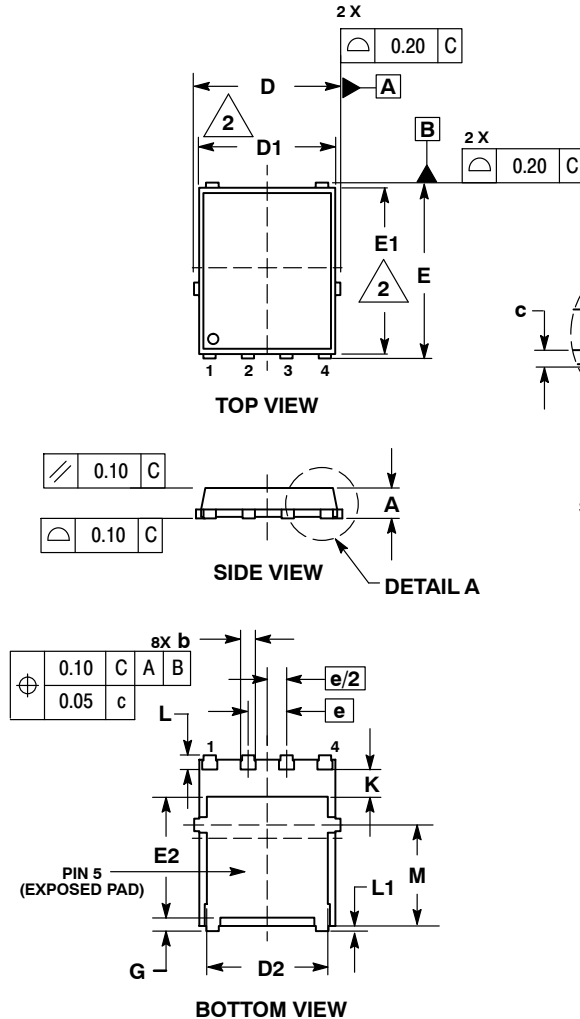


Figure 15. Avalanche Characteristics

NTMFS4C05N

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE M

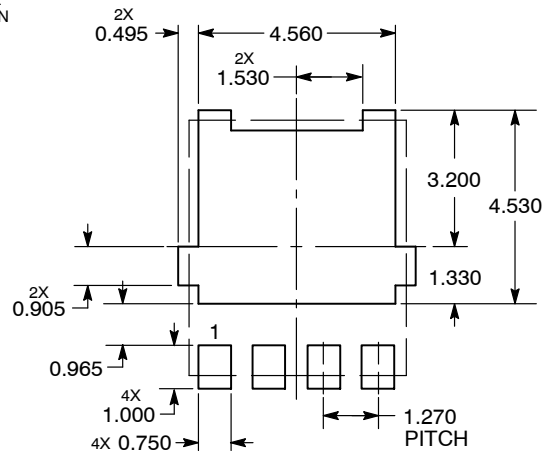


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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