## 4 X 4 Cross-Point Analog Switch with $\pm 130 \mathrm{~V}$ T/R Switches

## Features

- 16 cross-point analog echo signal matrix switches
- $\pm 130 \mathrm{~V} 20 \mathrm{~ns}$ T/R switch built-in for each channel
- $50 \Omega$ total ON resistance for low insertion loss
- $0.8 \mathrm{nV} / \mathrm{rt}$. Hz low RF input noise at 5 MHz
- DC to 100 MHz small signal bandwidth
- -55dB off-Isolation and -65dB crosstalk
- Shunt switch for LNA fast recovery
- Programmable auto trig levels and time
- $\pm 5 \mathrm{~V}$ power supply, 2.5 V to 3.3 V Logic
- 5 mA low power supply consumptions
- 20 MHz serial interface
- -55dB HD2 very low echo signal distortion


## Applications

- Medical imaging ultrasound beamforming receiver
- Software programmable echo multiplex switching
- High resolution phase array ultrasound NDT
- Ultrasonic phase array receiver focusing
- Array PZT transducer echo phase processing
- High speed T/R switch and wave-front summing


## General Description

The MD0201 is a low voltage analog $4 \times 4$ cross-point switch with four high voltage T/R switches, voltage limit diode and output shunt switch circuit. It is designed for medical ultrasound image system receiver beamforming applications. It also can be used in NDT and other ultrasound applications.

The MD0201 circuit consists of a low voltage CMOS analog switch and digital logic control serial interface circuits. These analog switches not only have low insertion loss, low noise, and wide frequency response, they also have high off isolation and low channel-to-channel crosstalk. The inputs of the analog switches are connected to the output of the two terminal type of ultrasound T/R switches, and two back-to-back diode voltage limiter circuits.

The buffered serial interface data registers have allowed the IC maximum flexibility to connect large number of channels to form the echo multiplexing, dynamic-focusing circuit for ultrasound image receive beamforming.


Ordering Information

| Part Number | Package Options | Packing |
| :--- | :--- | :--- |
| MD0201K6-G | 48-Lead (7x7) QFN | $260 /$ Tray |
| MD0201K6-G M933 | 48-Lead (7x7) QFN | $2000 /$ Reel |

-G denotes a lead (Pb)-free / RoHS compliant package

## Absolute Maximum Ratings

| Parameter | Value |
| :--- | ---: |
| GND reference voltage | 0 V |
| X0 $\sim 3$ input pins to GND voltage | 0 to $\pm 140 \mathrm{~V}$ |
| $\mathrm{~V}_{\mathrm{DD}}$ positive supply | -0.5 V to +6.0 V |
| $\mathrm{~V}_{\mathrm{SS}}$ negative supply | +0.5 V to -6.0 V |
| $\mathrm{~V}_{\mathrm{LL}}$ logic supply | -0.5 V to +4.2 V |
| All logic input pins | -0.5 V to +6.0 V |
| Maximum junction temperature | $+125^{\circ} \mathrm{C}$ |
| Storage temperature range | $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Typical Thermal Resistance

| Package | $\theta_{j a}$ |
| :--- | :--- |
| 48-Lead QFN | $18^{\circ} \mathrm{C} / \mathrm{W}$ |



ESD Sensitive Device

## Pin Configuration



## Product Marking

| MD0201K6 | L = Lot Number |
| :--- | :--- | :--- |
| LLLLLLLLL | WW Y Wear Sealed |
| YYWW | A = Assembler ID |
| AAA CCC | C = Country of Origin |
|  |  |

48-Lead QFN
Package may or may not include the following marks: Si or

Operating Supply Voltages (Over operating conditions unless othemise specified, $\left.V_{u}=3.3 v, V_{o 0}=+5 V_{,} T_{j}=25^{\circ} \mathrm{C}\right)$

| Sym | Parameter | Min | Typ | Max | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{D D}$ | Voltage power supply | 4.75 | 5.0 | 5.25 | V | $\mathrm{T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{ss}}$ | Voltage power supply | -5.25 | -5.0 | -4.75 |  |  |
| $\mathrm{V}_{\mathrm{LL}}$ | Voltage power supply | 2.3 | 3.3 | 3.6 |  |  |
| $\mathrm{V}_{\text {SIG }}$ | Signal input range (p-p) | - | $\pm 500$ | - | mV | 5 MHz sine wave, no clipping |
| $\mathrm{R}_{\text {ON }}$ | Cross-point switch ON resistance | - | 50 | 60 | $\Omega$ | $\mathrm{I}_{\mathrm{x}}= \pm 5.0 \mathrm{~mA}, \mathrm{~V}_{\text {x0-3 }}= \pm 300 \mathrm{mV}$ |
| $\Delta \mathrm{R}_{\text {ON }}$ | Ch to Ch $\mathrm{R}_{\text {ON }}$ difference | - | $\pm 5$ | - | \% | Switches ON resistance match within IC. |
| $V_{\text {F }}$ | Diode forward voltage | - | 0.8 | 1.0 | V | 1 mA |
| $\mathrm{C}_{\text {T }}$ | Diode total capacitance | - | - | 15 | pF | $V_{R}=0 \mathrm{~V}, \mathrm{f}=1 \mathrm{MHz}$ |
| $\mathrm{I}_{\text {FM }}$ | Diode forward continuous current | - | 100 | - | mA | on $4 \times 4$ inch $\mathrm{PCB}, \mathrm{V}_{\mathrm{F}}=1.2 \mathrm{~V}$ |
| $I_{\text {DDQ }}$ | $\mathrm{V}_{\mathrm{DD}}$ supply current 0 MHz | - | 2.2 | 3.0 | mA | SDI $=$ SCK $=0, \mathrm{CS}=0$ |
| $\mathrm{I}_{\text {DD30 }}$ | $\mathrm{V}_{\text {DD }}$ supply current 30 MHz | - | 7.0 | 30 | mA | $\mathrm{f}_{\text {sck }}=30 \mathrm{MHz}, \mathrm{SDI}=\mathrm{CS}=0$ |
| HD2 | Second harmonic distortion | - | -55 | -50 | dB | $5 \mathrm{MHz} \pm 300 \mathrm{mVp}$-p sine wave |

T/R Switch Characteristics (Over operating oonditions unness otherwise specified, $V_{U}=3.35, V_{D 0}=+5 V, T_{j}=25^{\circ}$ ),

| Sym | Parameter | Min | Typ | Max | Unit | Conditions |
| :---: | :--- | :---: | :---: | :---: | :---: | :--- |
| $\mathrm{V}_{\mathrm{x}}$ | Max $\mathrm{X}_{0-3}$ to GND input voltage | $\pm 130$ | - | - | V | $\mathrm{I}_{\mathrm{x}}= \pm 500 \mu \mathrm{~A}$ |
| $\mathrm{R}_{\text {TRSW }}$ | $\mathrm{T} / \mathrm{R}$ switch ON resistance | - | 15 | - | $\Omega$ | $\mathrm{I}_{\mathrm{x}}= \pm 5.0 \mathrm{~mA}$ |
| $\mathrm{~V}_{\text {TRIP }}$ | $\mathrm{V} \mathrm{X}_{0-3}$ trip point to turn off | - | $\pm 1.0$ | $\pm 2.0$ | V | --- |
| $\mathrm{V}_{\text {OFF }}$ | Switch turn off voltage | - | $\pm 2.0$ | - | V | $\mathrm{I}_{\mathrm{A}-\mathrm{B}}= \pm 1.0 \mathrm{~mA}$ |
| $\mathrm{I}_{\text {OFF }}$ | Switch off current | - | $\pm 200$ | $\pm 300$ | $\mu \mathrm{~A}$ | $\mathrm{X}_{\mathrm{n}}= \pm 100 \mathrm{~V}$ |
| $\mathrm{I}_{\text {PEAK }}$ | Peak T/R switch current | - | $\pm 60$ | - | mA | --- |
| $\mathrm{T}_{\text {OFF }}$ | Turn off time | - | - | 20 | ns | --- |
| $\mathrm{T}_{\text {ON }}$ | Turn on time | - | - | 20 | ns | --- |
| $\mathrm{C}_{\text {SW(ON) }}$ | Switch on capacitance | - | 21 | - | pF | $\mathrm{T} / \mathrm{R} \mathrm{SW}=\mathrm{ON}$ |
| $\mathrm{C}_{\text {Sw(OFF) }}$ | Switch off capacitance | - | 15 | - | pF | $\mathrm{X}_{\mathrm{n}}= \pm 25 \mathrm{~V}$ |

Clock and Logic I/O Characteristics (Over operating conditions unness othemise specified, $\left.V_{L}=3.3, V^{2}=+5 V, T_{=}=25^{\circ} \mathrm{C}\right)$

| $\mathrm{V}_{\mathrm{IH}}$ | Input logic high voltage | 2.5 | 3.3 | 5.0 | V | --- |
| :---: | :--- | :---: | :---: | :---: | :---: | :--- |
| $\mathrm{V}_{\mathrm{IL}}$ | Input logic low voltage | 0 | - | 0.6 | V | --- |
| $\mathrm{I}_{\mathrm{IH}}$ | Input logic high current | - | 0.4 | 1.0 | $\mu \mathrm{~A}$ | --- |
| $\mathrm{I}_{\mathrm{LL}}$ | Input logic low current | -1.0 | - | - | $\mu \mathrm{A}$ | --- |
| $\mathrm{C}_{\mathrm{IN}}$ | Input capacitance | - | 2.0 | 5.0 | pF | --- |
| $\mathrm{I}_{\mathrm{OH}}$ | $\mathrm{V}_{\text {DOUT }}$ sourcing current | 4.0 | - | - | mA | $\mathrm{V}_{\mathrm{LL}}=2.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{DOUT}}=0$ |
| $\mathrm{I}_{\mathrm{OL}}$ | $\mathrm{V}_{\text {DOUT }}$ sinking current | 4.0 | - | - | mA | $\mathrm{V}_{\mathrm{LL}}=\mathrm{V}_{\mathrm{DOUT}}=2.3 \mathrm{~V}$ |
| $\mathrm{~V}_{\mathrm{OH}}$ | Output logic high voltage | - | 1.59 | - | V | $\mathrm{I}_{\mathrm{OH}}=-2.0 \mathrm{~mA}$ |
| $\mathrm{~V}_{\mathrm{OL}}$ | Output logic low voltage | - | 0.67 | - | V | $\mathrm{I}_{\mathrm{OL}}=-2.0 \mathrm{~mA}$ |

AC Electrical Characteristics (Over operating oonditions untess othememse specified, $V_{U}=3.3, V_{V 0}=+5 V, T=25^{\circ}$ )

| $\mathrm{t}_{\text {d(on) }}$ | LV SW turn on time | - | 20 | 30 | ns | --- |
| :---: | :--- | :---: | :---: | :---: | :---: | :--- |
| $\mathrm{t}_{\text {d(off) }}$ | LV SW turn off time | - | 20 | 30 | ns | --- |
| $\mathrm{t}_{\text {co(on) }}$ | Output shunt switch on time | - | 40 | 50 | ns | $\mathrm{~V}_{\mathrm{x}}=5.0 \mathrm{~V}$ |
| $\mathrm{t}_{\text {co(off) }}$ | Output shunt switch off-delay | 1.0 | 2.0 | 3.0 | $\mu \mathrm{~s}$ |  |
| $\mathrm{~V}_{\text {STG }}$ | Shunt on-short trig voltage level | - | $\pm 0.8$ | - | V | --- |
| BW | Small signal bandwidth with T/R SW | - | 85 | - | MHz | $\mathrm{R}_{\text {LOAD }}=50 \Omega$ |
| $\mathrm{Q}_{\mathrm{C}}$ | LV SW charge injection | - | 2.6 | 3.5 | pC | $\mathrm{V}_{\mathrm{s}}=1.0 \mathrm{~V}, \mathrm{R}_{\mathrm{s}}=0 \Omega, \mathrm{C}_{\text {LOAD }}=100 \mathrm{pF}$ |
| $\mathrm{K}_{\mathrm{o}}$ | OFF isolation | - | -65 | - | dB | at $10 \mathrm{MHz}, \mathrm{R}_{\text {LOAD }}=50 \Omega$ |
| $\mathrm{~K}_{\text {CR }}$ | On channel crosstalk | - | -55 | - |  |  |
| $\mathrm{C}_{\text {(ON) }}$ | On capacitance output to RGND | - | 37 | - | pF | from OA~OD to RGND |
| $\mathrm{C}_{\text {(OFF) }}$ | Off capacitance output to RGND | - | 23 | - |  |  |
| $\mathrm{f}_{\mathrm{CLK}}$ | Serial clock frequency | - | 25 | - | MHz | --- |

AC Electrical Characteristics (cont.) (Over operating conditions uness othemise specified, $V_{U}=3.3, V_{V 0}=+5 V, T_{F}=25^{\circ}$ ),

| Sym | Parameter | Min | Typ | Max | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {sD }}$ | Setup time before LE rises | - | 10 | - | ns | At 25 MHz <br> $\mathrm{V}_{\mathrm{DD}}=4.75 \mathrm{~V}$ <br> $\mathrm{V}_{\mathrm{LL}}=2.5 \mathrm{~V}$ |
| $\mathrm{t}_{\text {wLE }}$ | Time width of LE | - | 20 | - |  |  |
| $\mathrm{t}_{\mathrm{DO}}$ | CLK delay time to data out | - | 13 | - |  |  |
| $\mathrm{t}_{\text {WCLR }}$ | Time width of CLR | 55 | 15 | - |  |  |
| $\mathrm{t}_{\text {su }}$ | Set up time data to clock | - | 5.0 | - |  |  |
| $t_{n}$ | Hold time data from clock | - | 5.0 | - |  |  |
| $\mathrm{t}_{\mathrm{ff}}$ | CLK rise and fall time | 1.5 | - | - |  |  |
| $\mathrm{V}_{\text {SPK }}$ | Spike of shunt switching on | - | 60 | 100 | mV | All cross-point switches off, $50 \Omega$ on O0~3 to GND 1 k on $\mathrm{XO} \sim 3$ to GND |
|  | Spike of shunt switching off | - | 10 | - |  |  |

## 20-bit Control Shift Registers

| MSB | Data Bits in the Register |  |  |  |  |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| D19 | D19 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | ... | D1 | D0 |
| Unused | TMR | SSTE | FASN | SWAO | SWB0 | SWCO | SWDO | SWA1 | ... | SWC3 | SWD3 |
| SW[D3:A0] |  |  | 0 | LV switches off* |  |  | Low voltage analog cross-point switch on/off control data. Each data bit controls each channel LV switch independently. |  |  |  |  |
|  |  |  | 1 | LV switches on |  |  |  |  |  |  |  |
| TMR |  |  | 0 | Set on-time to 1.0us* |  |  | The shunt switches controlled by a re-trigable one-short timer. TMR sets the one short on-time for all channels. |  |  |  |  |
|  |  |  | 1 | Set on-time to 2.0 us |  |  |  |  |  |  |  |
| SSTE |  |  | 0 | Shunt switch trig Disabled* |  |  | SSTE $=0$ trig disabled |  |  |  |  |
|  |  |  | 1 | Shunt switch trig Enabled |  |  |  |  |  |  |  |
| FASN |  |  | 0 | Normal trig * |  |  | FASN $=0$ trig causing shunt switch on for a period of TMR defined time. |  |  |  |  |
|  |  |  | 1 | Force all shunt switch on |  |  |  |  |  |  |  |

## Notes:

1. $\mathrm{D}[15: 0]$ are the cross-point switch $\mathrm{SW}[\mathrm{D} 3: A 0]$ control data bits.
2. Shift in MSB first.
3. D19 is reserved.
4. The * denotes power-on defaults status.

## Logic Timing Waveforms



## T/R Switch Typical I-V Curve



Pin Description (48-Lead QFN)

| Pin | Name | Description |
| :---: | :---: | :---: |
| 1 | NC | Not connected internally to the IC |
| 2 | X0 | T/R switch channel 0 high voltage input |
| 3 | NC | Not connected internally to the IC |
| 4 | NC | Not connected internally to the IC |
| 5 | X1 | T/R switch channel 1 high voltage input |
| 6 | NC | Not connected internally to the IC |
| 7 | NC | Not connected internally to the IC |
| 8 | X2 | T/R switch channel 2 high voltage input |
| 9 | NC | Not connected internally to the IC |
| 10 | NC | Not connected internally to the IC |
| 11 | X3 | T/R switch channel 3 high voltage input |
| 12 | NC | Not connected internally to the IC |
| 13 | NC | Not connected internally to the IC |
| 14 | NC | Not connected internally to the IC |
| 15 | NC | Not connected internally to the IC |
| 16 | NC | Not connected internally to the IC |
| 17 | NC | Not connected internally to the IC |
| 18 | RGND | RF ground, diodes and shunt switch return ground (0V) |
| 19 | OA | Low voltage analog switch channel 0 output |
| 20 | OB | Low voltage analog switch channel 1 output |
| 21 | OC | Low voltage analog switch channel 2 output |
| 22 | OD | Low voltage analog switch channel 3 output |
| 23 | NC | Not connected internally to the IC |
| 24 | NC | Not connected internally to the IC |
| 25 | NC | Not connected internally to the IC |
| 26 | NC | Not connected internally to the IC |
| 27 | NC | Not connected internally to the IC |
| 28 | NC | Not connected internally to the IC |
| 29 | NC | Not connected internally to the IC |
| 30 | NC | Not connected internally to the IC |
| 31 | NC | Not connected internally to the IC |
| 32 | NC | Not connected internally to the IC |
| 33 | NC | Not connected internally to the IC |
| 34 | VSS | Negative voltage power supply -5V |

Pin Description (48-Lead QFN)

| Pin | Name | Description |
| :---: | :---: | :--- |
| 35 | DGND | Digital control signal ground and VDD return ground (OV) |
| 36 | VDD | Positive voltage power supply +5V |
| 37 | DGND | Digital control signal ground and VDD return ground (OV) |
| 38 | VDD | Positive voltage power supply +5V |
| 39 | VLL | Logic supply voltage +2.5 to 3.3V |
| 40 | DIN | Serial data input |
| 41 | CLR | Data registers clear to all switches off, active high |
| 42 | CLK | Serial interface clock input |
| 43 | LE | Data registers latch enable, active on rising edge only |
| 44 | DOUT | Serial data output |
| 45 | NC | Not connected internally to the IC |
| 46 | NC | Not connected internally to the IC |
| 47 | NC | Not connected internally to the IC |
| 48 | NC | Not connected internally to the IC |

Note: Thermal pad of the IC package (RGND) must be connected to the RF ground on the PCB.

## 48-Lead QFN Package Outline (K6)

## $7.00 \times 7.00 \mathrm{~mm}$ body, 1.00 mm height (max), 0.50 mm pitch



Top View



## Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15 mm pullback $(L 1)$ may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol |  | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dimension (mm) | MIN | 0.80 | 0.00 | $\begin{aligned} & 0.20 \\ & \text { REF } \end{aligned}$ | 0.18 | 6.85* | 1.25 | 6.85* | 1.25 | $\begin{aligned} & 0.50 \\ & \text { BSC } \end{aligned}$ | $0.30{ }^{+}$ | 0.00 | $0^{\circ}$ |
|  | NOM | 0.90 | 0.02 |  | 0.25 | 7.00 | - | 7.00 | - |  | $0.40{ }^{+}$ | - | - |
|  | MAX | 1.00 | 0.05 |  | 0.30 | 7.15* | 5.45 | 7.15* | 5.45 |  | $0.50{ }^{+}$ | 0.15 | $14^{\circ}$ |

[^0](The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http:///www.supertex.com/packaging.html.)

[^1]
[^0]:    JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.

    * This dimension is not specified in the JEDEC drawing.
    $\dagger$ This dimension differs from the JEDEC drawing.
    Drawings are not to scale.
    Supertex Doc.\#: DSPD-48QFNK67X7P050, Version C041009.

[^1]:    Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. (website: http//www.supertex.com)

