

Audio/USB 2.0 Wired-OR Switch with Click and Pop Reduction

ISL54409, ISL54410

The Intersil ISL54409 and ISL54410 are Dual SPST (Single Pole/Single Throw) switches that provide a very low distortion audio path for a stereo headphone and can be connected in a wired-OR configuration at the switch outputs with USB2.0 HS signals for Audio/USB signal multiplexing to a common connector. The audio switch path can be disabled to provide high signal isolation, preventing crosstalk between the audio codec and USB data signals.

The ISL54409 and ISL54410 analog switches are negative swing capable with a single supply voltage and maintain excellent THD performance within a signal range of -1V to +1V. The switch terminals have low pin capacitance (4pF typical), minimizing impact to USB 2.0 High-Speed signals. The ISL54409 offers a Low Power Shutdown mode while the ISL54410 offers a High Off-Isolation mode. The ISL54410 contains active Audio Click and Pop Elimination circuitry for AC-coupled audio signals.

The ISL54409 and ISL54410 are available in a 8 Ld TDFN (2mmx2mm) or a 10 Ld μ TQFN (1.8mmx1.4mm) package. They operate over a temperature range of -40 to +85°C.

Features

- Single Supply Operation (V_{DD}) . . . +2.7V to +5.0V
- Negative Signal Handling (See "Audio/USB wired-OR Application" on page 8 on protecting USB controller)
- Low OFF Capacitance for HS USB 4pF
- Power Off Protection
- THD+N at 1mW into 32 Ω Load <0.02%
- Audio Muting >110dB
- Low Power Consumption. 21 μ W with 3V supply
- Low Power Shutdown Mode (ISL54409)
- Active Click and Pop Elimination Circuitry (ISL54410)
- USB V_{BUS} Hot Plug Operation
- Available in 8 Ld TDFN (2mmx2mm) or 10 Ld μ TQFN (1.8mmx1.4mm) Package

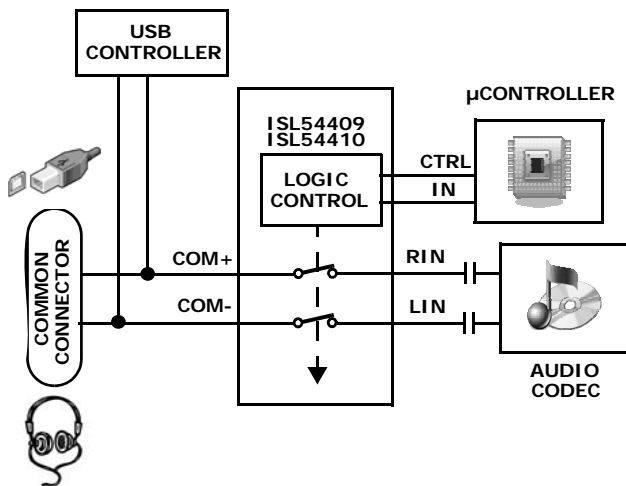
Applications* (see page 11)

- Consumer Entertainment Systems
- MP3 and other Personal Media Players
- Cellular/Mobile Phones and PDAs

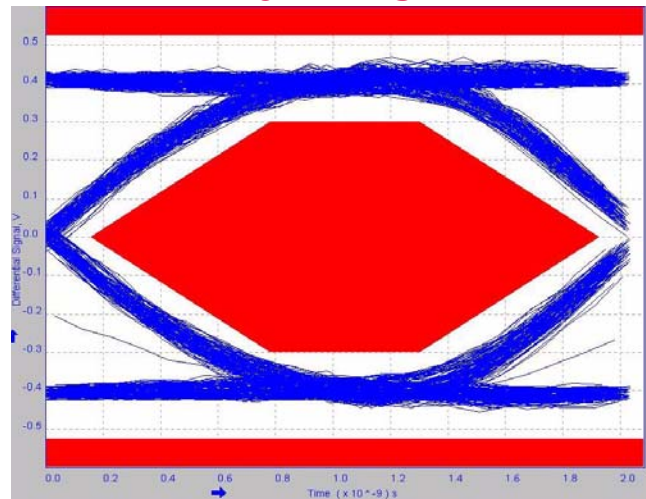
Related Literature* (see page 11)

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Typical Application



USB2.0 HS Eye Diagram



Application Block Diagrams

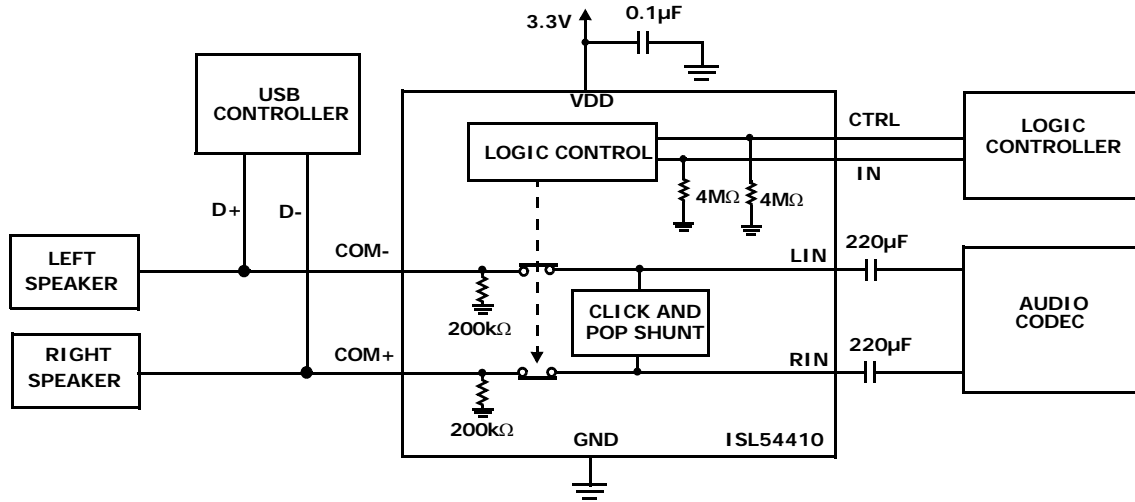
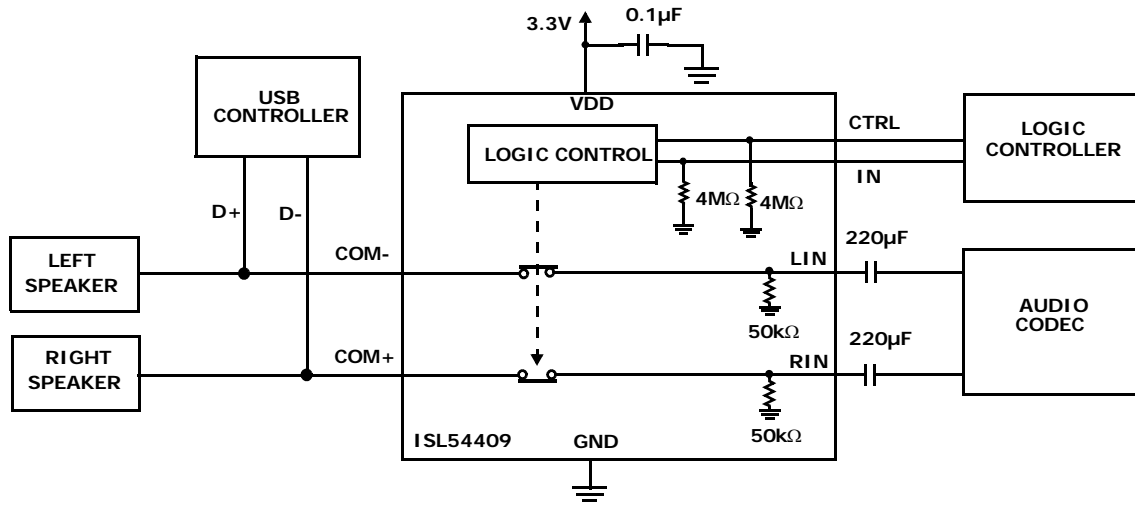
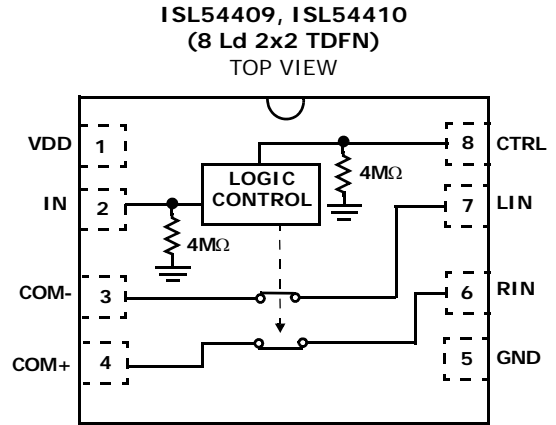
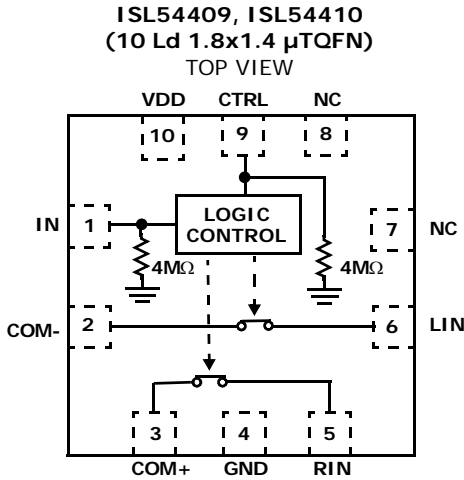


TABLE 1. ISL54409, ISL54410 FEATURES

| PART NUMBER | ANALOG SIGNAL RANGE | PACKAGE | LOW POWER MODE | CLICK AND POP ELIMINATION | V _{BUS} HOT PLUG OPERATION |
|-------------|---------------------|------------------------|----------------|---------------------------|-------------------------------------|
| ISL54409 | -1 TO +1V | 8 Ld TDFN, 10 Ld µTQFN | Yes | No | Yes |
| ISL54410 | -1 TO +1V | 8 Ld TDFN, 10 Ld µTQFN | No | Yes | Yes |

Pin Configurations (Note 1)



NOTE:

1. Switches shown with IN = 0 and CTRL = 1.

Pin Descriptions

| ISL54409 and ISL54410 | | | |
|-----------------------|------------|------|---|
| TDFN | μ TQFN | NAME | FUNCTION |
| 1 | 10 | VDD | Power Supply |
| 2 | 1 | IN | Logic Control; Internal 4M Ω pull down |
| 3 | 2 | COM- | Audio Left Output |
| 4 | 3 | COM+ | Audio Right Output |
| 5 | 4 | GND | IC Ground Connection |
| 6 | 5 | RIN | Audio Right Input |
| 7 | 6 | LIN | Audio Left Input |
| - | 7 | NC | Not Connected |
| - | 8 | NC | Not Connected |
| 8 | 9 | CTRL | Logic Control; Internal 4M Ω pull-down |
| PD | - | Pad | Thermal Pad; Connect to GND Plane |

Truth Tables

| ISL54409 | | | |
|----------|------|-----------|-----------|
| IN | CTRL | COM-/COM+ | MODE |
| 0 | 0 | OFF | Low Power |
| 0 | 1 | ON | Audio |
| 1 | X | OFF | Mute |

CTRL and IN: Logic "0" when $\leq 0.5V$, Logic "1" when $\geq 1.4V$

| ISL54410 | | | |
|----------|------|-----------|---------------|
| IN | CTRL | COM-/COM+ | MODE |
| 0 | 0 | OFF | Click and Pop |
| 0 | 1 | ON | Audio |
| 1 | X | OFF | Mute |

CTRL and IN: Logic "0" when $\leq 0.5V$, Logic "1" when $\geq 1.4V$

Ordering Information

| PART NUMBER (Note 2) | PART MARKING | TEMP. RANGE (°C) | PACKAGE Tape & Reel (Pb-Free) | PKG. DWG. # |
|-------------------------|------------------|---------------------|-------------------------------------|----------------|
| ISL54409IRTZ-T (Note 3) | 409 | -40 to +85 | 8 Ld 2x2 TDFN | L8.2x2C |
| ISL54409IRUZ-T (Note 4) | U2 | -40 to +85 | 10 Ld 1.8x1.4 μ TQFN | L10.1.8x1.4A |
| ISL54410IRTZ-T (Note 3) | 410 | -40 to +85 | 8 Ld 2x2 TDFN | L8.2x2C |
| ISL54410IRUZ-T (Note 4) | U3 | -40 to +85 | 10 Ld 1.8x1.4 μ TQFN | L10.1.8x1.4A |
| ISL54409EVAL1Z | Evaluation Board | | | |

NOTES:

- Please refer to [TB347](#) for details on reel specifications.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for [ISL54409](#), [ISL54410](#). For more information on MSL please see techbrief [TB363](#).

ISL54409, ISL54410

Absolute Maximum Ratings

| | |
|-----------------------------------|--------------------------------------|
| VDD to GND | -0.3V to 5.5V |
| Input Voltages | |
| LIN, RIN (Note 6) | -2V to ((V _{DD}) + 0.3V) |
| IN, CTRL (Note 6) | -0.3V to ((V _{DD}) + 0.3V) |
| Output Voltages | |
| COM-, COM+ (Note 6) | -2V to ((V _{DD}) + 0.3V) |
| Continuous Current (LIN, RIN) | ±150mA |
| Peak Current (LIN, RIN) | |
| (Pulsed 1ms, 10% Duty Cycle, Max) | ±300mA |
| ESD Ratings: | |
| Human Body Model | |
| ISL54409 | 3.5kV |
| ISL54410 | 6kV |
| Machine Model | |
| ISL54409 | 250V |
| ISL54410 | 300V |
| Charged Device Model | 2kV |

Thermal Information

| | | |
|--|---|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 1.8x1.4mm μ TQFN (Notes 7, 8) | 160 | 61.9 |
| 2mmx2mm TDFN (Notes 7, 8) | 84 | 10 |
| Maximum Junction Temperature (Plastic Package) | +150°C | |
| Storage Temperature Range | -65°C to +150°C | |
| Pb-Free Reflow Profile | see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp | |

Recommended Operating Conditions

| | |
|-------------|----------------|
| Temperature | -40°C to +85°C |
|-------------|----------------|

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- Signals on LIN, RIN, COM-, COM+, IN and CTRL exceeding VDD or GND by specified amount are clamped. Limit current to maximum current ratings.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{CTRL} = 1.4V, V_{IN} = 0.5V, (Notes 9, 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 10, 11) | TYP | MAX (Notes 10, 11) | UNITS |
|--|---|-----------|--------------------|-----|--------------------|------------|
| ANALOG SWITCH CHARACTERISTICS | | | | | | |
| Analog Input Signal Range, V _{ANALOG} | V _{DD} = 3.3V | Full | -1.5 | - | 1.5 | V |
| ON-Resistance, r _{ON} | I _{XOUT} = 40mA, V _{LIN} or V _{RIN} = -0.85V to 0.85V, (See Figure 2, Note 14) | +25 | - | 2.5 | 2.8 | Ω |
| | | Full | - | - | 3.8 | Ω |
| r _{ON} Flatness, r _{FLAT(ON)} | I _{XOUT} = 40mA, V _{LIN} or V _{RIN} = -0.85V to 0.85V, (Notes 12, 14) | +25 | - | 20 | 60 | m Ω |
| | | Full | - | - | 70 | m Ω |
| r _{ON} Matching Between Channels, Δr_{ON} | I _{XOUT} = 40mA, V _{LIN} or V _{RIN} = Voltage at max r _{ON} over signal range of -0.85V to 0.85V, (Notes 13, 14) | +25 | - | 0.1 | 0.32 | Ω |
| | | Full | - | - | 0.4 | Ω |
| Active Click and Pop Shunt Resistance | V _{CTRL} = 0V, V _{IN} = 0V, V _{LIN} or V _{RIN} = -1.5V to 1.5V, ISL54410 only | +25 | - | 40 | - | Ω |
| | | Full | - | - | - | Ω |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-ON Time, t _{ON} | V _{DD} = 2.7V, R _L = 50 Ω , C _L = 10pF (see Figure 1) | +25 | - | 5 | - | μ s |
| Turn-OFF Time, t _{OFF} | V _{DD} = 2.7V, R _L = 50 Ω , C _L = 10pF (see Figure 1) | +25 | - | 45 | - | ns |
| OFF-Isolation | V _{IN} = 3V, V _{LIN} or V _{RIN} = 0.707V _{RMS} , R _L = 32 Ω , f = 20Hz to 20kHz (see Figure 3) | +25 | - | 110 | - | dB |
| Crosstalk RIN to LOUT, LIN to ROUT | V _{CTRL} = 3.0V, V _{IN} = 0V, R _L = 32 Ω , f = 20Hz to 20kHz, V _{LIN} or V _{RIN} = 0.707V _{RMS} (2V _{p-p}), (See Figure 4) | +25 | - | -90 | - | dB |

ISL54409, ISL54410

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: $V_{DD} = +3.0V$, $GND = 0V$, $V_{CTRL} = 1.4V$, $V_{IN} = 0.5V$, (Notes 9, 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 10, 11) | TYP | MAX (Notes 10, 11) | UNITS |
|---|---|-----------|--------------------|------|--------------------|---------------|
| Total Harmonic Distortion | $f = 20\text{Hz to } 20\text{kHz}$, $V_{CTRL} = 3.0V$, $V_{IN} = 0V$, V_{LIN} or $V_{RIN} = 0.36V_{RMS}$ (1V _{p-p}), $R_L = 32\Omega$ | +25 | - | 0.03 | - | % |
| | $f = 20\text{Hz to } 20\text{kHz}$, $V_{CTRL} = 3.0V$, $V_{IN} = 0V$, V_{LIN} or $V_{RIN} = 0.707V_{RMS}$ (2V _{p-p}), $R_L = 32\Omega$ | +25 | - | 0.06 | - | % |
| COM-, COM+ OFF Capacitance, C_{OFF} | $f = 240\text{MHz}$, $V_{CTRL} = 0V$, $V_{IN} = 3V$, V_{LIN} or $V_{RIN} = 0V$ | +25 | - | 5 | - | pF |
| | $f = 240\text{MHz}$, $V_{CTRL} = 0V$, $V_{IN} = 0V$, V_{LIN} or $V_{RIN} = 0V$ | +25 | - | 4 | - | pF |
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range, V_{DD} | | Full | 2.7 | | 3.6 | V |
| Audio Mode Supply Current, I_{DD} | $V_{DD} = 3.6V$ | +25 | - | 7 | 13 | μA |
| | | Full | - | - | 15 | μA |
| Shutdown Current, I_{SHDN} | $V_{DD} = 3.6V$, $V_{CTRL} = 0.5V$, $V_{IN} = 0.5V$; ISL54409 | +25 | - | 1 | 10 | nA |
| | | Full | - | - | 150 | nA |
| | $V_{DD} = 3.6V$, $V_{CTRL} = 0.5V$, $V_{IN} = 0.5V$; ISL54410 | +25 | - | 2.4 | 4 | μA |
| | | Full | - | - | 5 | μA |
| Power OFF-Current, $I_{RIN/LIN}$ or $I_{COM-/COM+}$ | $V_{DD} = 0V$, $V_{CTRL} = V_{IN} = \text{Float}$, $V_{LIN/RIN} = V_{COM-/COM+} = 5.25V$, | +25 | - | 7 | - | μA |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Logic Voltage Low, V_{Logic_L} | $V_{DD} = 2.7V$ to $3.6V$ | Full | - | - | 0.5 | V |
| Logic Voltage High, V_{Logic_H} | $V_{DD} = 2.7V$ to $3.6V$ | Full | 1.4 | - | - | V |
| Logic Input Low Current, I_{Logic_L} | $V_{DD} = 3.6V$, $V_{Logic} = 0V$ | Full | -50 | 20 | 50 | nA |
| Logic Input High Current, I_{Logic_H} | $V_{DD} = 3.6V$, $V_{Logic} = 3.6V$ | Full | -2 | 1 | 2 | μA |
| Logic Pull-Down Resistor, R_{Logic} | $V_{DD} = 3.6V$, $V_{Logic} = 3.6V$ | Full | - | 4 | - | M Ω |

NOTES:

9. V_{Logic} = Logic input voltage to perform proper function.
10. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
12. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
13. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
14. Limits established by characterization and are not production tested.

Test Circuits and Waveforms

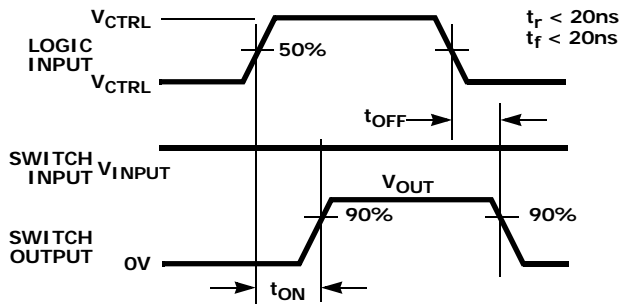
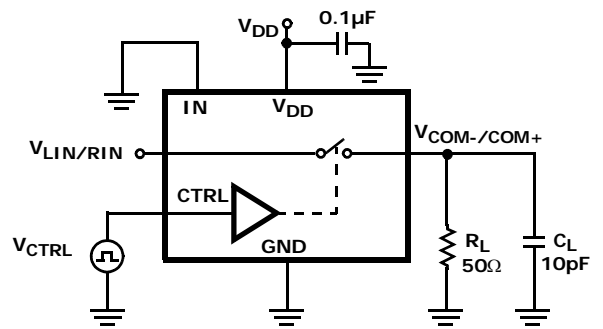


FIGURE 1A. MEASUREMENT POINTS

FIGURE 1. SWITCHING TIMES



* C_L includes board capacitance

FIGURE 1B. TEST CIRCUIT

Repeat test for all switches.
 $r_{ON} = V_1 / 40mA$

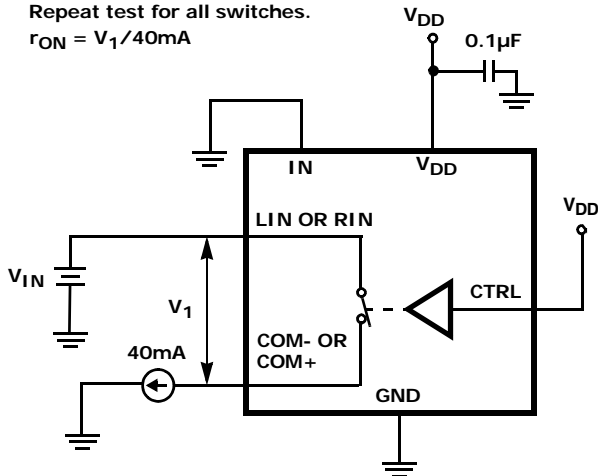


FIGURE 2. r_{ON} TEST CIRCUIT

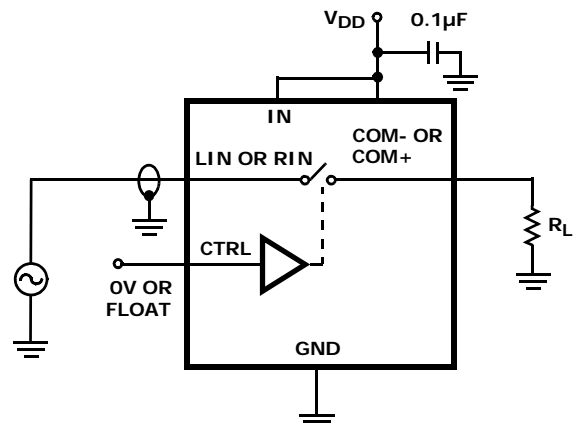


FIGURE 3. OFF ISOLATION CIRCUIT

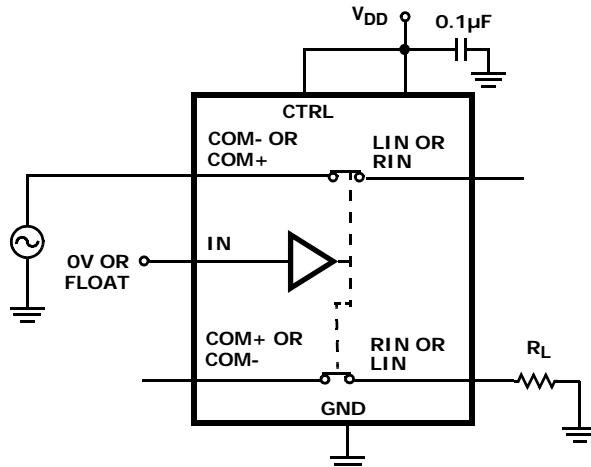


FIGURE 4. CROSSTALK TEST CIRCUIT

Detailed Description

The ISL54409, ISL54410 are +2.7 to +5.0V, Single Pole Single Throw (SPST) audio switches that are negative swing capable. The switch outputs (COM-, COM+) have low OFF capacitance (4pF) that is capable of multiplexing USB2.0 HS data and audio signals in a wired-OR configuration for common connector applications (see “Application Block Diagrams” on page 2). The ISL54409 features a low power shutdown mode while the ISL54410 features audio Click and Pop Elimination circuitry.

The ISL54409, ISL54410 are offered in a 8 Ld 2mmx2mm TDFN or 10 Ld 1.4x1.8mm μ TQFN packages.

Power Supply Considerations

The ISL54409, ISL54410 operates on a +2.7V to +5.0V power supply. A 0.1 μ F local decoupling capacitor placed as close as possible from the V_{DD} pin to GND is highly recommended for stable operation.

Audio Switches

The ISL54409, ISL54410 switches are designed to have low THD+N from a signal range of -1V to +1V for audio applications (see Figures 8 through 11). The ON-resistance of the audio switches have a typical resistance of 2.6 Ω .

The analog signal range of the audio switches are capable beyond -1V to +1V however, the ON-resistance of the switches increases beyond it. The THD+N performance deteriorates beyond a signal range of -1V to +1V.

Audio/USB wired-OR Application

The ISL54409, ISL54410 allows the connection of an audio codec and USB Controller to a common connector. For audio mode of operation, the switch is closed to pass low distortion audio from the codec to a headphone. When the switch is open, USB2.0 HS data (480MBps) can be transmitted to a host controller with minimal signal degradation.

Since the USB device is always connected to the COM- and COM+ pins on the ISL54409, ISL54410, considerations must be taken to protect the USB Controller when passing audio signals through the switch. The USB2.0 specification requires the USB data line to sustain a signal of -1V without damage to the device. Audio signals from the codec may swing below -1V in some applications. Since the USB Controller is high impedance when not operating, exceeding -1V may cause high leakage currents or damage sensitive devices on the USB device. It is highly recommended to keep the audio signal range within -1V to +1V.

USB V_{BUS} Hot Plug Operation

The ISL54409, ISL54410 allows the hot plug operation of the USB V_{BUS} signal to operate the switch. This can be accomplished by connecting CTRL to V_{DD} at all times. The V_{BUS} signal from the USB Host is used to drive the IN logic pin. Note from the “Absolute Maximum Ratings” on page 5 that the IN pin must be kept below V_{DD} .

Exceeding V_{DD} by putting the 5V V_{BUS} signal to the IN pin will forward bias the ESD diode on the IN pin, which will draw excessive diode current and result in a damaged pin on the device. To prevent damage to the IN pin, it is recommended to place a current limiting series resistor or use a voltage divider to bring the voltage at the IN pin below V_{DD} . A 10k Ω series resistor will reduce current significantly to prevent possible damage to the IN pin. For further protection, a voltage divider with $R_T = 10k\Omega$ will reduce the IN voltage below V_{DD} with no impact on logic threshold voltages (see Figure 5).

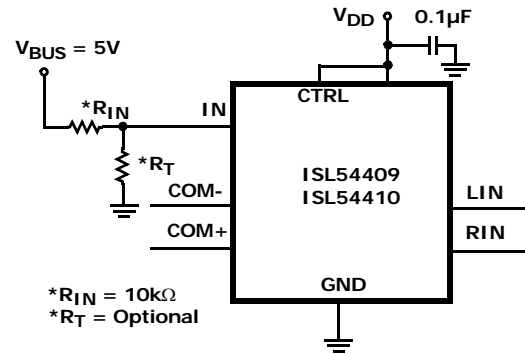


FIGURE 5. USB V_{BUS} HOT PLUG PROTECTION

Low Power Shutdown/Click and Pop Mode

When the CTRL and IN pins are at logic “0”, the ISL54409 and ISL54410 enter into a disabled mode of operation. In the disabled mode of operation, both switches are turned OFF. For the ISL54409, the disabled mode is Low Power Shutdown. The device is brought to a low powered state and the I_{CC} current is significantly reduced.

*Note: When placed in the Low Power Shutdown state, the internal charge pumps that generate the negative supply rails for negative signal swing capability are turned off to reduce power consumption. With the internal negative supply rail disabled the ISL54409 will have poor isolation and crosstalk performance for negative signal swings on the switch terminals. Negative voltages will have a low impedance path to the other switch terminals. It is not recommended to operate the switch in Low Power Shutdown if the audio codec will remain active when transmitting USB data on the COM- and COM+ pins.

For the ISL54410, the disabled mode is Audio Click and Pop Elimination. The switch input pins LIN and RIN have their active Click and Pop circuitry enabled, which turns on a typical 40 Ω shunt resistance from the switch input pin to GND. Some audio application requires DC biasing the audio codec above ground for full output signal swing. The audio signal must have the DC component removed with a blocking capacitor at the headphone load. This blocking capacitor is typically the source of audible click and pop transients when the audio codec powers up or down with the DC bias. The negative signal swing capability of the audio switch allows the DC blocking capacitor to be placed on input side of the switch, which allows the Click and Pop Elimination circuitry to discharge the DC blocking capacitor of any transient currents, eliminating audio clicks and pops.

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified

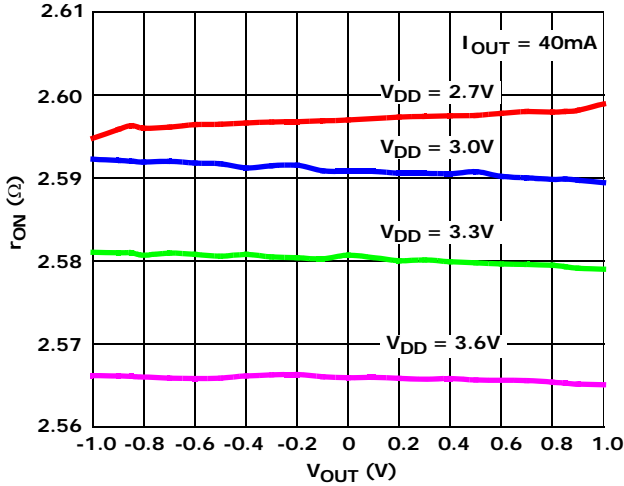


FIGURE 6. ON-RESISTANCE vs SWITCH VOLTAGE vs SUPPLY VOLTAGE

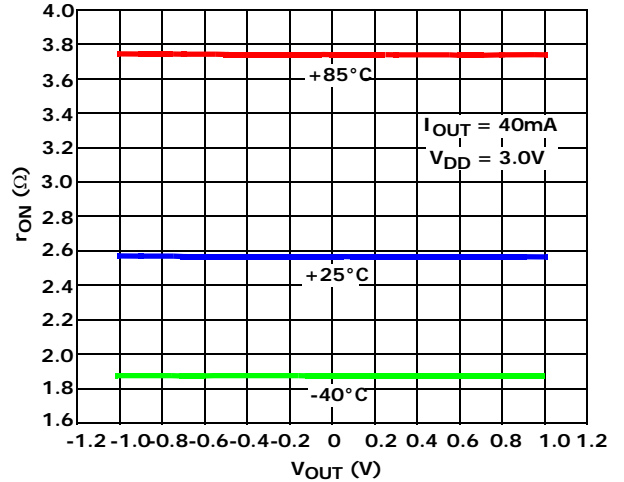


FIGURE 7. ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

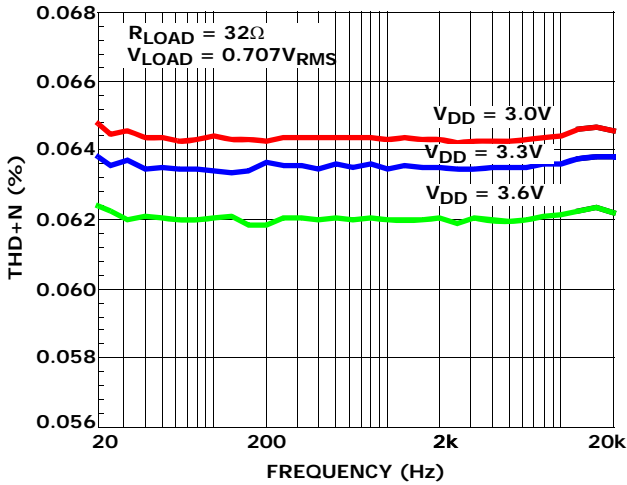


FIGURE 8. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

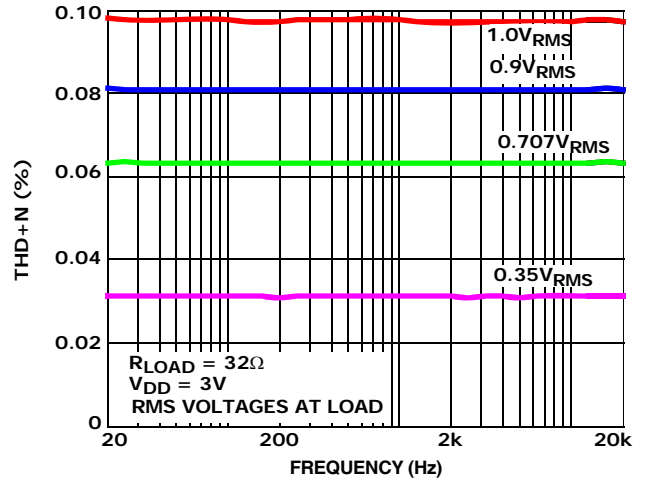


FIGURE 9. THD+N vs SIGNAL LEVELS vs FREQUENCY

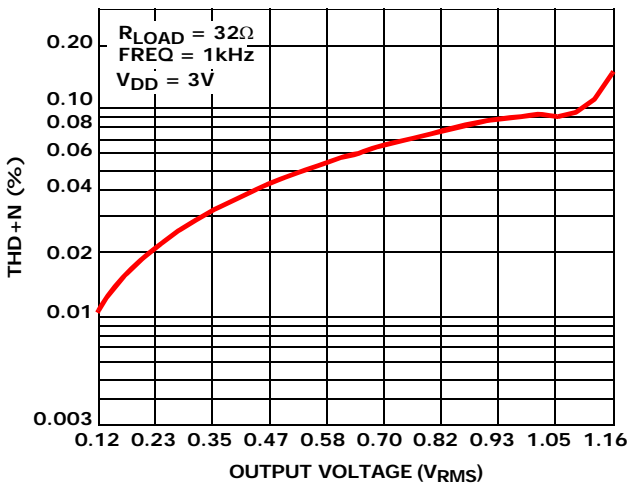


FIGURE 10. THD+N vs OUTPUT VOLTAGE

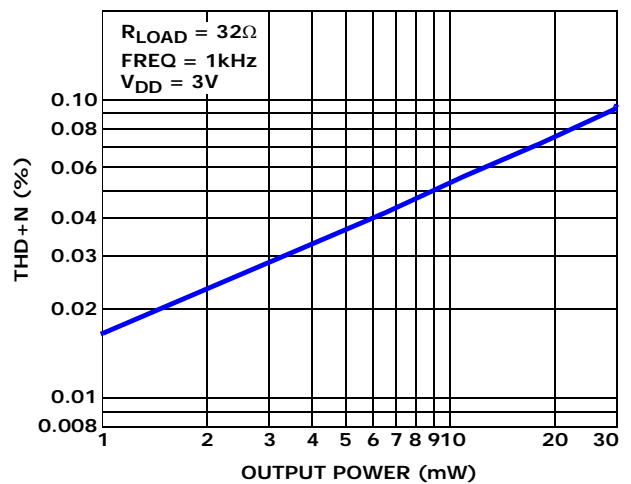


FIGURE 11. THD+N vs OUTPUT POWER

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified (Continued)

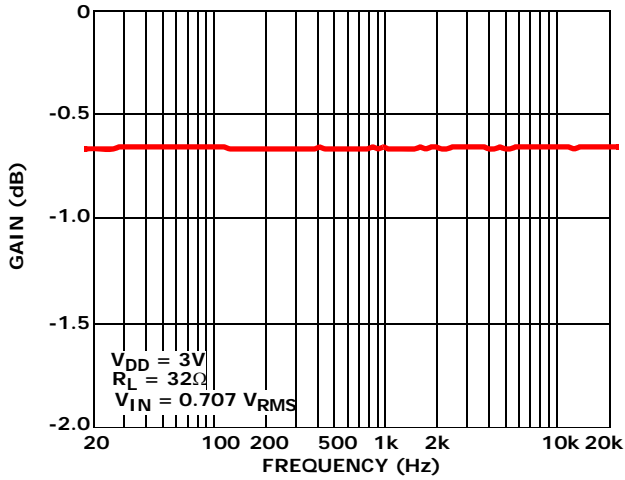


FIGURE 12. INSERTION LOSS

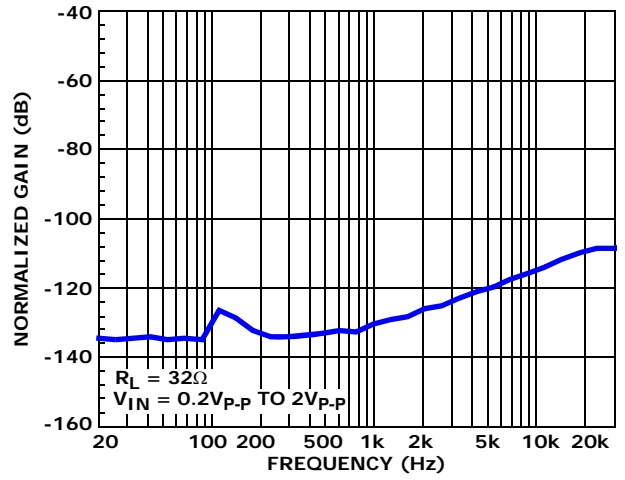


FIGURE 13. OFF-ISOLATION

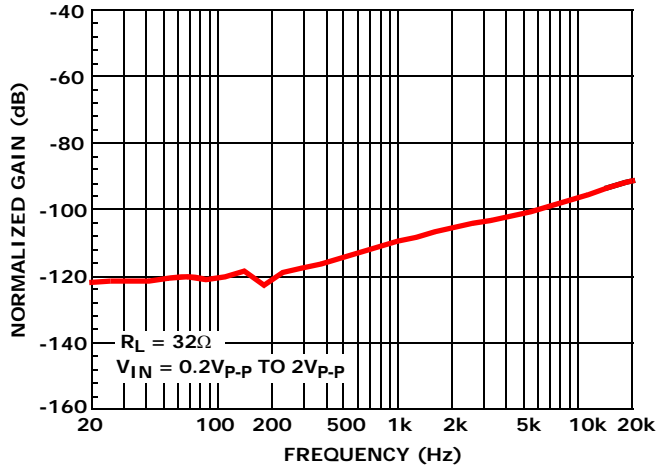


FIGURE 14. CROSSTALK

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---------|----------|--|
| 1/14/10 | FN6983.0 | Removed "Coming Soon" from TDFN package options in "Ordering Information" on page 4. Added "ISL54409EVAL1Z" to "Ordering Information" on page 4. Updated Package Outline Drawing L10.1.8x1.4A on page 12. Revisions were to move dimensions from table onto drawing. |
| 9/25/09 | FN6983.0 | Initial Release. |

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL54409](#), [ISL54410](#)

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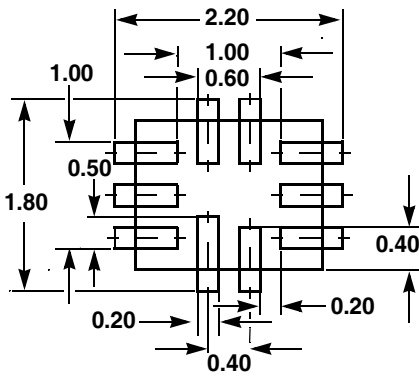
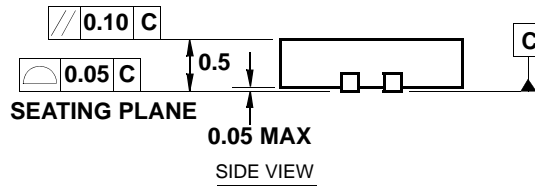
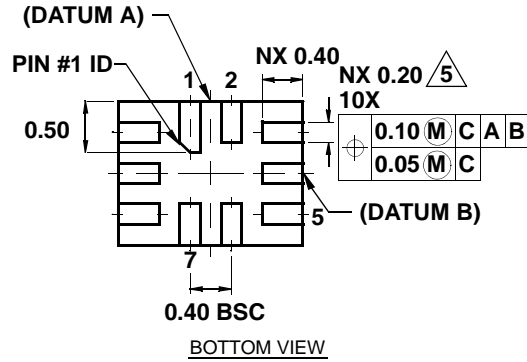
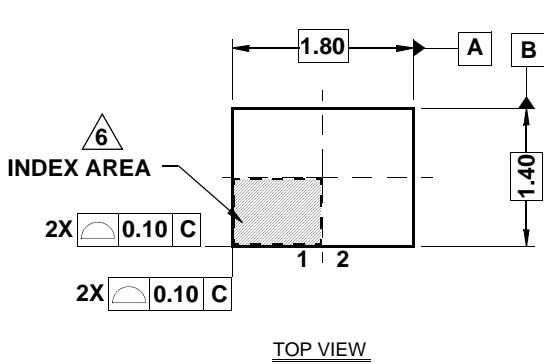
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Package Outline Drawing

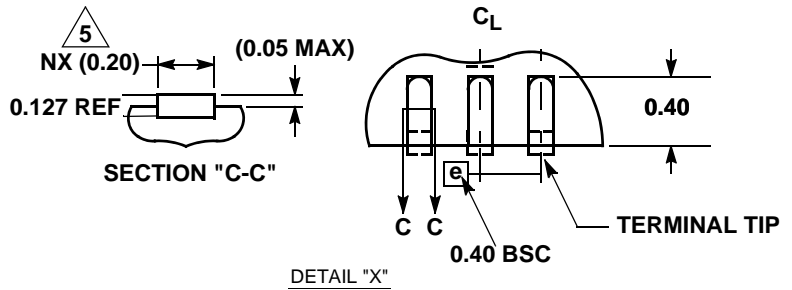
L10.1.8x1.4A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 4, 9/09



TYPICAL RECOMMENDED LAND PATTERN



NOTES:

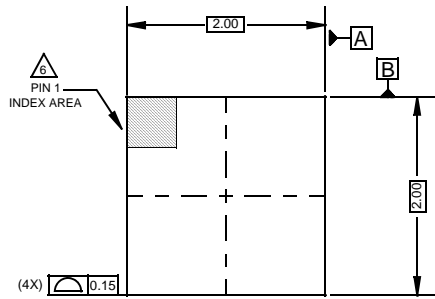
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals. Total 10 leads.
3. Nd and Ne refer to the number of terminals on D (4) and E (6) side, respectively.
4. All dimensions are in millimeters. Tolerances $\pm 0.05\text{mm}$ unless otherwise noted. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

Package Outline Drawing

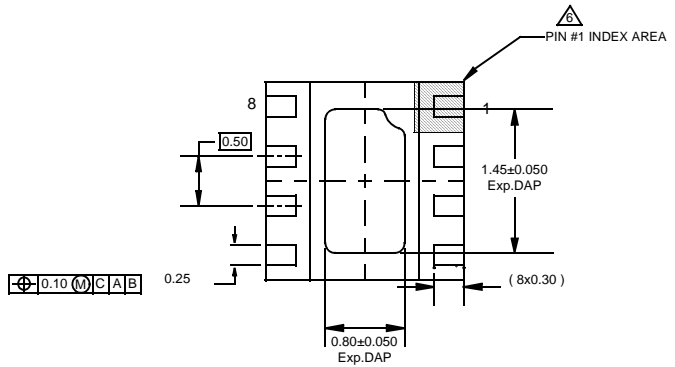
L8.2x2C

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN) WITH E-PAD

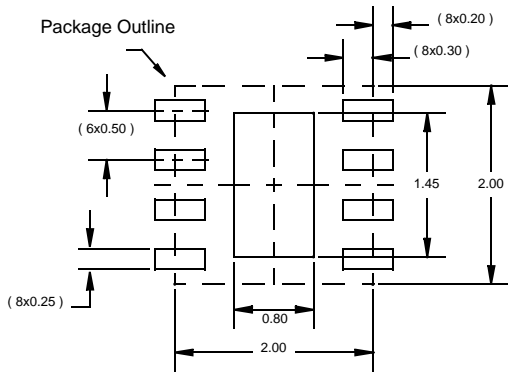
Rev 0, 07/08



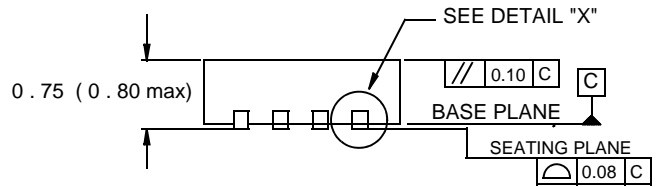
TOP VIEW



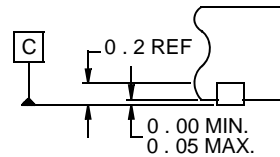
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.