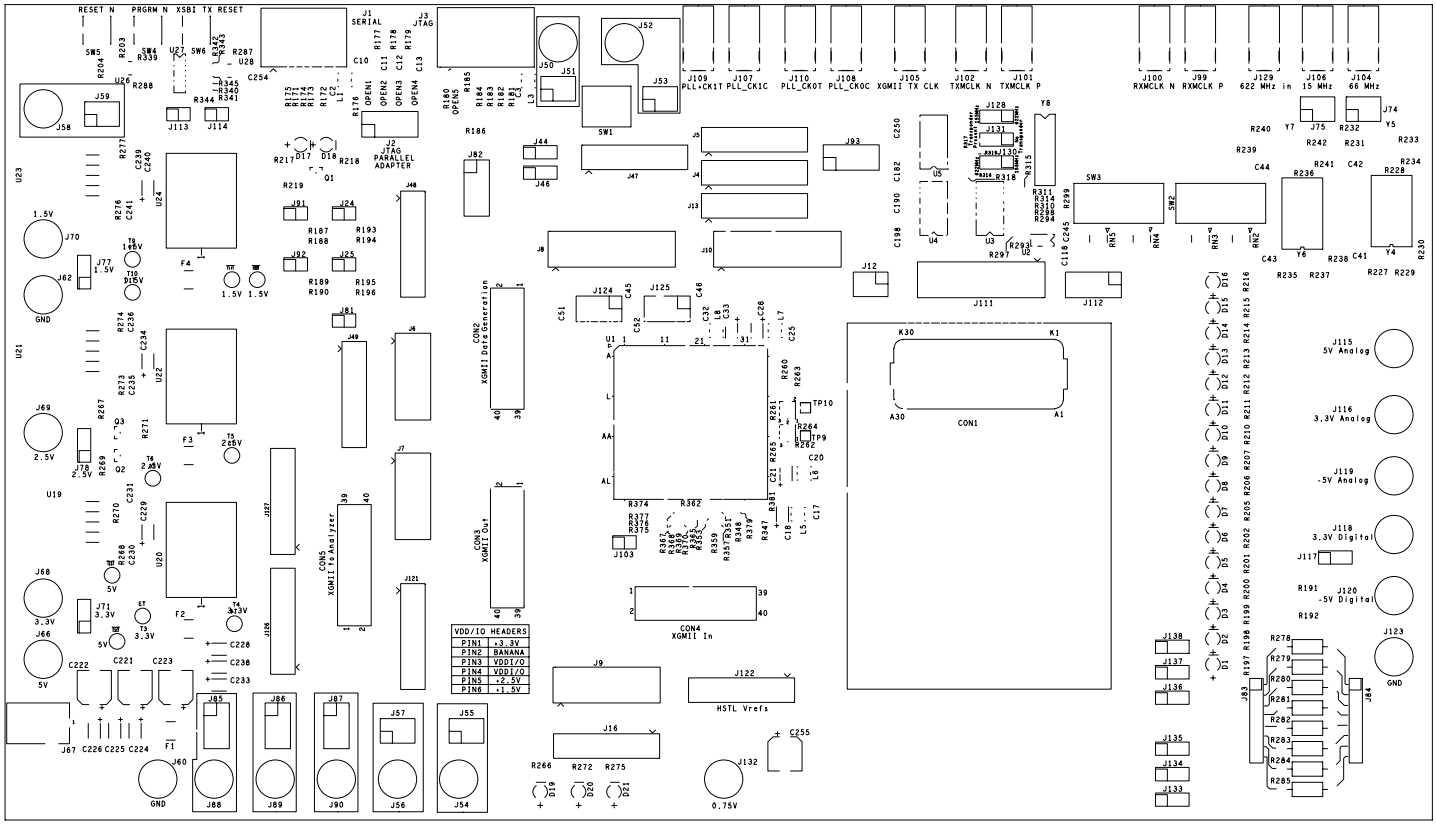
ORLI10G
Evaluation Board
User Manual

SECTION	PAGE

Layout of ORLI10G board:



Connectors and jumpers J1 to J127:

J1

Schematic page 2

A 7-pin serial connector used for configuration. An arrow, as well as the company's logo indicates pin one.

Serial Connector	
Pin 1	VDD
Pin 2	CCLK
Pin 3	D0
Pin 4	DONE
Pin 5	PROG
Pin 6	NC
Pin 7	GND

J2

Schematic page 2

Ten-pin header (2X5) used with an adapter to program the device via a parallel cable. **J2** is numbered as a standard header. Looking at it from above, pin one would be the top left pin. Pin two is to the right of pin one. Pin three is under pin one. Pin four is to the right of pin three, etc.

JTAG Parallel Adapter			
Pin 1	VDD	Pin 2	DONE
Pin 3	PRGRM_N	Pin 4	TDI
Pin 5	RESET_N	Pin 6	TMS
Pin 7	INIT_N	Pin 8	TCK
Pin 9	GND	Pin 10	RD_DATA_TDO

J3

Schematic page 2

J3 is an 8-pin JTAG connector. It is physically similar to **J1**; an arrow indicates pin 1.

JTAG Connector	
Pin 1	VDD
Pin 2	TDI
Pin 3	TMS
Pin 4	TCK
Pin 5	TDO
Pin 6	RD_CFG
Pin 7	INIT_N
Pin 8	GND

J4

Schematic page 2

This is a *standard* header. Pin one is at the top left. Pin numbers increment from left to right. The pins on this header correspond to dip switches. **J4** is in line with **J13**. They can be connected via a ribbon cable to provide input for the ORLI10G.

J4			
Pin 1	SW3.1	Pin 2	SW3.2
Pin 3	SW3.3	Pin 4	SW3.4
Pin 5	SW3.5	Pin 6	SW3.6
Pin 7	SW3.7	Pin 8	SW3.8
Pin 9	NC	Pin 10	NC
Pin 11	SW2.8	Pin 12	SW2.7
Pin 13	SW2.6	Pin 14	SW2.5
Pin 15	SW2.4	Pin 16	SW2.3
Pin 17	SW2.2	Pin 18	SW2.1
Pin 19	NC	Pin 20	NC

J5

Schematic page 4

This is a standard header as described above. This header connects to LEDs. When a jumper cable is used, output from the ORLI10G can drive these LEDs to display a pattern. The connections are:

J5			
Pin 1	red LED	Pin 2	red LED
Pin 3	red LED	Pin 4	red LED
Pin 5	yellow LED	Pin 6	yellow LED
Pin 7	yellow LED	Pin 8	yellow LED
Pin 9	N.C.	Pin 10	N.C.
Pin 11	green LED	Pin 12	green LED
Pin 13	green LED	Pin 14	green LED
Pin 15	red LED	Pin 16	red LED
Pin 17	red LED	Pin 18	red LED
Pin 19	N.C.	Pin 20	N.C.

J5 is positioned in line with **J13**. They can be connected with a ribbon cable to provide a visual output for the ORLI10G.

J6-J7

Schematic page 7

These are 3 by 8 headers that provide differential output from the ORLI10G. The first column (pins 1, 4, 7, 10, etc.) connect to the true side of the pair. Ground is connected to the middle column (pins 2, 5, 8, 11, etc.). And, the third column (pins 3, 6, 9, 12, etc.) are connected to the complement side of the pair.

J6					
Pin 1	PL5A	Pin 2	GND	Pin 3	PL5B
Pin 4	PL6C	Pin 5	GND	Pin 6	PL6D
Pin 7	PL9C	Pin 8	GND	Pin 9	PL9D
Pin 10	PL12A	Pin 11	GND	Pin 12	PL12B
Pin 13	PL12C	Pin 14	GND	Pin 15	PL12D
Pin 16	PL13A	Pin 17	GND	Pin 18	PL13B
Pin 19	PL18A	Pin 20	GND	Pin 21	PL18B
Pin 22	PL19A	Pin 23	GND	Pin 24	PL19B

J7					
Pin 1	PL20A	Pin 2	GND	Pin 3	PL20B
Pin 4	PL21A	Pin 5	GND	Pin 6	PL21B
Pin 7	PL27A	Pin 8	GND	Pin 9	PL27B
Pin 10	PL34A	Pin 11	GND	Pin 12	PL34B
Pin 13	PL35A	Pin 14	GND	Pin 15	PL35B
Pin 16	PL39A	Pin 17	GND	Pin 18	PL39B
Pin 19	PL4C	Pin 20	GND	Pin 21	PL4D
Pin 22	NC	Pin 23	GND	Pin 24	NC

J8 and J10

Schematic page 7

These are 3 by 12 headers that provide differential output from the ORLI10G. The first column (pins 1, 4, 7, 10, etc.) connect to the true side of the pair. Ground is connected to the middle column (pins 2, 5, 8, 11, etc.). And, the third column (pins 3, 6, 9, 12, etc.) are connected to the complement side of the pair.

J8					
Pin 1	NC	Pin 2	GND	Pin 3	NC
Pin 4	PT2A	Pin 5	GND	Pin 6	PT2B
Pin 7	PT3A	Pin 8	GND	Pin 9	PT3B
Pin 10	PT4A	Pin 11	GND	Pin 12	PT4B
Pin 13	PT5C	Pin 14	GND	Pin 15	PT5D
Pin 16	PT6C	Pin 17	GND	Pin 18	PT6D
Pin 19	PT7C	Pin 20	GND	Pin 21	PT7D
Pin 22	PT27A	Pin 23	GND	Pin 24	PT27B
Pin 25	PT28A	Pin 26	GND	Pin 27	PT28B
Pin 28	PT28C	Pin 29	GND	Pin 30	PT28D
Pin 31	PT29A	Pin 32	GND	Pin 33	PT29B
Pin 34	PT29C	Pin 35	GND	Pin 36	PT29D

J10					
Pin 1	PT10C	Pin 2	GND	Pin 3	PT10D
Pin 4	PT12A	Pin 5	GND	Pin 6	PT12B
Pin 7	PT13C	Pin 8	GND	Pin 9	PT13D
Pin 10	PT15C	Pin 11	GND	Pin 12	PT15D
Pin 13	PT18A	Pin 14	GND	Pin 15	PT18B
Pin 16	PT19A	Pin 17	GND	Pin 18	PT19B
Pin 19	PT20C	Pin 20	GND	Pin 21	PT20D
Pin 22	PT21C	Pin 23	GND	Pin 24	PT21D
Pin 25	PT22C	Pin 26	GND	Pin 27	PT22D
Pin 28	PT23C	Pin 29	GND	Pin 30	PT23D
Pin 31	PT25C	Pin 32	GND	Pin 33	PT25D
Pin 34	PT26A	Pin 35	GND	Pin 36	PT26B

J9

Schematic page 7

These are 3 by 10 headers that provide differential output from the ORLI10G. The first column (pins 1, 4, 7, 10, etc.) connect to the true side of the pair. Ground is connected to the middle column (pins 2, 5, 8, 11, etc.). And, the third column (pins 3, 6, 9, 12, etc.) are connected to the complement side of the pair.

J9					
Pin 1	GND	Pin 2	GND	Pin 3	GND
Pin 4	PB2A	Pin 5	GND	Pin 6	PB2B
Pin 7	PB6A	Pin 8	GND	Pin 9	PB6B
Pin 10	PB11A	Pin 11	GND	Pin 12	PB11B
Pin 13	PB12A	Pin 14	GND	Pin 15	PB12B
Pin 16	PB13A	Pin 17	GND	Pin 18	PB13B
Pin 19	PB14A	Pin 20	GND	Pin 21	PB14B
Pin 22	PB30C	Pin 23	GND	Pin 24	PB30D
Pin 25	PB32C	Pin 26	GND	Pin 27	PB32D
Pin 28	GND	Pin 29	GND	Pin 30	GND

J11

Schematic page 10

SMA outputs the RX Clock from the XGMII interface.

J12

Schematic page 15

This is a standard 2 by 3 header that connects to the transponder to provide input.

J12			
Pin 1	LsTUNE0	Pin 2	GND
Pin 3	LsTUNE1	Pin 4	GND
Pin 5	LsTUNE2	Pin 6	GND

J13

Schematic page 6

This is a standard header that is physically located in line with **J5** and **J4**. By using a ribbon cable as a jumper, one can use output signals from **J13** to control the LEDs via **J5**, or control the input signals by the dip switches via **J4**. Only 16 pins are used for this purpose. The header can also be used as basic input/output.

J13			
Pin 1	PT3D	Pin 2	PT15A
Pin 3	PT5B	Pin 4	PT16A
Pin 5	PT6A	Pin 6	PT16C
Pin 7	PT9A	Pin 8	PT17A
Pin 9	PT9C	Pin 10	PT19D
Pin 11	PT10A	Pin 12	PT22A
Pin 13	PT11A	Pin 14	PT23A
Pin 15	PT13B	Pin 16	PT24A
Pin 17	PT14A	Pin 18	PT24D
Pin 19	PT14D	Pin 20	PT26D

J16

Schematic page 6

This is a standard header. By connecting this header to either **J5** or **J4** with a ribbon cable, one can use the jumpers to input signals to the ORLI10G or display the output of signals from the ORLI10G. Only the first 16 pins are used for this purpose. The header can also be used as basic input/output.

J16			
Pin 1	PB33C	Pin 2	PB9C
Pin 3	PB31D	Pin 4	PB9A
Pin 5	PB30A	Pin 6	PB8A
Pin 7	PB19C	Pin 8	PB7C
Pin 9	PB16A	Pin 10	PB7A
Pin 11	PB15C	Pin 12	PB6C
Pin 13	PB15A	Pin 14	PB4C
Pin 15	PB13C	Pin 16	PB4B
Pin 17	PB11C	Pin 18	PB3C
Pin 19	PB10A	Pin 20	PB3A

J24, J25

Schematic page 3

These headers are the chip select controls. The default is selected when no jumpers are present. **J24** controls CS1 and **J25** controls CS0_N.

J44, J46

Schematic page 13

These are three pin headers for the differential clock input. Pin one is complement, pin two is ground, and pin three is true.

J47-J49

Schematic page 18

These are 2X10 reference voltage headers. The extra pins are unconnected.

J47			
Pin 1	VREF_TC10	Pin 2	VREF_TC06
Pin 3	VREF_TC05	Pin 4	VREF_TC04
Pin 5	VREF_TC03	Pin 6	VREF_TC02
Pin 7	VREF_TC01	Pin 8	NC
Pin 9	NC	Pin 10	NC
Pin 11	NC	Pin 12	NC
Pin 13	NC	Pin 14	NC
Pin 15	NC	Pin 16	NC
Pin 17	NC	Pin 18	NC
Pin 19	NC	Pin 20	NC

J48			
Pin 1	VREF_TL01	Pin 2	VREF_TL02
Pin 3	VREF_TL03	Pin 4	VREF_TL04
Pin 5	VREF_TL05	Pin 6	VREF_TL06
Pin 7	VREF_TL07	Pin 8	VREF_TL08
Pin 9	VREF_TL09	Pin 10	VREF_TL10
Pin 11	NC	Pin 12	NC
Pin 13	NC	Pin 14	NC
Pin 15	NC	Pin 16	NC
Pin 17	NC	Pin 18	NC
Pin 19	NC	Pin 20	NC

J49			
Pin 1	VREF_CL1	Pin 2	VREF_CL2
Pin 3	VREF_CL3	Pin 4	VREF_CL4
Pin 5	VREF_CL5	Pin 6	VREF_CL6
Pin 7	VREF_CL7	Pin 8	VREF_CL8
Pin 9	NC	Pin 10	NC
Pin 11	NC	Pin 12	NC
Pin 13	NC	Pin 14	NC
Pin 15	NC	Pin 16	NC
Pin 17	NC	Pin 18	NC
Pin 19	NC	Pin 20	NC

J50, J52, J54, J56, J58

Schematic page 19

These banana jacks may be selected by connecting pin two with pin four on jumpers **J51**, **J53**, **J55**, **J57**, and **J59**, respectively, as input for the VddI/O.

J51, J53, J55, J57, J59

Schematic page 19

A 2 by 3 header that allows jumpers to select the input for the VddI/O voltage.

J51, J53, J55, J57, and J59			
Pin 1	3.3V	Pin 2	BANANA
Pin 3	VDDIO	Pin 4	VDDIO
Pin 5	2.5V	Pin 6	1.5V

J60, J62

Schematic page 20

These banana jacks are connected to the ground plane of the board.

J66

Schematic page 20

This banana jack connects to 5V and may be used to provide power to the board.

J67

Schematic page 20

This power jack takes 5V from the wall adapter.

J68-J70

Schematic page 21

These banana jacks may be selected to provide power to the board through relays controlled by jumpers **J71**, **J77** and **J78**. **J68** connects to 3.3V input, **J69** connects to 2.5V input, and **J70** connects to 1.5V input.

J71

Schematic page 21

This jumper selects if 3.3V is provided to the board by the regulator or from the banana jack.

J74

Schematic page 11

This jumper selects between a built in 66 MHz oscillator and an oscillator socket. Adding a jumper to pins 1 and 3 selects the socket. Pins 3 and 5 select the 66 MHz oscillator. The connector has a column of ground pins (pins 2, 4, and 6) so that the clock can be sent from the header via a twisted pair.

J74			
Pin 1	CLK SOCKET Y4	Pin 2	GND
Pin 3	SMA J104	Pin 4	GND
Pin 5	66MHz CLK Y5	Pin 6	GND

J75

Schematic page 11

This jumper selects between a built in 15 MHz oscillator and an oscillator socket. Adding a jumper to pins 1 and 3 selects the socket. Pins 3 and 5 select the 15 MHz oscillator. The connector has a column of ground pins (pins 2, 4, and 6) so that the clock can be sent from the header via a twisted pair.

J75			
Pin 1	CLK SOCKET Y6	Pin 2	GND
Pin 3	SMA J106	Pin 4	GND
Pin 5	15 MHz CLK Y7	Pin 6	GND

J77, J78

Schematic page 21

These jumpers select if the board is powered from the regulators or from the banana jacks. **J78** selects the 2.5V source, and **J77** selects the 1.5V source.

J81

Schematic page 3

This two-pin header is used to output the PTEMP signal from the ORLI10G. Pin 2 is connected to ground.

J82

Schematic page 2

J82 is a ten-pin header for additional dedicated signals from the ORLI10G. Unused pins are connected to ground.

J82			
Pin 1	GND	Pin 2	HDC
Pin 3	PCFG_MPI_IRQ	Pin 4	LDC_N
Pin 5	GND	Pin 6	DOUT
Pin 7	GND	Pin 8	RDY_BUSY_N_RCLK
Pin 9	GND	Pin 10	LVDS_R

J83, J84

Schematic page 22

These two 1 X 8 headers connect to the resistor sockets. The table shows the pin connections to the specific sockets.

J83	J84	Resistor
Pin 1	Pin 1	R278
Pin 2	Pin 2	R279
Pin 3	Pin 3	R280
Pin 4	Pin 4	R281
Pin 5	Pin 5	R282
Pin 6	Pin 6	R283
Pin 7	Pin 7	R284
Pin 8	Pin 8	R285

J85-J87

Schematic page 22

These headers are connected to banana jacks **J88**, **J89**, and **J90**.

J88-J90

Schematic page 22

These banana jacks are connected to headers **J85**, **J86**, and **J87**.

J91

Schematic page 3

This header is the PLL_BYPASS control. The default (logic low) is selected when a jumper is not present.

J92

Schematic page 3

This header is the PWRDN control. The default (logic low) is selected when a jumper is not present.

J93

Schematic page 6

This header is for any additional single ended I/O. Unused pins are connected to ground.

J93			
Pin 1	PT27C	Pin 2	GND
Pin 3	PT30A	Pin 4	GND
Pin 5	PT30D	Pin 6	GND
Pin 7	PT31D	Pin 8	PT32D
Pin 9	PT32C	Pin 10	GND

J99 - J102

Schematic page 10

These SMA connectors output the extra clock signals from the transponder.

J99	J100	J101	J102
RXMCLK_P	RXMCLK_N	TXMCLK_P	TXMCLK_N

J104

Schematic page 11

This SMA connector outputs the clock signal from Y5 or Y4 based on jumper placement in header **J74**.

J105 & J367

Schematic page 10

This SMA J105 connector inputs the XGMII_TXCLK_156 clock signal and J367 is input to XGMII_RXCLK_156 signal to the ORLI10G's XGMII interface.

J106

Schematic page 11

This SMA connector outputs the clock signal from Y6 or Y7 based on jumper placement in header **J75**.

J107-J110

Schematic page 13

These SMA connectors provide differential input to the PLL clocks. The pairs are:

J107	J109	J108	J110
PLL_CLK1C	PLL_CLK1T	PLL_CLK0C	PLL_CLK0T

J111

Schematic page 14

This 3 by 12 header is used to select the input to the transponder.

J8					
Pin 1	3.3V	Pin 2	LSENABLE	Pin 3	GND
Pin 4	3.3V	Pin 5	TXREFESL1	Pin 6	GND
Pin 7	3.3V	Pin 8	TXREFSEL0	Pin 9	GND
Pin 10	3.3V	Pin 11	RXREFSEL0	Pin 12	GND
Pin 13	3.3V	Pin 14	RXREFSEL1	Pin 15	GND
Pin 16	3.3V	Pin 17	RXMUTEDOUT	Pin 18	GND
Pin 19	3.3V	Pin 20	RXLCKREF	Pin 21	GND
Pin 22	3.3V	Pin 23	RXMCLKSEL	Pin 24	GND
Pin 25	3.3V	Pin 26	TXSKEWSEL0	Pin 27	GND
Pin 28	3.3V	Pin 29	TXSKEWSEL1	Pin 30	GND
Pin 31	3.3V	Pin 32	TXPCLKSEL	Pin 33	GND
Pin 34	3.3V	Pin 35	TXPICLKSEL	Pin 36	GND

J112

Schematic page 14

Output signals from the transponder.

J112			
Pin 1	LSBIASMON	Pin 2	RESERVED1
Pin 3	LSBIASALM	Pin 4	RESERVED0
Pin 5	RXLOPMON	Pin 6	LSPOWMON
Pin 7	RXLOSMON	Pin 8	TXLOCKERR
Pin 9	RXLOCKERR	Pin 10	NC

J113, J114

Schematic page 4

These jumper headers select if either or both resets from **SW6** are applied to the transponder. If there is a jumper across **J113** then the transmit reset is applied when **SW6** is pushed. If there is a jumper across **J114** then the receive reset is applied when **SW6** is pushed. Both may be used at the same time, so that both are reset when **SW6** is pushed.

J115, J116

Schematic page 15

These banana jacks are connected to the positive analog 5V (**J115**) and the positive analog 3.3V (**J116**) of the transponder.

J117

Schematic page 15

This header allows the selection of the source of the digital 3.3V power to the transponder. Placing a jumper across pin 1 and 2 select the on-board 3.3V, while pin 3 and 2 select the banana jack **J118**.

J118

Schematic page 15

This banana jack is connected to the positive digital 3.3V of the transponder through the header **J117**.

J119, J120

Schematic page 15

These banana jacks are connected to the negative analog 5V (**J119**) and the negative digital 5V (**J120**) of the transponder.

J121, J122

Schematic page 18

These are 2X10 reference voltage headers. The extra pins are unconnected.

J121			
Pin 1	VREF_BL01	Pin 2	VREF_BL02
Pin 3	VREF_BL03	Pin 4	VREF_BL04
Pin 5	VREF_BL05	Pin 6	VREF_BL06
Pin 7	VREF_BL07	Pin 8	VREF_BL08
Pin 9	VREF_BL09	Pin 10	VREF_BL10
Pin 11	VREF_BL11	Pin 12	NC
Pin 13	NC	Pin 14	NC
Pin 15	NC	Pin 16	NC
Pin 17	NC	Pin 18	NC
Pin 19	NC	Pin 20	NC

J122			
Pin 1	VREF_BC08	Pin 2	VREF_BC07
Pin 3	VREF_BC06	Pin 4	VREF_BC05
Pin 5	VREF_BC04	Pin 6	VREF_BC03
Pin 7	VREF_BC02	Pin 8	VREF_BC01
Pin 9	NC	Pin 10	NC
Pin 11	NC	Pin 12	NC
Pin 13	NC	Pin 14	NC
Pin 15	NC	Pin 16	NC
Pin 17	NC	Pin 18	NC
Pin 19	NC	Pin 20	NC

J123

Schematic page 20

This banana jack is connected to the ground plane of the board.

J124, J125

Schematic page 13

J124 to **J125** are eight-pin headers (2X4) that control the termination of the differential clock input provided through SMAs **J107** to **J110**.

J126, J127

Schematic page 3

These 2X10 headers provide an output for any of the microstrip connectors. By jumpering from a Micro-strip connector to **CON5**, one can conveniently view the output by reading it from a logic analyzer through headers **J127** and **J127**. The last two pins on one side of the header are connected to ground.

J126			
Pin 1	CON5.3	Pin 2	CON5.13
Pin 3	CON5.4	Pin 4	CON5.14
Pin 5	CON5.5	Pin 6	CON5.15
Pin 7	CON5.6	Pin 8	CON5.16
Pin 9	CON5.7	Pin 10	CON5.17
Pin 11	CON5.8	Pin 12	CON5.18
Pin 13	CON5.9	Pin 14	CON5.19
Pin 15	CON5.10	Pin 16	CON5.20
Pin 17	CON5.11	Pin 18	GND
Pin 19	CON5.12	Pin 20	GND

J127			
Pin 1	CON5.21	Pin 2	CON5.31
Pin 3	CON5.22	Pin 4	CON5.32
Pin 5	CON5.23	Pin 6	CON5.33
Pin 7	CON5.24	Pin 8	CON5.34
Pin 9	CON5.25	Pin 10	CON5.35
Pin 11	CON5.26	Pin 12	CON5.36
Pin 13	CON5.27	Pin 14	CON5.37
Pin 15	CON5.28	Pin 16	CON5.38
Pin 17	CON5.29	Pin 18	GND
Pin 19	CON5.30	Pin 20	GND

J128

Schematic page 12

This header selects between the socketed 155 MHz clock and clock provided via **J129**. The jumper controls half of the dual 2:1 MUX **U4**. The output is connected to TXREFCLK. Adding a jumper across pin one and two selects **J129** as the output. A jumper across pins two and three selects the 155 MHz clock.

J129

Schematic page 12

This SMA provides the input for the 622/644 MHz clock, if one is not generated from the transponder.

J130

Schematic page 12

This header selects between the socketed 155/156 MHz clock and clock provided via **J129**. The jumper controls half of the dual 2:1 multiplexer **U4**. The output is connected to another MUX, **U5**. Applying a jumper to pins one and two selects the 155 MHz clock on the output. Adding a jumper across pins two and three selects the clock provided via **J129**.

J131

Schematic page 12

This jumper selects the clock returning to the ORLI10G from the transponder. If pin 3 is selected, the transponder is assumed to be present and provided the TXPCLK. If pin 1 is selected the clock is provided on board from the output of **U4** (either the 155 MHz socketed oscillator or the clock input via **J129**).

J132

Schematic page 20

This banana jack is used to provide 0.75V to the board.

J133-J138

Schematic page 14

These are the additional synchronous clocks that are unused when the device is in 10G mode.

Connectors CON1 to CON5:
CON 2

Schematic page 6

This Amp Micro-strip connector has 47 pins. The center row pins are grounded. Check the datasheet from www.amp.com (part number 536255-1) for pin number information. The Amp cable part is 621189. This connector provides test data from the FPGA to the XGMII interface.

CON 1	
Pin 1	GND
Pin 2	GND
Pin 3	PL3D
Pin 4	PL4B
Pin 5	PL7C
Pin 6	PL9A
Pin 7	PL11A
Pin 8	PL11C
Pin 9	PL13C
Pin 10	PL15C
Pin 11	PL16A
Pin 12	PL16C
Pin 13	PL17A
Pin 14	PL18C
Pin 15	PL20C
Pin 16	PL21C
Pin 17	PL23A
Pin 18	PL23C
Pin 19	PL24A
Pin 20	PL24C
Pin 21	PL25A
Pin 22	PL25C
Pin 23	PL26B
Pin 24	PL26C
Pin 25	PL29A
Pin 26	PL29C
Pin 27	PL30C
Pin 28	PL31A
Pin 29	PL31C
Pin 30	PL32A
Pin 31	PL33C
Pin 32	PL36A
Pin 33	PL36C
Pin 34	PL37B
Pin 35	PL38A
Pin 36	PL38B
Pin 37	PL38C
Pin 38	PL39C
Pin 39	GND
Pin 40	GND

CON 3

Schematic page 9

This Amp Micro-strip connector is connected to the XGMII control and data OUT signals.

CON2	XGMII
Pin 1	GND
Pin 2	GND
Pin 3	ctl out 0
Pin 4	ctl out 1
Pin 5	ctl out 2
Pin 6	ctl out 3
Pin 7	data out 0
Pin 8	data out 1
Pin 9	data out 2
Pin 10	data out 3
Pin 11	data out 4
Pin 12	data out 5
Pin 13	data out 6
Pin 14	data out 7
Pin 15	data out 8
Pin 16	data out 9
Pin 17	data out 10
Pin 18	data out 11
Pin 19	data out 12
Pin 20	data out 13
Pin 21	data out 14
Pin 22	data out 15
Pin 23	data out 16
Pin 24	data out 17
Pin 25	data out 18
Pin 26	data out 19
Pin 27	data out 20
Pin 28	data out 21
Pin 29	data out 22
Pin 30	data out 23
Pin 31	data out 24
Pin 32	data out 25
Pin 33	data out 26
Pin 34	data out 27
Pin 35	data out 28
Pin 36	data out 29
Pin 37	data out 30
Pin 38	data out 31
Pin 39	GND
Pin 40	GND

CON 4

Schematic page 9

This Amp Micro-strip connector is connected to the XGMII control and data IN signals.

CON2	XGMII
Pin 1	GND
Pin 2	GND
Pin 3	ctl in 0
Pin 4	ctl in 1
Pin 5	ctl in 2
Pin 6	ctl in 3
Pin 7	data in 0
Pin 8	data in 1
Pin 9	data in 2
Pin 10	data in 3
Pin 11	data in 4
Pin 12	data in 5
Pin 13	data in 6
Pin 14	data in 7
Pin 15	data in 8
Pin 16	data in 9
Pin 17	data in 10
Pin 18	data in 11
Pin 19	data in 12
Pin 20	data in 13
Pin 21	data in 14
Pin 22	data in 15
Pin 23	data in 16
Pin 24	data in 17
Pin 25	data in 18
Pin 26	data in 19
Pin 27	data in 20
Pin 28	data in 21
Pin 29	data in 22
Pin 30	data in 23
Pin 31	data in 24
Pin 32	data in 25
Pin 33	data in 26
Pin 34	data in 27
Pin 35	data in 28
Pin 36	data in 29
Pin 37	data in 30
Pin 38	data in 31
Pin 39	GND
Pin 40	GND

CON 5

Schematic page 3

This Amp Micro-strip connector is issoloate from the ORLI10G. The purpose of this connector is to jump signals from the other microstrip headers to basic 2X10 headers where they can easily be viewed by a logic analyser. Typically a cable would jumper this header to **CON3** or **CON4**.

CON5	
Pin 1	GND
Pin 2	GND
Pin 3	J126.1
Pin 4	J126.3
Pin 5	J126.5
Pin 6	J126.7
Pin 7	J126.9
Pin 8	J126.11
Pin 9	J126.13
Pin 10	J126.15
Pin 11	J126.17
Pin 12	J126.19
Pin 13	J126.2
Pin 14	J126.4
Pin 15	J126.6
Pin 16	J126.8
Pin 17	J126.10
Pin 18	J126.12
Pin 19	J126.14
Pin 20	J126.16
Pin 21	J127.1
Pin 22	J127.3
Pin 23	J127.5
Pin 24	J127.7
Pin 25	J127.9
Pin 26	J127.11
Pin 27	J127.13
Pin 28	J127.15
Pin 29	J127.17
Pin 30	J127.19
Pin 31	J127.2
Pin 32	J127.4
Pin 33	J127.6
Pin 34	J127.8
Pin 35	J127.10
Pin 36	J127.12
Pin 37	J127.14
Pin 38	J127.16
Pin 39	GND
Pin 40	GND

Adjustable resistors:

R261

Schematic page 18

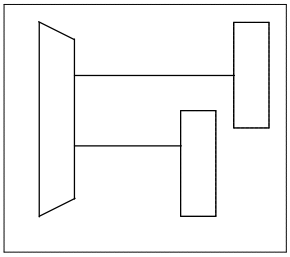
This adjustable resistor is used along with test point (reference **TP10**) to set the 1.4 Volts reference for the ORLI10G.

R264

Schematic page 18

This adjustable resistor is used along with test point (reference **TP9**) to set the 1.0 Volts reference for the ORLI10G.

Microstrip to headers



Standard Headers 3X12
Standard Headers 3X10
Standard Headers 3X8

LVDS I/O

8-Pin JTAG
7-Pin Serial
Parallel Adapter

Standard Headers
Microstrip Connector

Extra I/O

FPGA Control and Test

XGMII OUT
32 bit + 4 control + 1 clock
Microstrip Connector

Line Interface Clock
622 MHz/
644 MHz

TX

RX

TX

RX

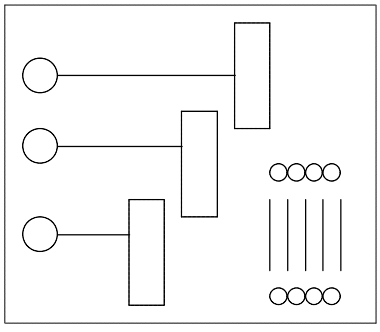
66 MHz

15 MHz

ORLI10G

PLL

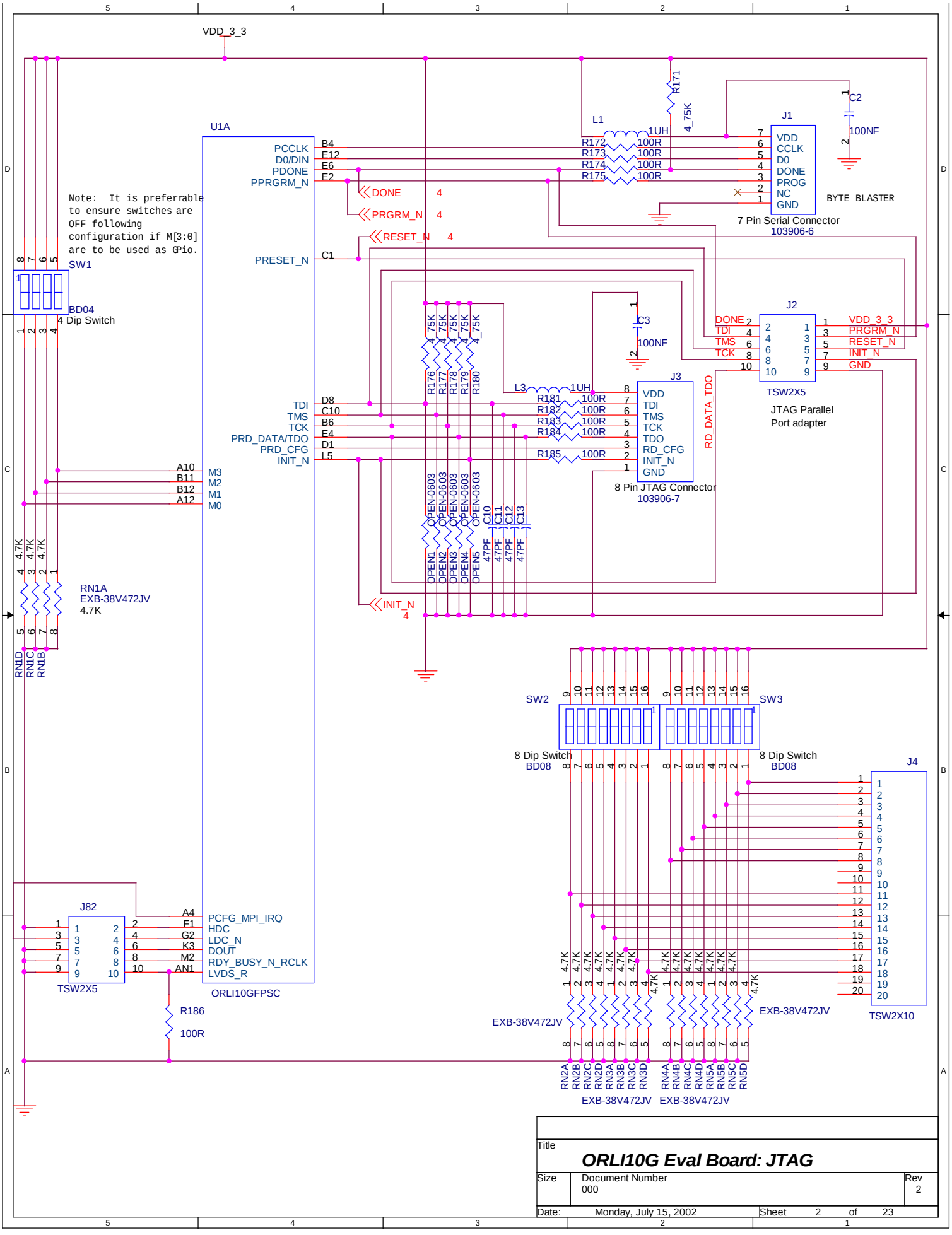
Resistor Sockets
Headers



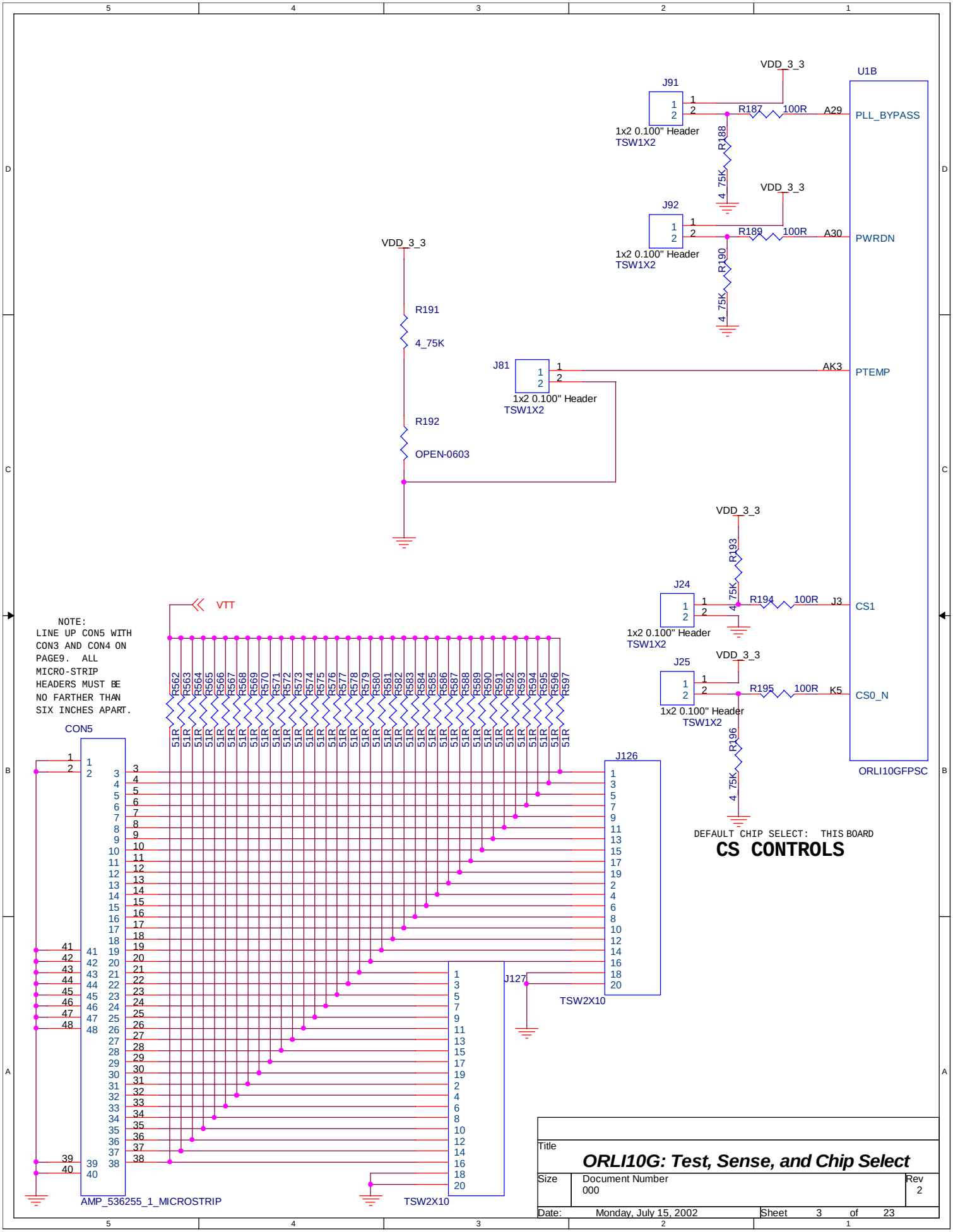
XGMII IN
32 bit + 4 control + 1 clock
Microstrip Connector

50 Ohm SMA

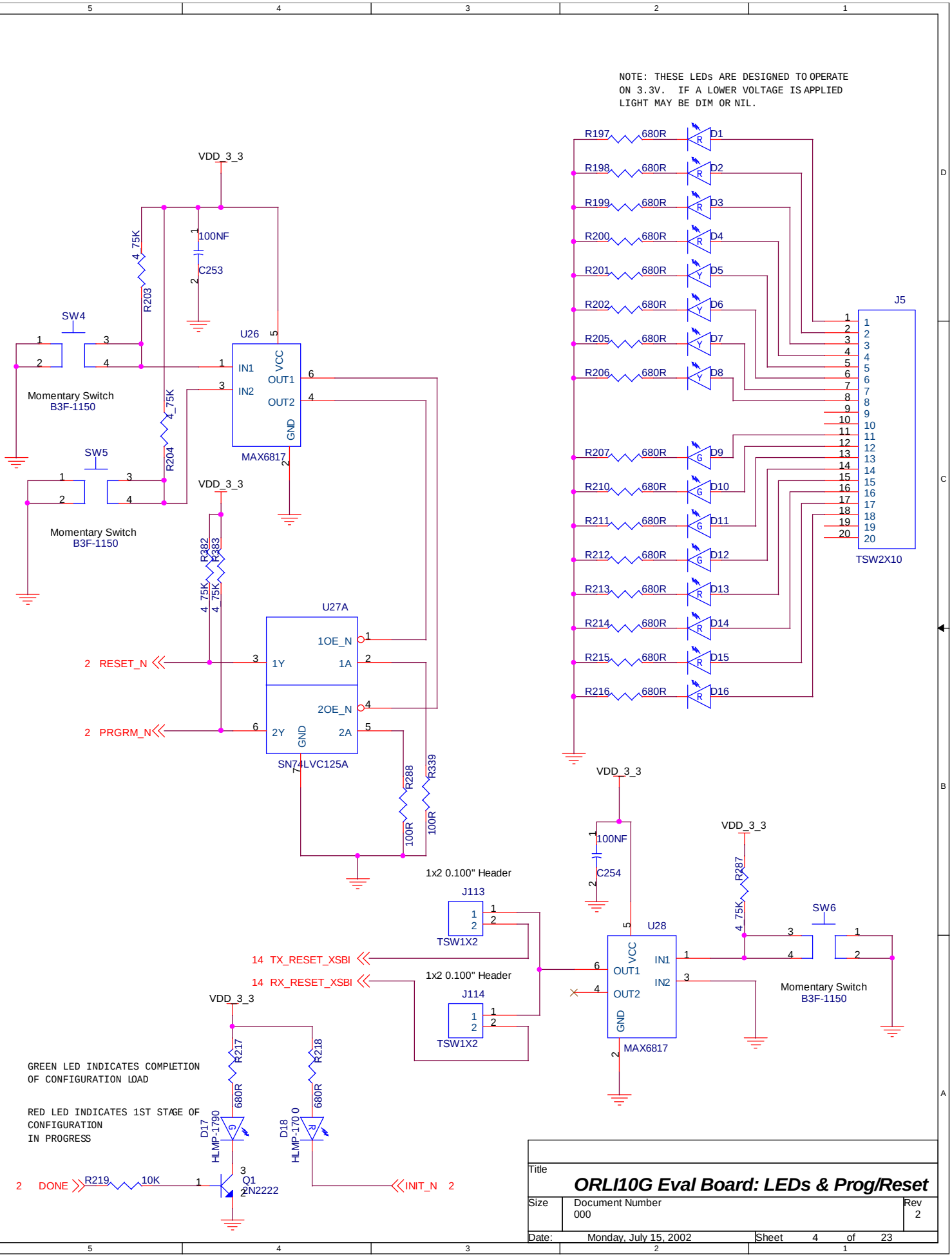
Title	***ORLI10G Eval Board: Block Diagram***	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 1 of 23	

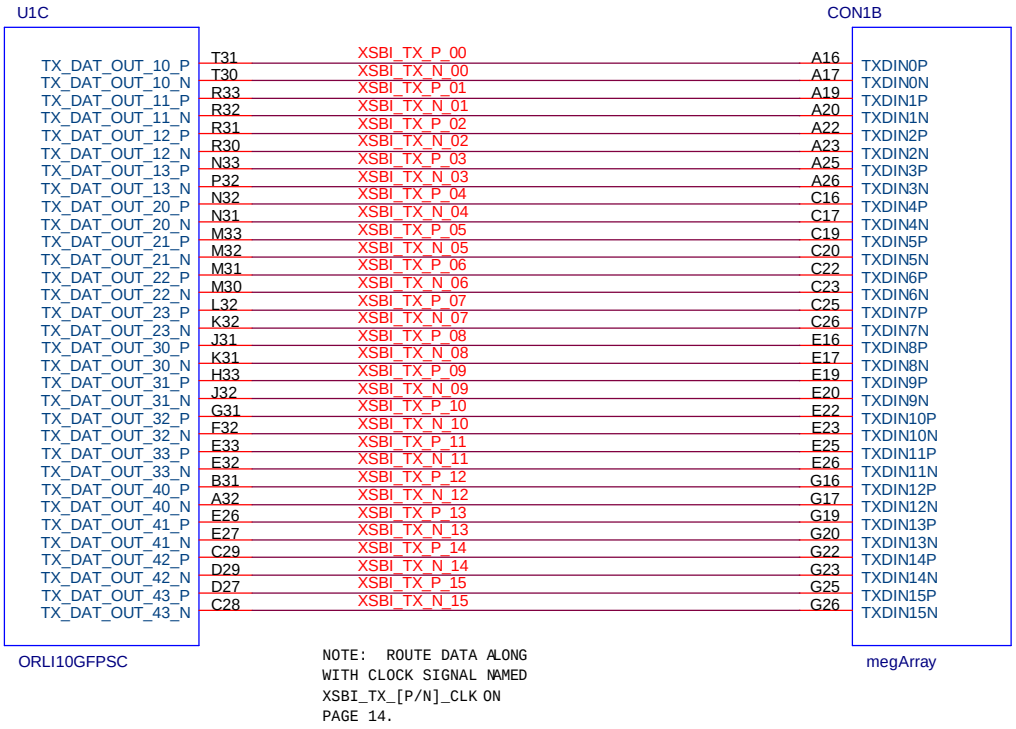


Title	**ORLI10G Eval Board: JTAG**	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 2 of 23	



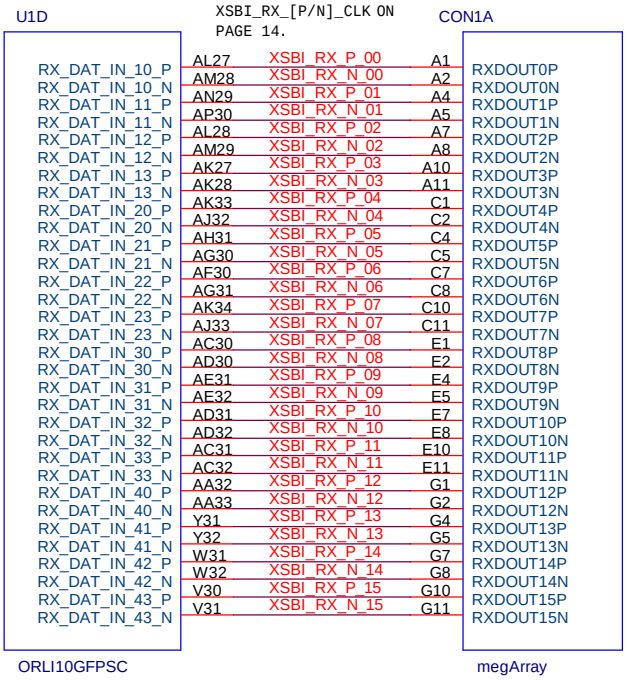
Title	ORLI10G: Test, Sense, and Chip Select	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 3 of 23	


NOTE: THESE LEDs ARE DESIGNED TO OPERATE ON 3.3V. IF A LOWER VOLTAGE IS APPLIED LIGHT MAY BE DIM OR NIL.
VDD_3_3
R197 680R D1
R198 680R D2
R199 680R D3
R200 680R D4
R201 680R D5
R202 680R D6
R205 680R D7
R206 680R D8
R207 680R D9
R210 680R D10
R211 680R D11
R212 680R D12
R213 680R D13
R214 680R D14
R215 680R D15
R216 680R D16
J5
TSW2X10
SW4
SW5
Momentary Switch B3F-1150
Momentary Switch B3F-1150
R203 4.75K
R204 4.75K
100NF C253
U26
IN1
IN2
VCC
OUT1
OUT2
GND
MAX6817
R382 4.75K
R383 4.75K
U27A
1OE_N
2OE_N
1Y
2Y
1A
2A
GND
SN74LVC125A
2 RESET_N
2 PRGRM_N
R288 100R
R339 100R
1x2 0.100" Header
J113
TSW1X2
14 TX_RESET_XSBI
14 RX_RESET_XSBI
1x2 0.100" Header
J114
TSW1X2
100NF C254
U28
MAX6817
R287 4.75K
SW6
Momentary Switch B3F-1150
GREEN LED INDICATES COMPLETION OF CONFIGURATION LOAD
RED LED INDICATES 1ST STAGE OF CONFIGURATION IN PROGRESS
R217 680R
R218 680R
D17 HLMP-1790
D18 HLMP-1700
2 DONE
R219 10K
Q1 2N2222
INIT_N 2
Title
ORLI10G Eval Board: LEDs & Prog/Reset
Size
Document Number 000
Rev 2
Date: Monday, July 15, 2002
Sheet 4 of 23



NOTE: ROUTE DATA ALONG WITH CLOCK SIGNAL NAMED XSBI_TX_[P/N]_CLK ON PAGE 14.

NOTE: ROUTE DATA ALONG WITH CLOCK SIGNAL NAMED XSBI_RX_[P/N]_CLK ON PAGE 14.

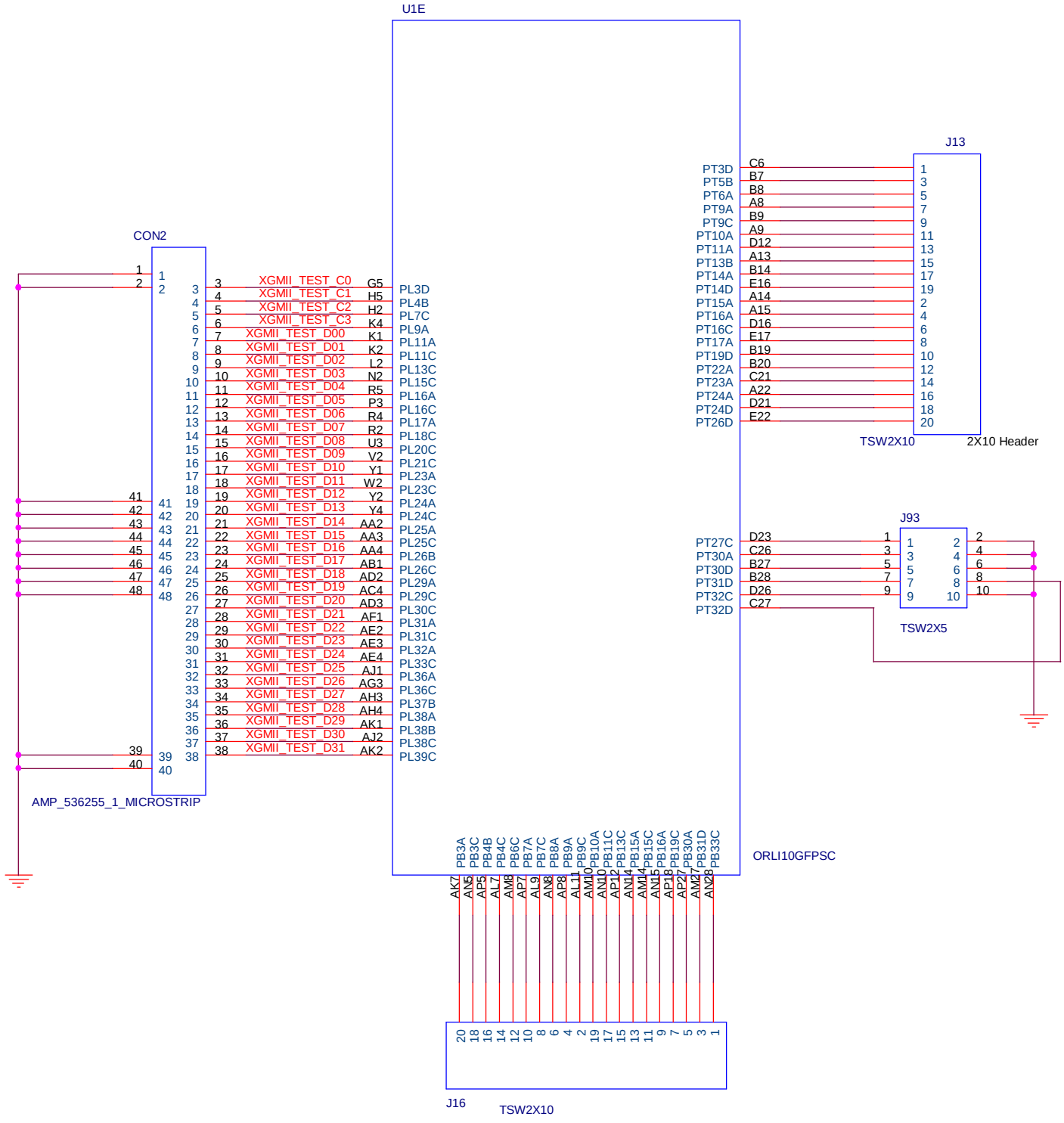


Title

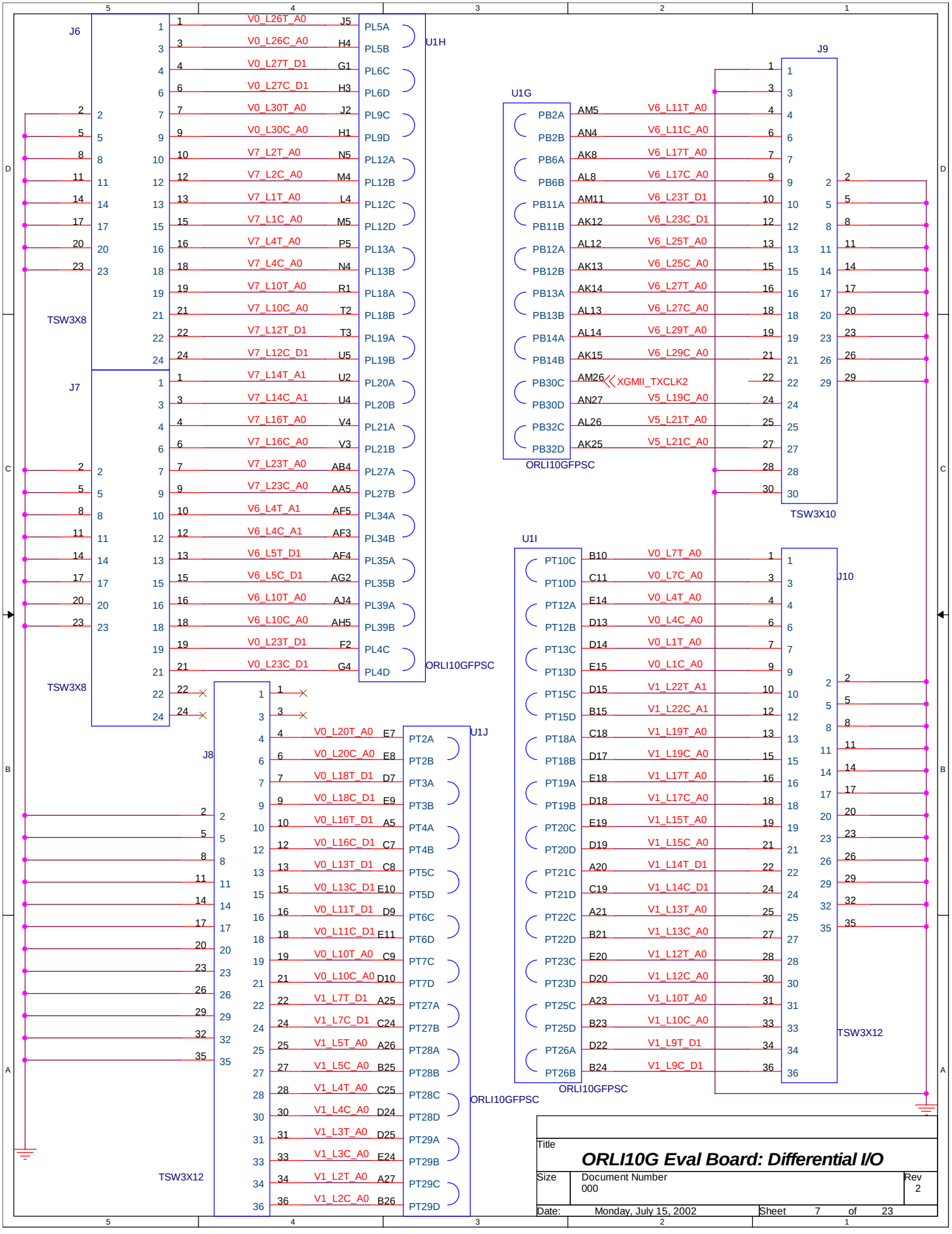
ORLI0G Eval Board: XSBI RX / TX Data

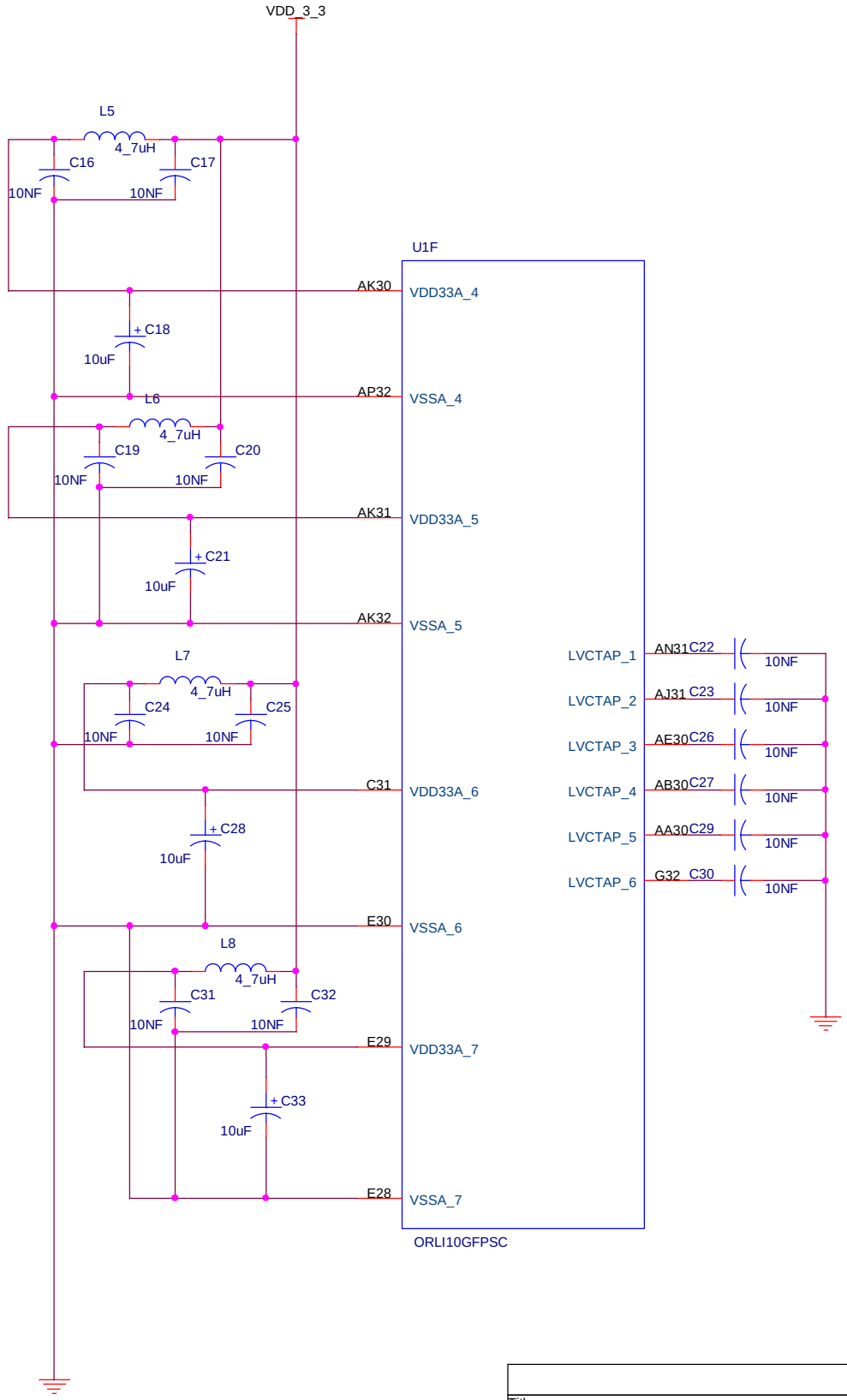
Size	Document Number	Rev
	000	2

Date: Monday, July 15, 2002 Sheet 5 of 23

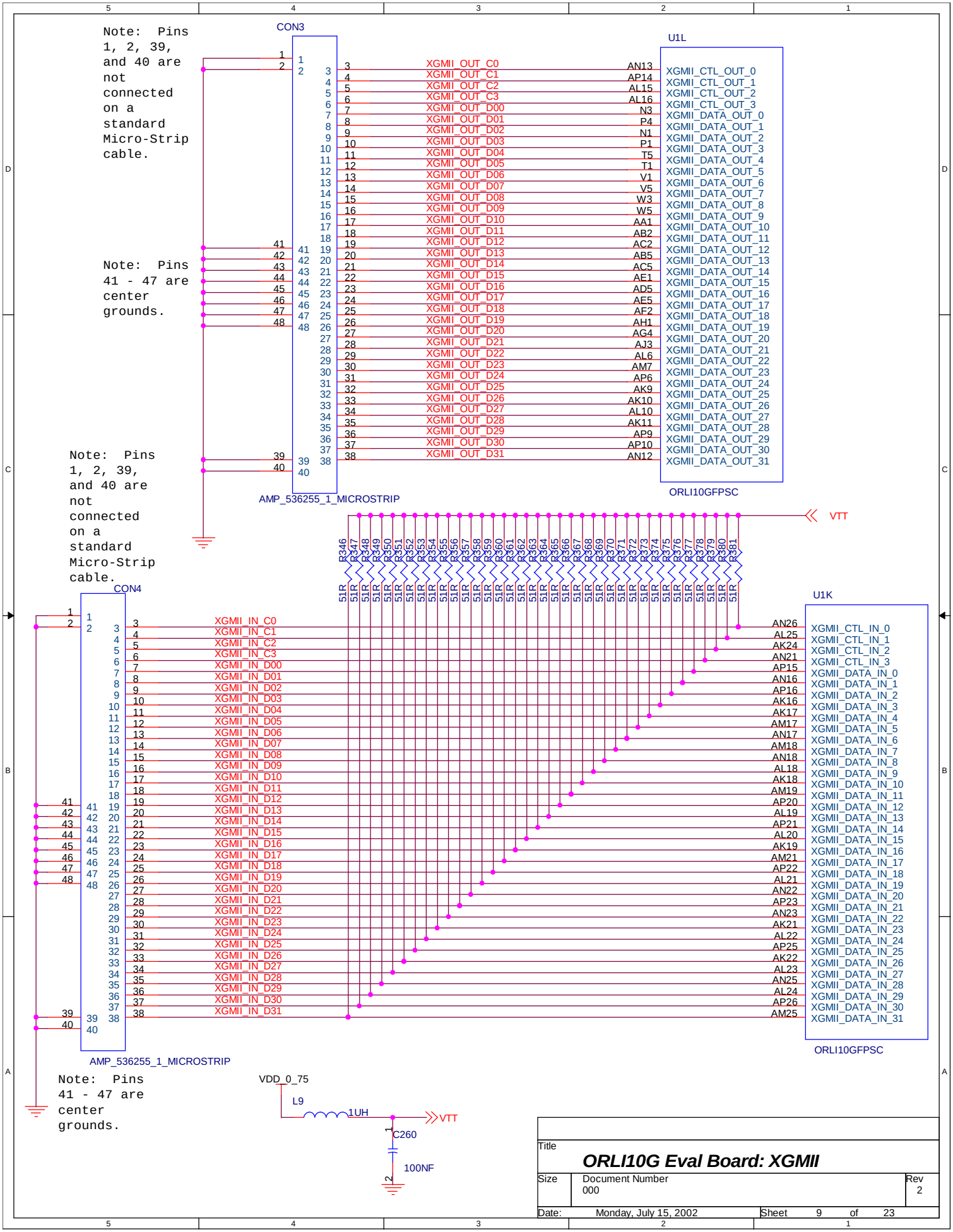


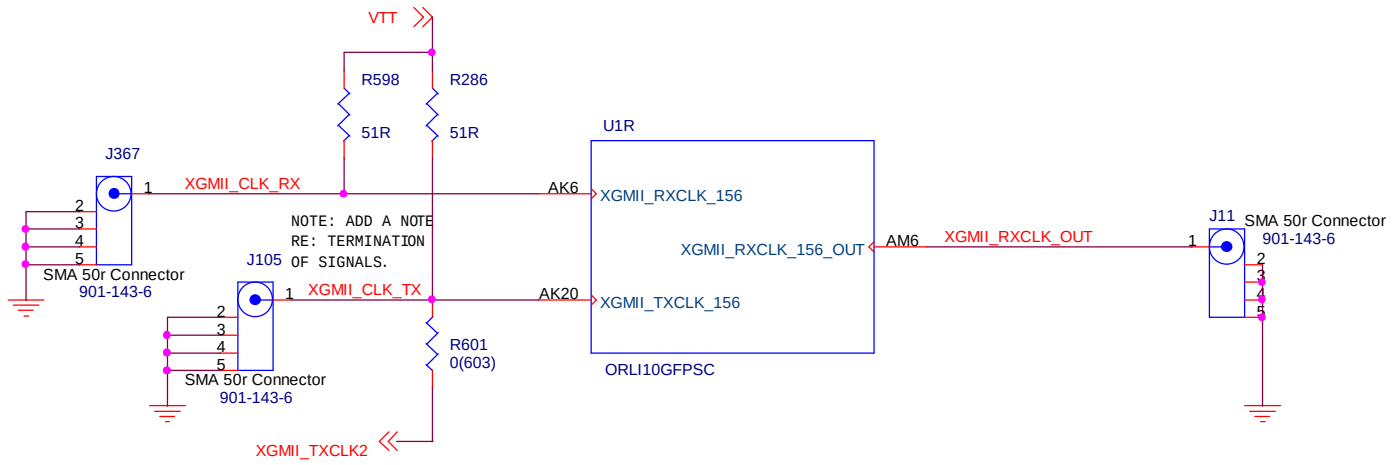
Title	**ORLI10G Eval Board: Extra I/O**	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 6 of 23	

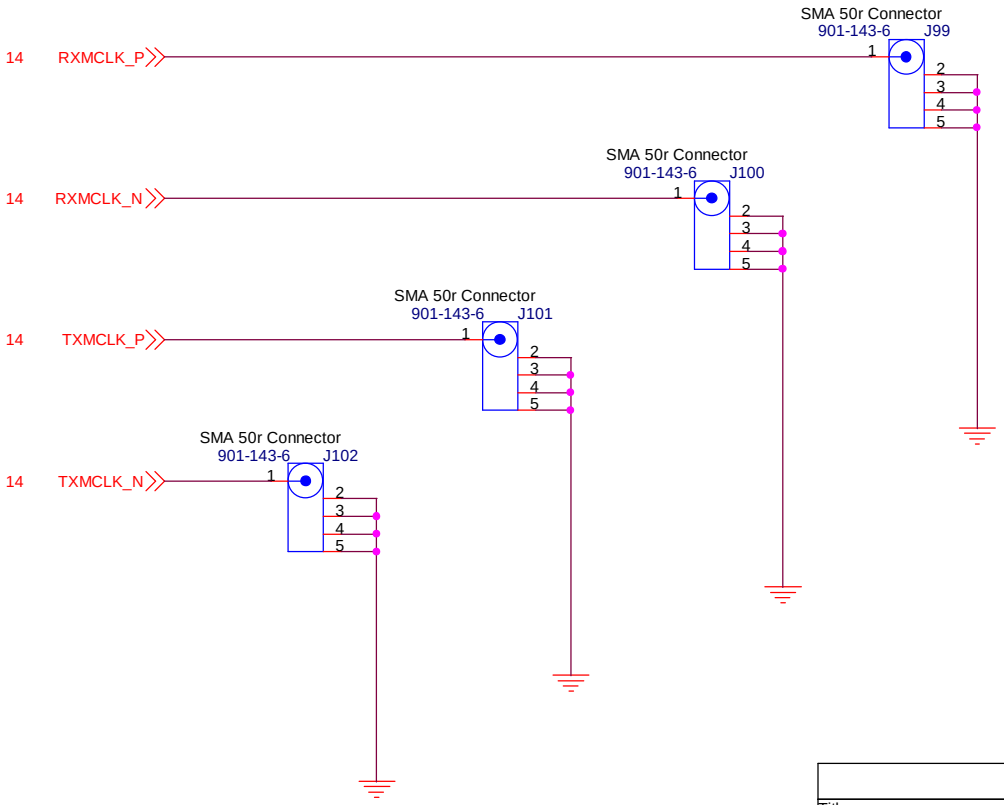

J6
TSW3X8
J7
TSW3X8
J8
TSW3X12
U1H
ORLI10GFPSC
U1J
ORLI10GFPSC
U1G
ORLI10GFPSC
U1I
ORLI10GFPSC
J9
TSW3X10
J10
TSW3X12
XGMII_TXCLK2
Title
ORLI10G Eval Board: Differential I/O
Size
Document Number
000
Rev
2
Date: Monday, July 15, 2002
Sheet 7 of 23



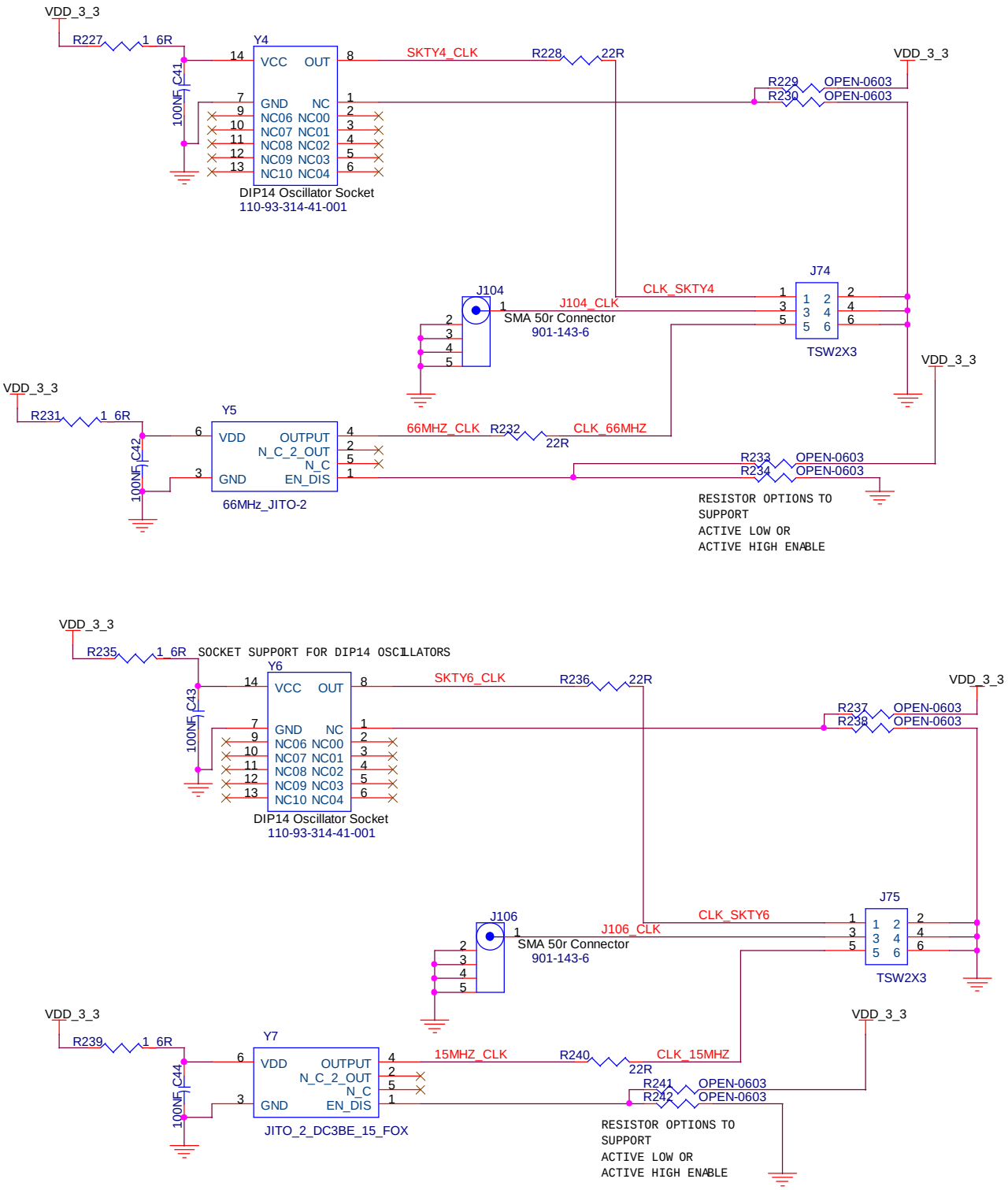
Title	***ORLI10G Eval Board: Center Tap***	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 8 of 23	


Note: Pins 1, 2, 39, and 40 are not connected on a standard Micro-Strip cable.
Note: Pins 41 - 47 are center grounds.
CON3
AMP_536255_1_MICROSTRIP
U1L
ORLI10GFPSC
XGMII_OUT_C0
XGMII_OUT_C1
XGMII_OUT_C2
XGMII_OUT_C3
XGMII_OUT_D00
XGMII_OUT_D01
XGMII_OUT_D02
XGMII_OUT_D03
XGMII_OUT_D04
XGMII_OUT_D05
XGMII_OUT_D06
XGMII_OUT_D07
XGMII_OUT_D08
XGMII_OUT_D09
XGMII_OUT_D10
XGMII_OUT_D11
XGMII_OUT_D12
XGMII_OUT_D13
XGMII_OUT_D14
XGMII_OUT_D15
XGMII_OUT_D16
XGMII_OUT_D17
XGMII_OUT_D18
XGMII_OUT_D19
XGMII_OUT_D20
XGMII_OUT_D21
XGMII_OUT_D22
XGMII_OUT_D23
XGMII_OUT_D24
XGMII_OUT_D25
XGMII_OUT_D26
XGMII_OUT_D27
XGMII_OUT_D28
XGMII_OUT_D29
XGMII_OUT_D30
XGMII_OUT_D31
AN13
AP14
AL15
AL16
N3
P4
N1
P1
T5
T1
V1
V5
W3
W5
AA1
AB2
AC2
AB5
AC5
AE1
AD5
AE5
AF2
AH1
AG4
AJ3
AL6
AM7
AP6
AK9
AK10
AL10
AK11
AP9
AP10
AN12
XGMII_CTL_OUT_0
XGMII_CTL_OUT_1
XGMII_CTL_OUT_2
XGMII_CTL_OUT_3
XGMII_DATA_OUT_0
XGMII_DATA_OUT_1
XGMII_DATA_OUT_2
XGMII_DATA_OUT_3
XGMII_DATA_OUT_4
XGMII_DATA_OUT_5
XGMII_DATA_OUT_6
XGMII_DATA_OUT_7
XGMII_DATA_OUT_8
XGMII_DATA_OUT_9
XGMII_DATA_OUT_10
XGMII_DATA_OUT_11
XGMII_DATA_OUT_12
XGMII_DATA_OUT_13
XGMII_DATA_OUT_14
XGMII_DATA_OUT_15
XGMII_DATA_OUT_16
XGMII_DATA_OUT_17
XGMII_DATA_OUT_18
XGMII_DATA_OUT_19
XGMII_DATA_OUT_20
XGMII_DATA_OUT_21
XGMII_DATA_OUT_22
XGMII_DATA_OUT_23
XGMII_DATA_OUT_24
XGMII_DATA_OUT_25
XGMII_DATA_OUT_26
XGMII_DATA_OUT_27
XGMII_DATA_OUT_28
XGMII_DATA_OUT_29
XGMII_DATA_OUT_30
XGMII_DATA_OUT_31
Note: Pins 1, 2, 39, and 40 are not connected on a standard Micro-Strip cable.
CON4
AMP_536255_1_MICROSTRIP
VTT
R346 R347 R348 R349 R350 R351 R352 R353 R354 R355 R356 R357 R358 R359 R360 R361 R362 R363 R364 R365 R366 R367 R368 R369 R370 R371 R372 R373 R374 R375 R376 R377 R378 R379 R380 R381
51R
U1K
ORLI10GFPSC
XGMII_IN_C0
XGMII_IN_C1
XGMII_IN_C2
XGMII_IN_C3
XGMII_IN_D00
XGMII_IN_D01
XGMII_IN_D02
XGMII_IN_D03
XGMII_IN_D04
XGMII_IN_D05
XGMII_IN_D06
XGMII_IN_D07
XGMII_IN_D08
XGMII_IN_D09
XGMII_IN_D10
XGMII_IN_D11
XGMII_IN_D12
XGMII_IN_D13
XGMII_IN_D14
XGMII_IN_D15
XGMII_IN_D16
XGMII_IN_D17
XGMII_IN_D18
XGMII_IN_D19
XGMII_IN_D20
XGMII_IN_D21
XGMII_IN_D22
XGMII_IN_D23
XGMII_IN_D24
XGMII_IN_D25
XGMII_IN_D26
XGMII_IN_D27
XGMII_IN_D28
XGMII_IN_D29
XGMII_IN_D30
XGMII_IN_D31
AN26
AL25
AK24
AN21
AP15
AN16
AP16
AK16
AK17
AM17
AN17
AM18
AN18
AL18
AK18
AM19
AP20
AL19
AP21
AL20
AK19
AM21
AP22
AL21
AN22
AP23
AN23
AK21
AL22
AP25
AK22
AL23
AN25
AL24
AP26
AM25
XGMII_CTL_IN_0
XGMII_CTL_IN_1
XGMII_CTL_IN_2
XGMII_CTL_IN_3
XGMII_DATA_IN_0
XGMII_DATA_IN_1
XGMII_DATA_IN_2
XGMII_DATA_IN_3
XGMII_DATA_IN_4
XGMII_DATA_IN_5
XGMII_DATA_IN_6
XGMII_DATA_IN_7
XGMII_DATA_IN_8
XGMII_DATA_IN_9
XGMII_DATA_IN_10
XGMII_DATA_IN_11
XGMII_DATA_IN_12
XGMII_DATA_IN_13
XGMII_DATA_IN_14
XGMII_DATA_IN_15
XGMII_DATA_IN_16
XGMII_DATA_IN_17
XGMII_DATA_IN_18
XGMII_DATA_IN_19
XGMII_DATA_IN_20
XGMII_DATA_IN_21
XGMII_DATA_IN_22
XGMII_DATA_IN_23
XGMII_DATA_IN_24
XGMII_DATA_IN_25
XGMII_DATA_IN_26
XGMII_DATA_IN_27
XGMII_DATA_IN_28
XGMII_DATA_IN_29
XGMII_DATA_IN_30
XGMII_DATA_IN_31
Note: Pins 41 - 47 are center grounds.
VDD_0_75
L9
1UH
VTT
C260
100NF
Title
ORLI10G Eval Board: XGMII
Size
Document Number
000
Rev
2
Date: Monday, July 15, 2002
Sheet 9 of 23

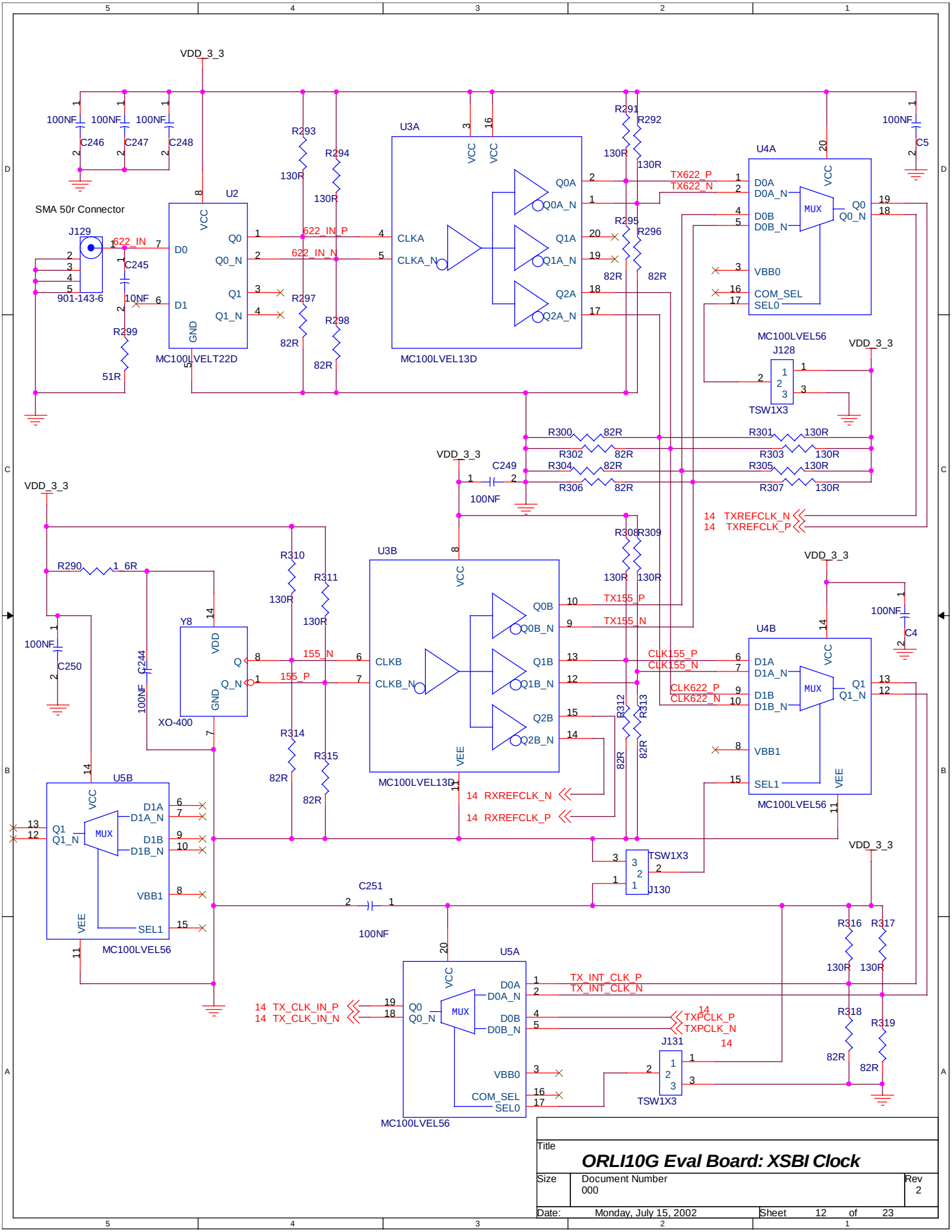


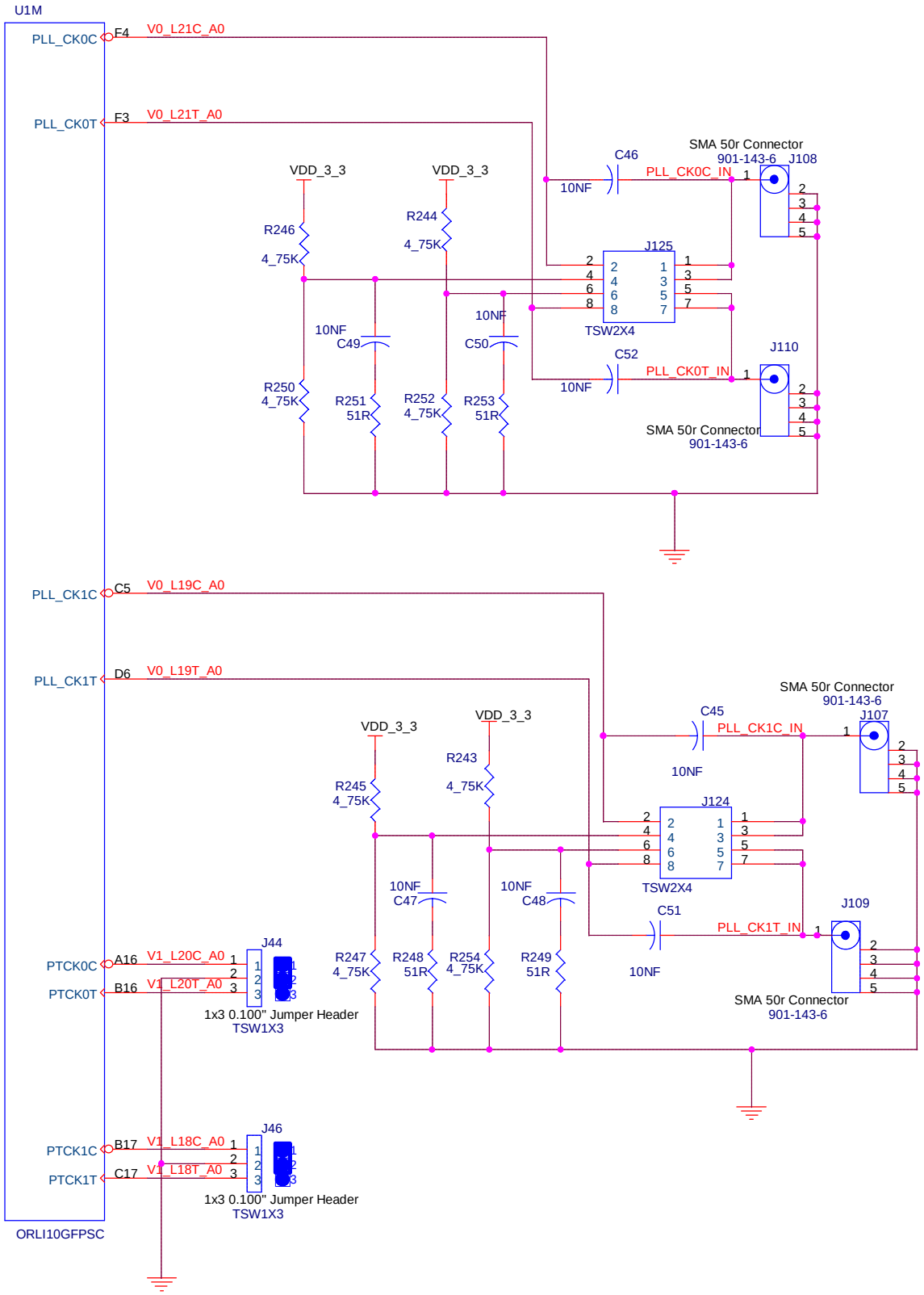


Title	***ORLI10G Eval Board: XGMII/XSBI Clock***	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 10 of 23	



Title	**ORLI10G Eval Board: Clock Sources**	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 11 of 23	


VDD_3_3
100NF
C246
C247
C248
R293
R294
130R
U3A
VCC
Q0A
Q0A_N
Q1A
Q1A_N
Q2A
Q2A_N
CLKA
CLKA_N
MC100LVEL13D
R291
R292
R295
R296
82R
U4A
MUX
D0A
D0A_N
D0B
D0B_N
Q0
Q0_N
VBB0
COM_SEL
SEL0
MC100LVEL56
TX622_P
TX622_N
C5
SMA 50r Connector
J129
901-143-6
622_IN
C245
10NF
U2
D0
D1
Q0
Q0_N
Q1
Q1_N
GND
MC100LVELT22D
622_IN_P
622_IN_N
R297
R298
R299
51R
J128
TSW1X3
R300
R301
R302
R303
R304
R305
R306
R307
C249
TXREFCLK_N
TXREFCLK_P
R290
1_6R
R308
R309
U3B
Q0B
Q0B_N
Q1B
Q1B_N
Q2B
Q2B_N
CLKB
CLKB_N
MC100LVEL13D
TX155_P
TX155_N
R310
R311
Y8
XO-400
155_N
155_P
C244
C250
U4B
CLK155_P
CLK155_N
CLK622_P
CLK622_N
R312
R313
R314
R315
RXREFCLK_N
RXREFCLK_P
U5B
MC100LVEL56
J130
C251
U5A
TX_CLK_IN_P
TX_CLK_IN_N
TX_INT_CLK_P
TX_INT_CLK_N
TXPCLK_P
TXPCLK_N
J131
R316
R317
R318
R319
Title
ORLI10G Eval Board: XSBI Clock
Size
Document Number
000
Rev
2
Date:
Monday, July 15, 2002
Sheet
12
of
23

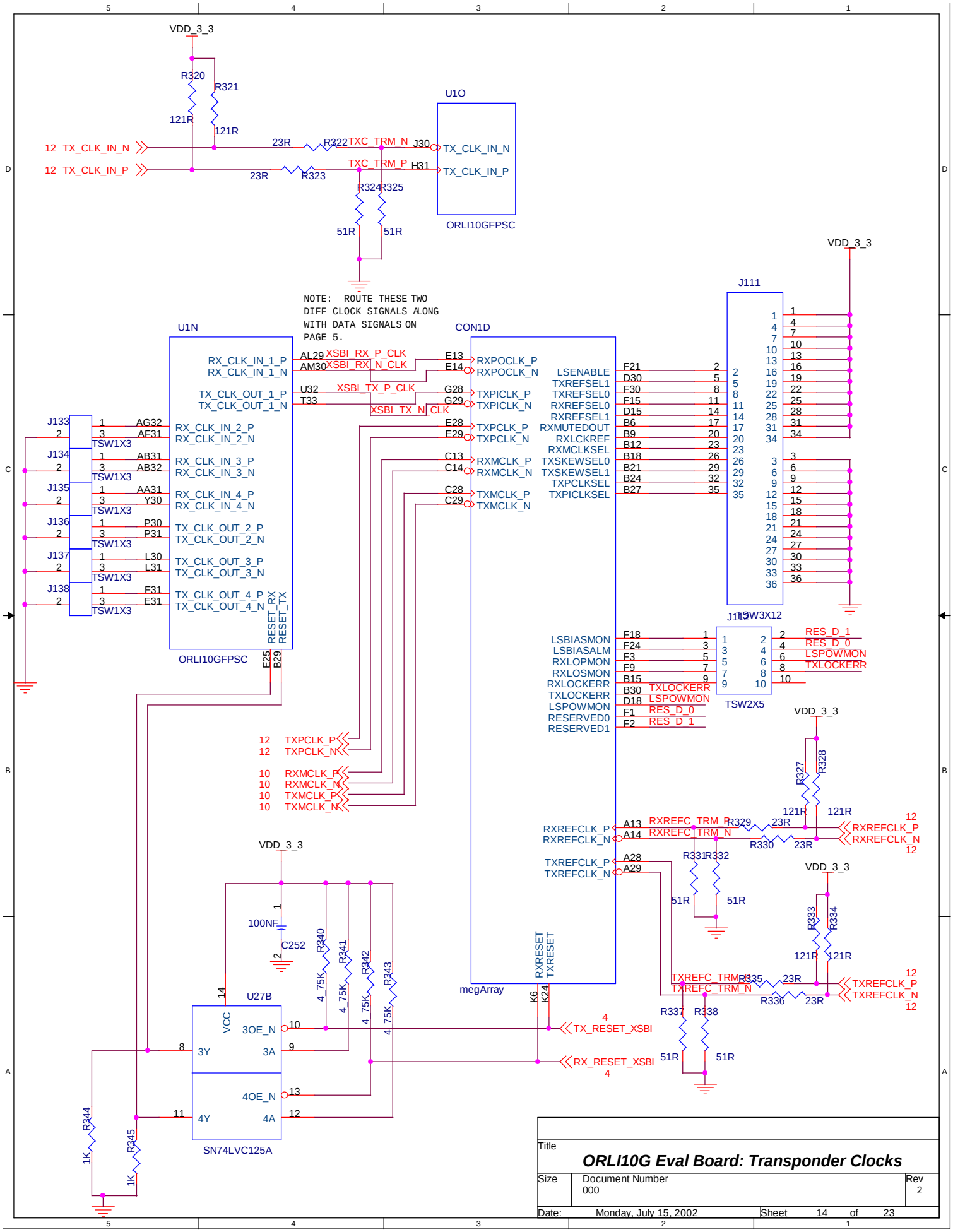


Title

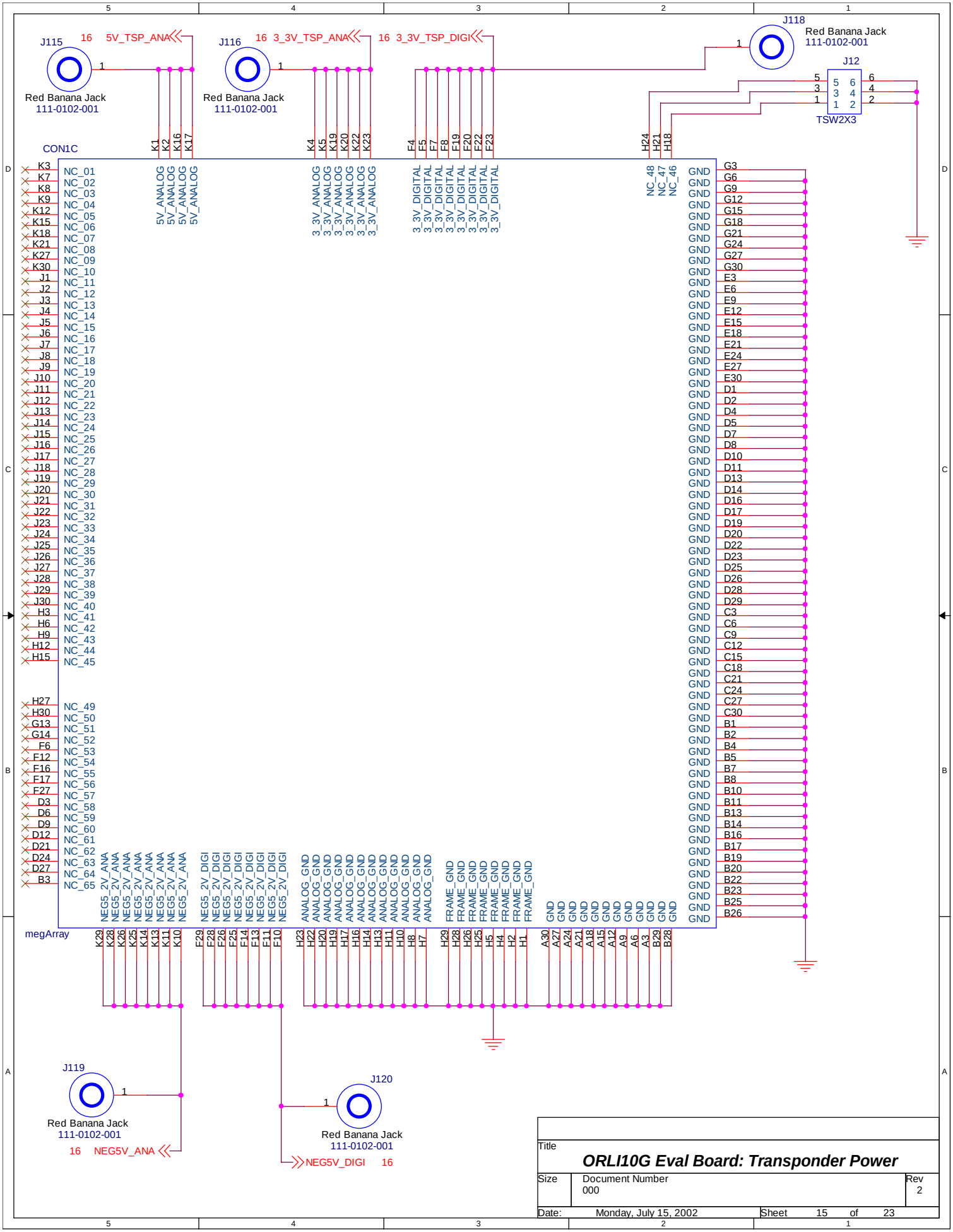
ORLI10G Eval Board: PLL Clock

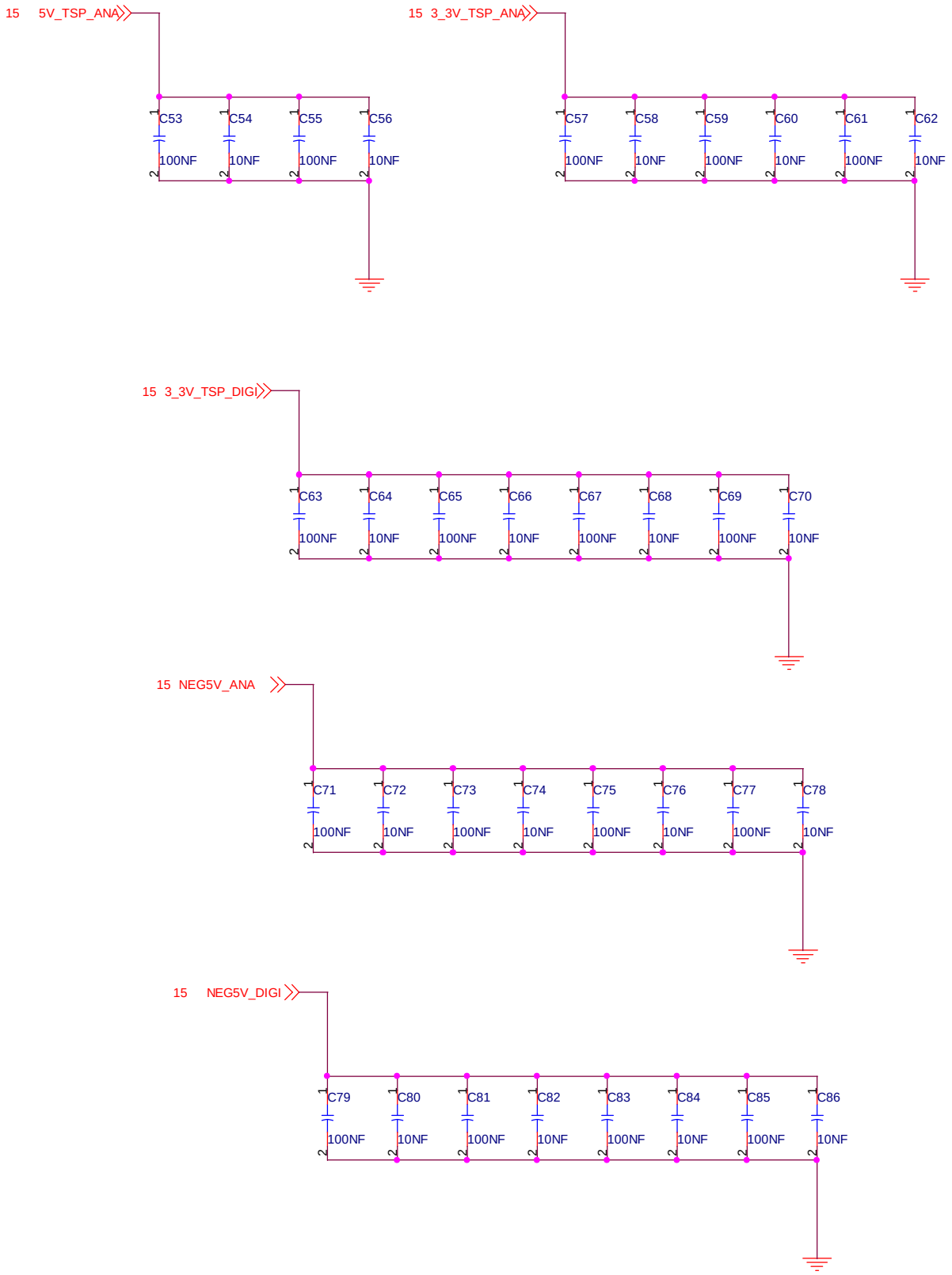
Size	Document Number	Rev
	000	2

Date: Monday, July 15, 2002 Sheet 13 of 23

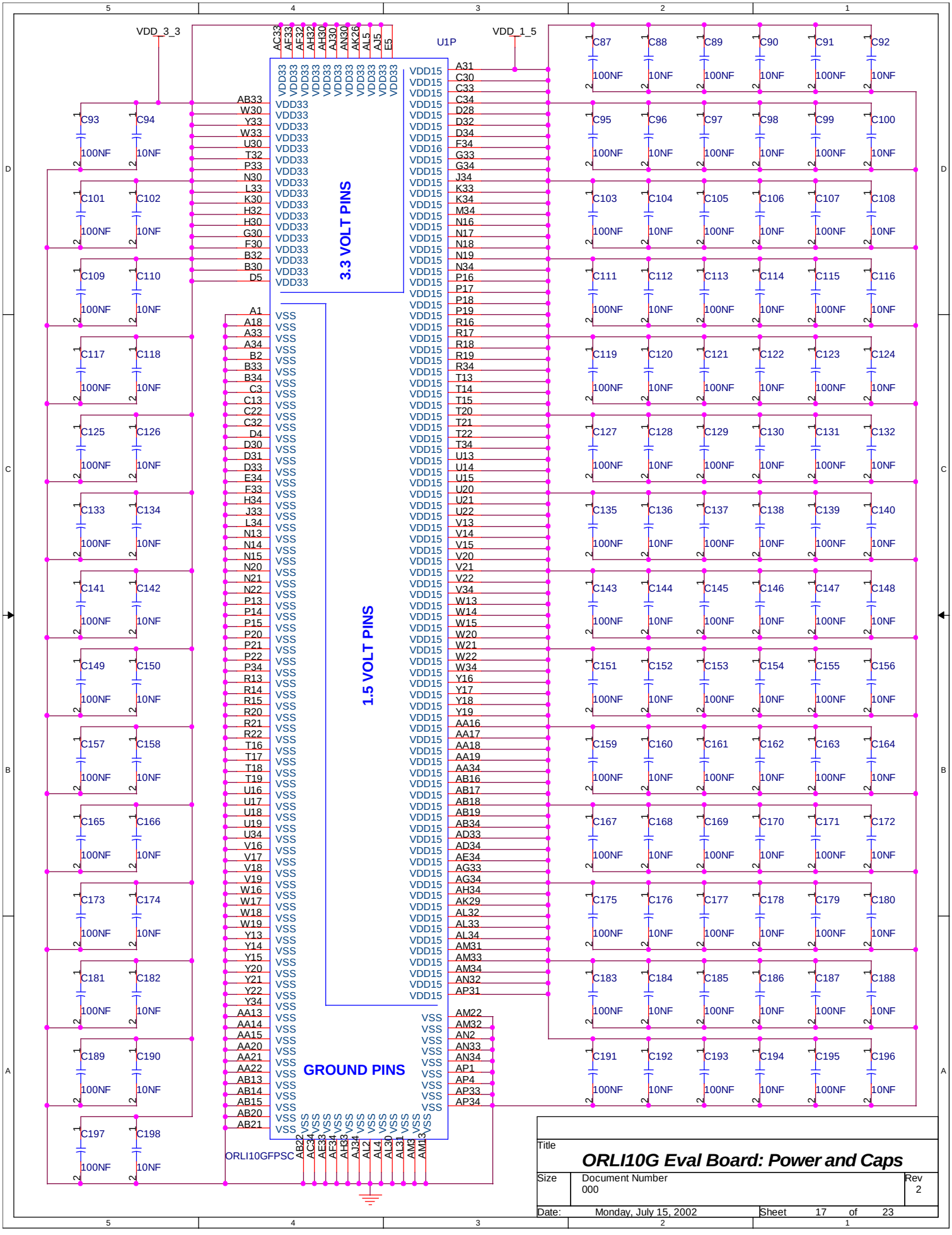


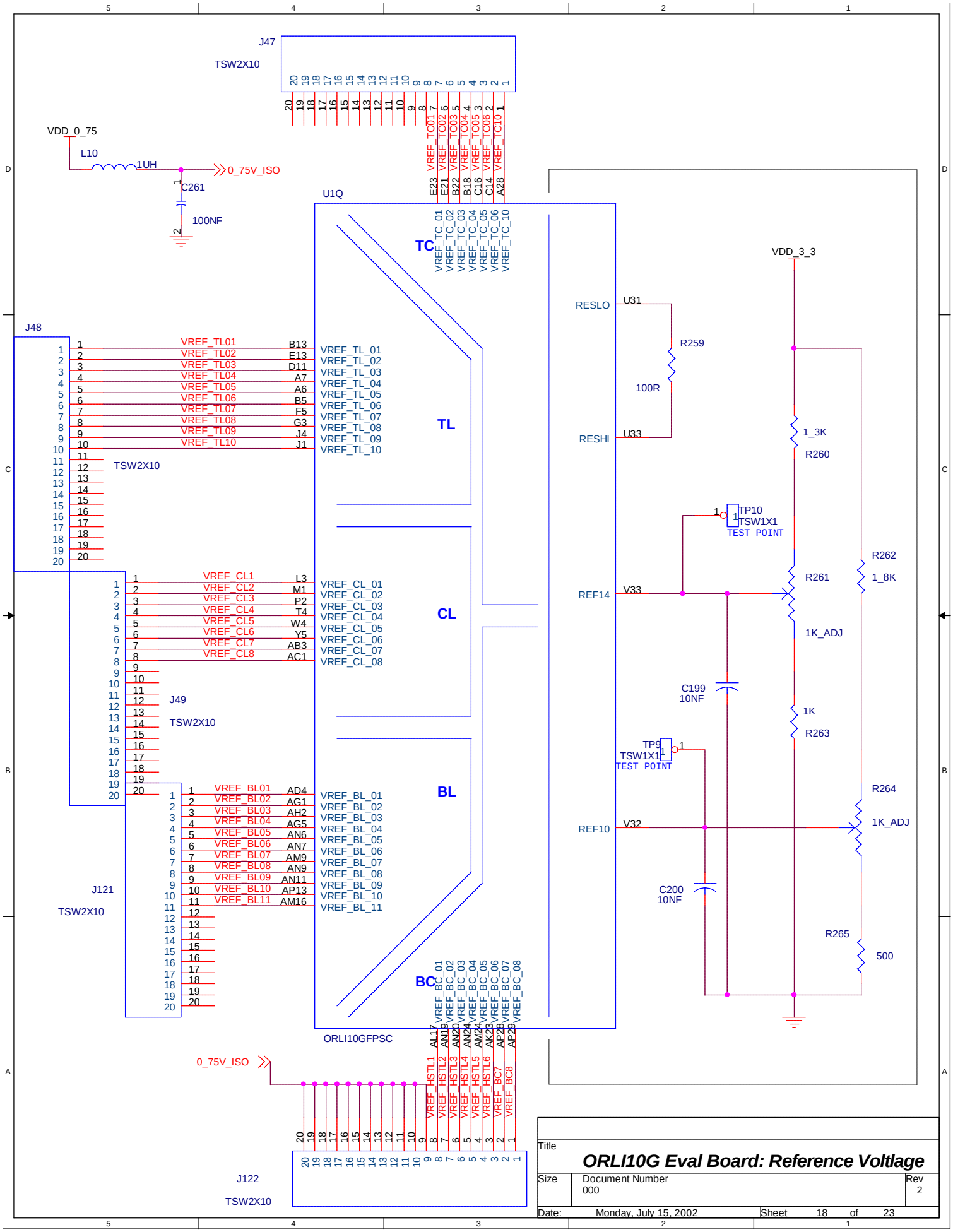
Title	**ORLI10G Eval Board: Transponder Clocks**	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 14 of 23	


J115
16 5V_TSP_ANA
Red Banana Jack
111-0102-001
J116
16 3_3V_TSP_ANA
16 3_3V_TSP_DIGI
Red Banana Jack
111-0102-001
J118
Red Banana Jack
111-0102-001
J12
TSW2X3
CON1C
megArray
J119
Red Banana Jack
111-0102-001
16 NEG5V_ANA
J120
Red Banana Jack
111-0102-001
NEG5V_DIGI 16
Title
ORLI10G Eval Board: Transponder Power
Size
Document Number
000
Rev
2
Date: Monday, July 15, 2002
Sheet 15 of 23



Title	**ORLI10G Eval Board: Bypass Caps**	
Size	Document Number 000	Rev 2
Date: Monday, July 15, 2002	Sheet 16 of 23	


VDD_3_3
VDD_1_5
U1P
3.3 VOLT PINS
1.5 VOLT PINS
GROUND PINS
ORLI10GFPSC
100NF
Title
ORLI10G Eval Board: Power and Caps
Size
Document Number
000
Rev
2
Date: Monday, July 15, 2002
Sheet 17 of 23


J47
TSW2X10
VDD_0_75
L10
1UH
0_75V_ISO
C261
100NF
U1Q
TC
TL
CL
BL
BC
ORLI10GFPSC
J48
TSW2X10
J49
TSW2X10
J121
TSW2X10
J122
TSW2X10
VDD_3_3
RESLO
U31
R259
100R
RESHI
U33
1_3K
R260
TP10
TSW1X1
TEST POINT
R262
1_8K
R261
REF14
V33
1K_ADJ
C199
10NF
1K
R263
TP9
TSW1X1
TEST POINT
R264
1K_ADJ
REF10
V32
C200
10NF
R265
500
Title
ORLI10G Eval Board: Reference Voltlage
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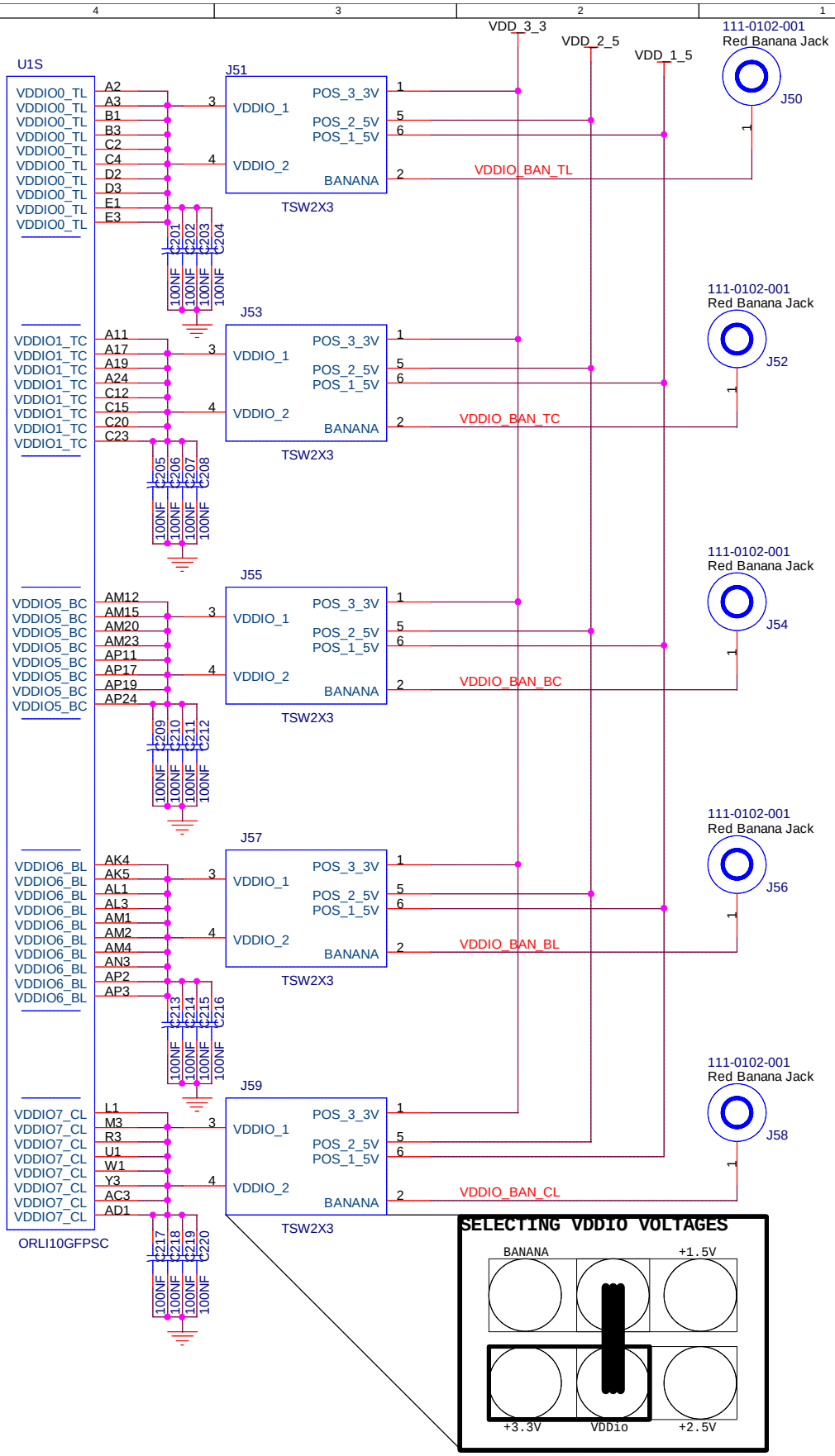

Title	**ORLI10G Eval Board: VDD I/O Selection**	
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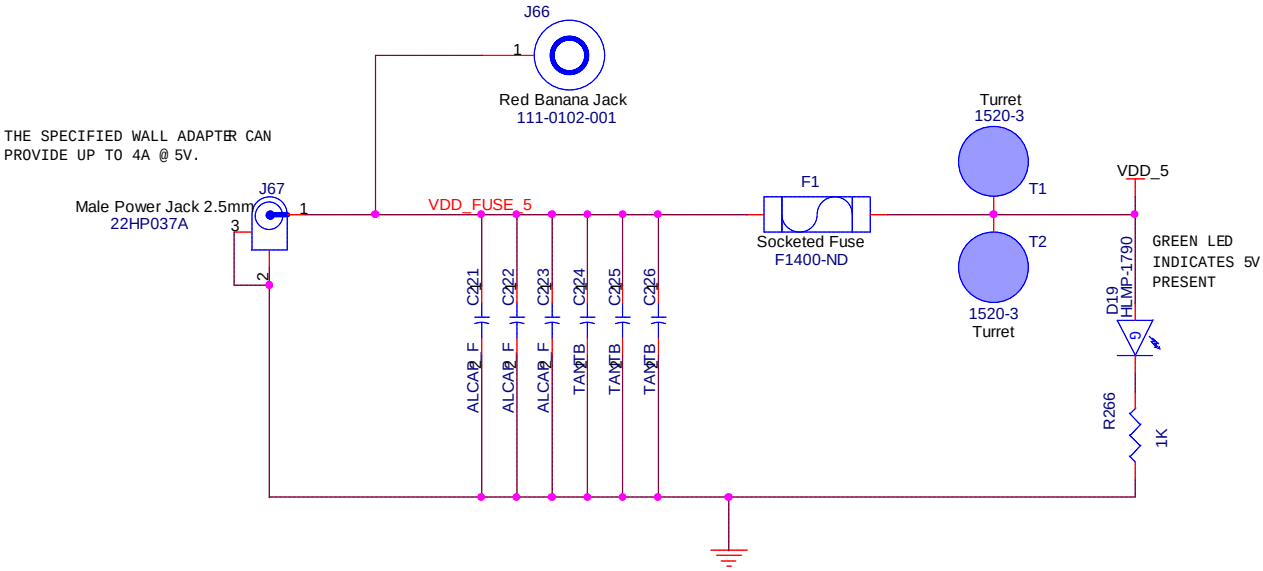

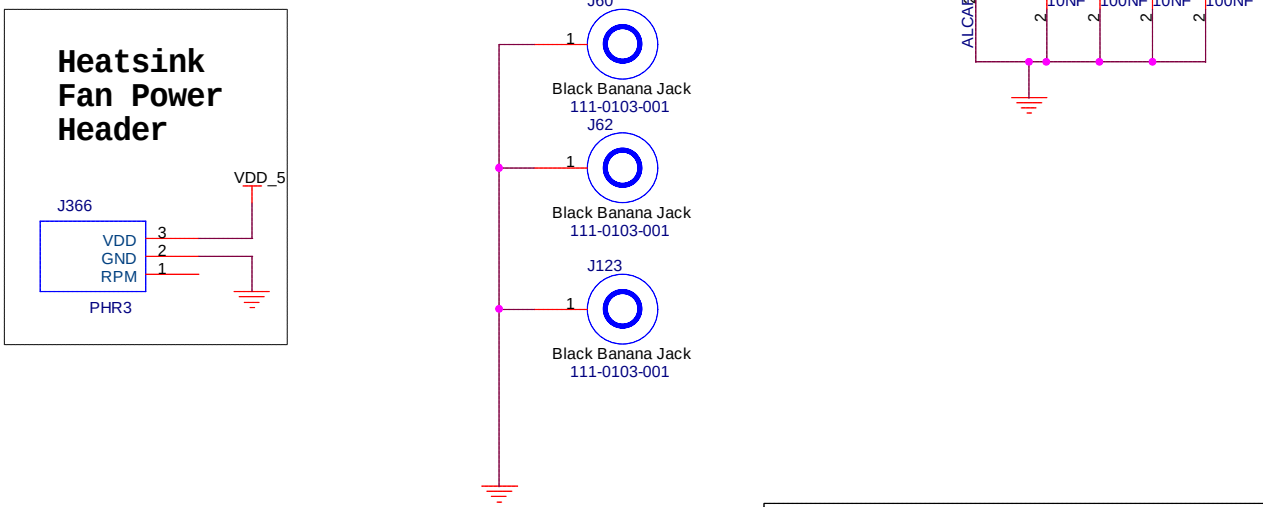

Title	***ORLI10G Eval Board: Power Generation 1***	
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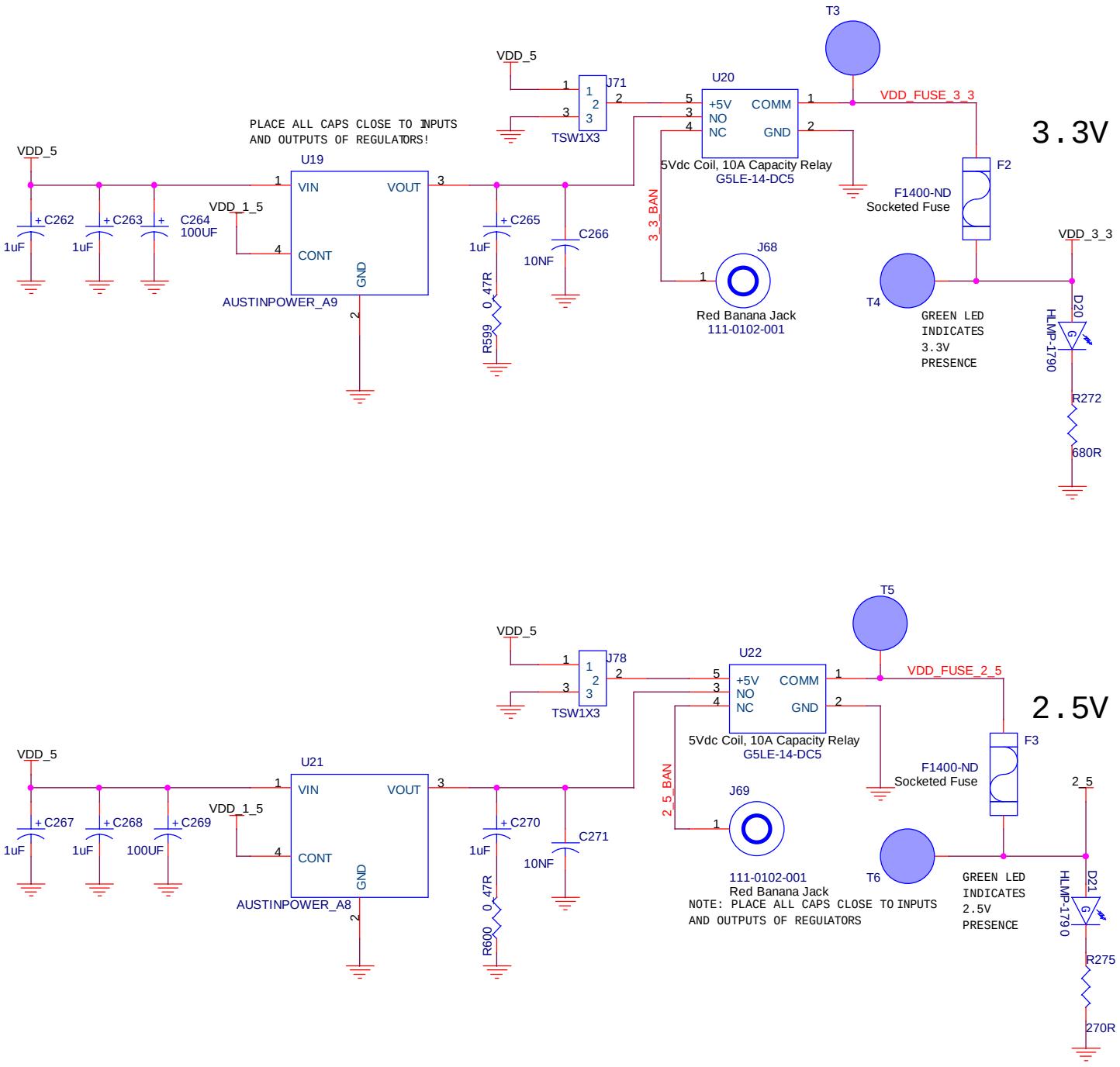

Title	**ORLI10G Eval Board: Power Gen 2**	
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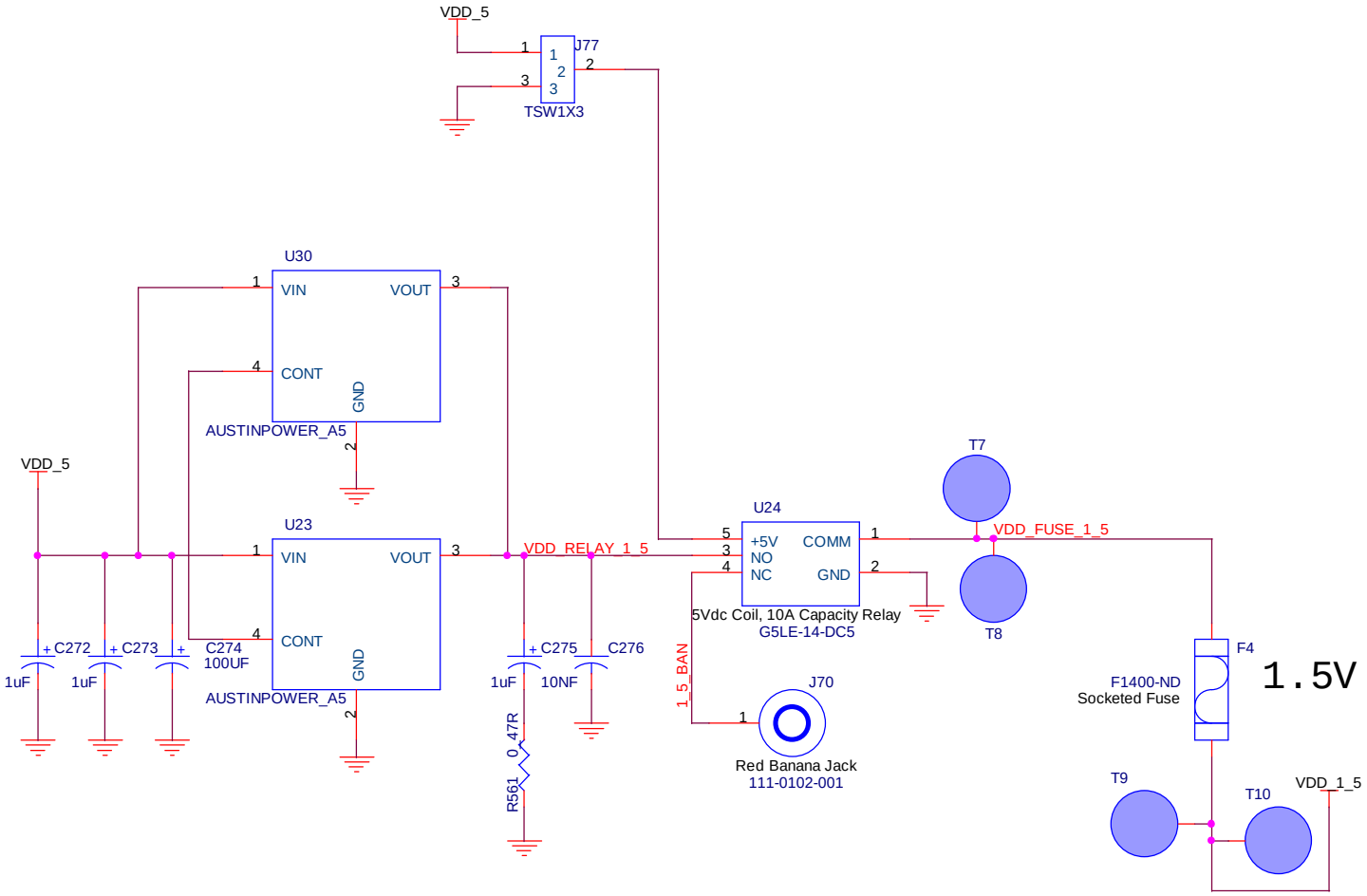

Title	**ORLI10G Eval Board: Power Gen 3**	
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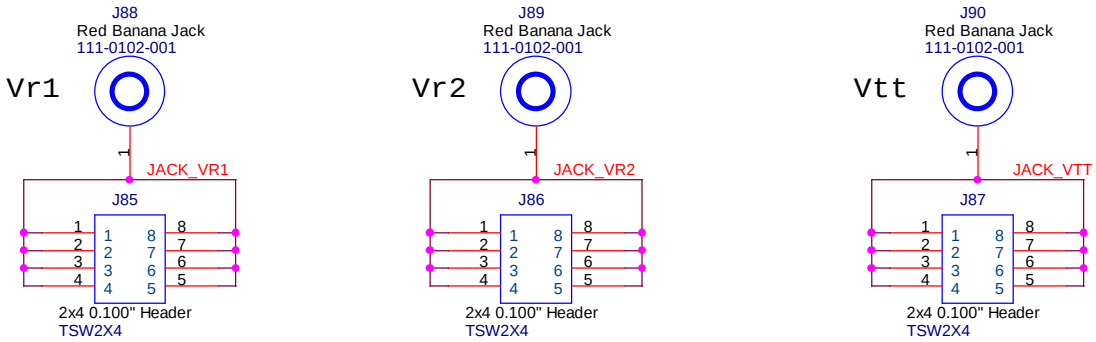
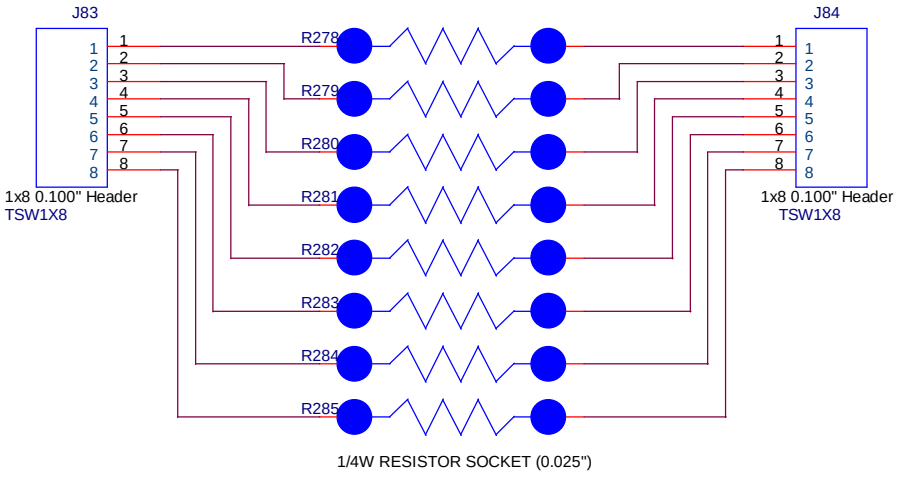
GENERAL PURPOSE BANANAS



RESISTOR SOCKETS



Title	***ORLI10G: Resistor Sockets***	
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