ISL1557

xDSL Differential Line Driver

FN7522
Rev.5.00
Nov 7, 2019

The ISL1557 is a dual operational amplifier designed for VDSL2 and ADSL line driving in DMT based solutions. This device features a high drive capability of 750mA while consuming only 6mA of supply current per amplifier and operating from a single 4.5V to 12V supply. The driver achieves a typical distortion of -80dBc at 150kHz into a 25Ω load.

The ISL1557 is available in the thermally-enhanced 16 Ld QFN and 10 Ld HMSOP package and is specified for operation across -40°C to +85°C (IRZ, IUEZ) or -40°C to +125°C (FRZ) temperature ranges. The ISL1557 has control pins C0 and C1 for controlling the bias and enable/disable of the outputs. These controls allow for lowering the power to fit the performance/power ratio for the application.

The ISL1557 is ideal for ADSL2+, SDSL, HDSL2, and VDSL line driving applications, including both 14.5dBm and 21dBm applications.

Related Literature

For a full list of related documents, visit our website

- ISL1557 product page

Features

- Full-range industrial temperature (FRZ only): -40°C to +125°C
- 21dBm output power capability
- Drives up to 750mA from a +12V supply
- $20V_{P-P}$ differential output drive into 21Ω
- -80dBc typical driver output distortion at full output at 150kHz
- -75dBc typical driver output distortion at 4MHz
- -71dBc typical driver output distortion at 10MHz
- -75dBc typical driver output distortion at 17MHz
- Low quiescent current of 6mA per amplifier
- Supply range
  - ISL1557IRZ, ISL1557FRZ. . . . ±2.25V to ±6V, 4.5V to 12V
  - ISL1557IUEZ. . . . . 4.5V to 12V
- 300MHz bandwidth
- Thermal shutdown
- Pb-free (RoHS compliant)

Applications

- VDSL2 line drivers
- Power line communications line drivers
- ADSL2+ CPE line driving
- G.SHDSL and HDSL2 line drivers

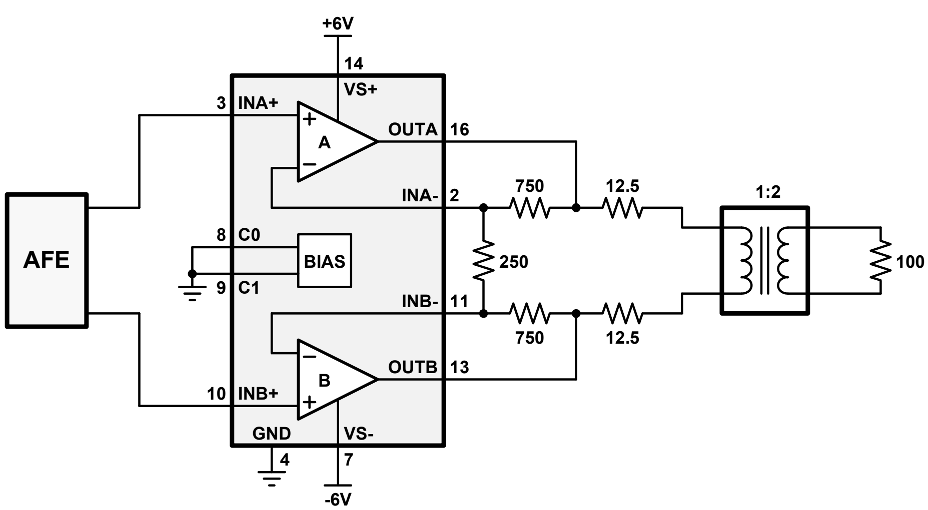


FIGURE 1. TYPICAL OPERATING CIRCUIT

Ordering Information

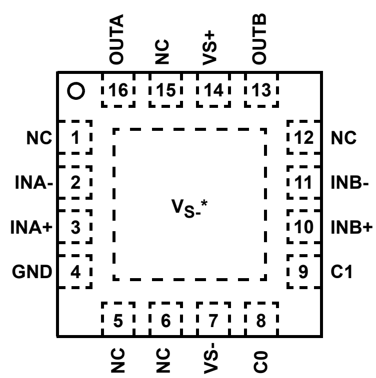
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL1557FRZ	155 7FRZ	-40 to +125	-	16 Ld 4x4 QFN	L16.4x4H
ISL1557FRZ-T7	155 7FRZ	-40 to +125	1k	16 Ld 4x4 QFN	L16.4x4H
ISL1557IRZ	155 7IRZ	-40 to +85	-	16 Ld 4x4 QFN	L16.4x4H
ISL1557IRZ-T7	155 7IRZ	-40 to +85	1k	16 Ld 4x4 QFN	L16.4x4H
ISL1557IUEZ	BBVAA	-40 to +85	-	10 Ld HMSOP	M10.118B
ISL1557IUEZ-T7	BBVAA	-40 to +85	1.5k	10 Ld HMSOP	M10.118B
ISL1557IRZ-EVAL	Evaluation Board				

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL1557 product information page. For more information about MSL, refer to TB363.

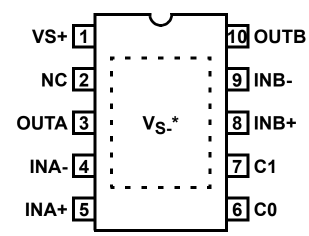
Pin Configurations

ISL1557
(16 LD QFN)
TOP VIEW



*THERMAL PAD MUST BE CONNECTED TO NEGATIVE SUPPLY: V_{S-}.
QFN PACKAGE CAN BE USED IN SINGLE AND DUAL SUPPLY APPLICATIONS.

ISL1557
(10 LD HMSOP)
TOP VIEW



*THERMAL PAD MUST BE CONNECTED TO NEGATIVE SUPPLY: V_{S-}.
HMSOP PACKAGE CAN BE USED IN SINGLE SUPPLY APPLICATIONS ONLY.

Pin Descriptions

16 LD QFN (Note 4)	10 LD HMSOP (Note 5)	PIN NAME	FUNCTION
1, 5, 6, 12, 15	2	NC	No Connect
2	4	INA-	Inverting Input of Amplifier A
3	5	INA+	Non-Inverting Input of Amplifier A
4	-	GND	Ground Connect
7	-	VS-	Negative Supply
8	6	CO	Bias Control Pin 0
9	7	C1	Bias Control Pin 1
10	8	INB+	Non-Inverting Input of Amplifier B
11	9	INB-	Inverting Input of Amplifier B
13	10	OUTB	Output of Amplifier B
14	1	VS+	Positive Supply
16	3	OUTA	Output of Amplifier A

NOTE:

4. Thermal pad must be connected to negative supply: V_{S-}. QFN package can be used in single and dual supply applications.
5. Thermal pad must be connected to negative supply: V_{S-}. HMSOP package can be used in single supply applications only.

TABLE 1. BIAS MODE CONTROL

CONTROL INPUTS		BIAS MODES	TYPICAL SUPPLY CURRENT PER AMPLIFIER (mA)
CO (V)	C1 (V)		
0	0	Full	15
0	5	Medium	11
5	0	Low	6.0
5	5	Power Down	0.6

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Voltage to Ground . . . . -0.3V to +13.2V
V_{IN}+ Voltage . . . . GND to V_S+
Current into any Input 8mA
Continuous Output Current 75mA
C0, C1 to Ground . . . . +6.6V
ESD Rating
Human Body Model 3kV
Machine Model 250V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld HMSOP Package (Notes 6, 7)	62	14
16 Ld QFN Package (Notes 6, 7)	52	14

Ambient Operating Temperature Range
ISL1557FRZ . . . . -40°C to +125°C
ISL1557IRZ, ISL1557IUEZ . . . . -40°C to +85°C
Storage Temperature Range . . . . -60°C to +150°C
Operating Junction Temperature . . . . +150°C
Power Dissipation . . . . See Figure 24 on page 9
Pb-Free reflow profile . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_S = 12V, R_F = 750Ω, $R_{L\text{-}DIFF}$ = 50Ω, T_A = +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
AC PERFORMANCE						
-3dB Bandwidth	BW	R_F = 499Ω, A_V = +5		300		MHz
		R_F = 750Ω, A_V = +5		250		MHz
		R_F = 750Ω, A_V = +10		200		MHz
Total Harmonic Distortion, Differential	THD	f = 200kHz, V_O = 16$V_{P\text{-}P}$, $R_{L\text{-}DIFF}$ = 100Ω	-72	-83		dBc
		f = 4MHz, V_O = 2$V_{P\text{-}P}$, $R_{L\text{-}DIFF}$ = 100Ω		-75		dBc
		f = 10MHz, V_O = 2$V_{P\text{-}P}$, $R_{L\text{-}DIFF}$ = 100Ω		-71		dBc
		f = 17MHz, V_O = 2$V_{P\text{-}P}$, $R_{L\text{-}DIFF}$ = 100Ω		-75		dBc
Slew Rate, Single-Ended	SR	V_{OUT} from -3V to +3V	750	1200		V/µs
DC PERFORMANCE						
Offset Voltage Common-Mode	V_{OS_CM}		-40		+40	mV
Offset Voltage Differential Mode	V_{OS_DM}		-7.5		+7.5	mV
Differential Transimpedance	R_{OL}	V_{OUT} = 12$V_{P\text{-}P}$ differential, unloaded		3.0		MΩ
INPUT CHARACTERISTICS						
Non-Inverting Input Bias Current	I_B+		-7.0		+7.0	µA
Inverting Input Bias Current Differential Mode	I_{B^-} DM		-75	3	+75	µA
Input Noise Voltage	e_N			6		nV/√Hz
-Input Noise Current	i_N			13		pA/√Hz
OUTPUT CHARACTERISTICS						
Loaded Output Swing (Single-Ended)	V_{OUT}	V_S = ±6V, $R_{L\ DIFF}$ = 50Ω (FRZ)	±4.75	±5.0		V
		V_S = ±6V, $R_{L\ DIFF}$ = 20Ω (FRZ)	±4.20	±4.7		V
		V_S = ±6V, $R_{L\ DIFF}$ = 50Ω (IRZ, IUEZ)	±4.85	±5.0		V
		V_S = ±6V, $R_{L\ DIFF}$ = 20Ω (IRZ, IUEZ)	±4.4	±4.7		V
Output Current	I_{OUT}	R_L = 0Ω		1000		mA

Electrical Specifications (Continued) V_S = 12V, R_F = 750Ω, R_{L-DIFF} = 50Ω, T_A = +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
SUPPLY						
Supply Voltage	V_S	Single supply	4.5		13.2	V
Positive Supply Current per Amplifier	I_S+ (Full Bias)	All outputs at 0V, C_0 = C_1 = 0V	13	15	19	mA
Positive Supply Current per Amplifier	I_S+ (Medium Bias)	All outputs at 0V, C_0 = 5V, C_1 = 0V		11		mA
Positive Supply Current per Amplifier	I_S+ (Low Bias)	All outputs at 0V, C_0 = 0V, C_1 = 5V		6.0		mA
Positive Supply Current per Amplifier	I_S+ (Power-down)	All outputs at 0V, C_0 = C_1 = 5V		0.6	1.0	mA
C_0, C_1 Input Current, High	I_{INH}, C_0 or C_1	C_0, C_1 = 6V	100	175	250	µA
C_0, C_1 Input Current, Low	I_{INL}, C_0 or C_1	C_0, C_1 = 0V	-5		+5	µA
C_0, C_1 Input Voltage, High	V_{INH}, C_0 or C_1		2.0			V
C_0, C_1 Input Voltage, Low	V_{INL}, C_0 or C_1				0.8	V

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Typical Performance Curves

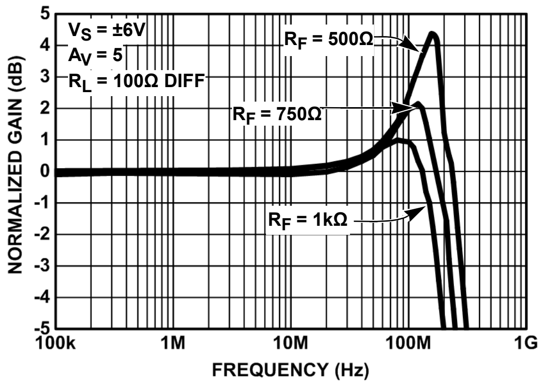


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (FULL BIAS MODE)

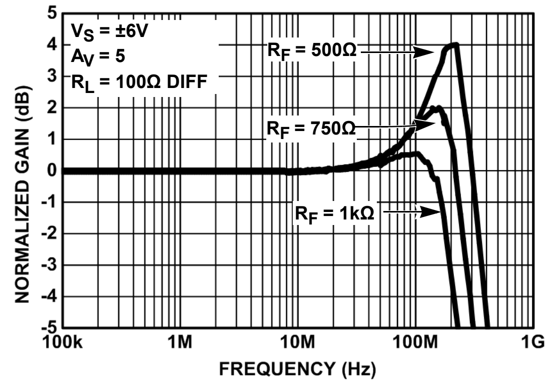


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (MEDIUM BIAS MODE)

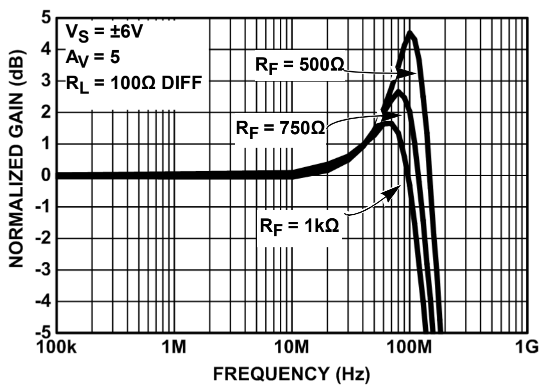


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (LOW BIAS MODE)

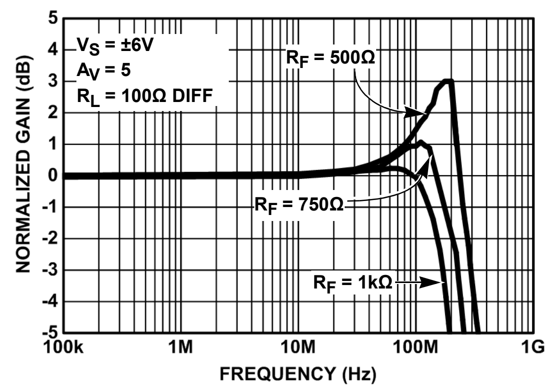


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (FULL BIAS MODE)

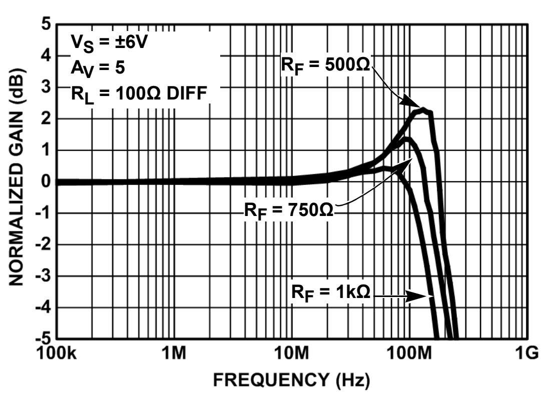


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (MEDIUM BIAS MODE)

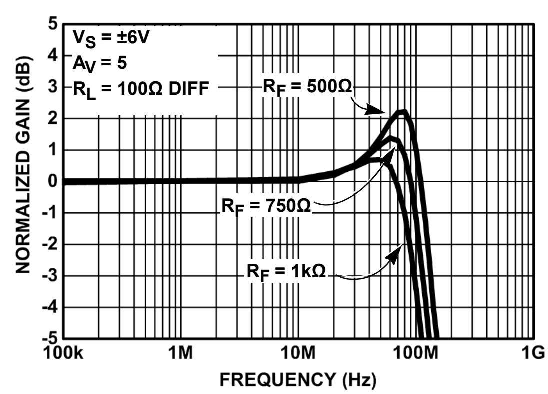


FIGURE 7. DIFFERENTIAL FREQUENCY RESPONSE WITH VARIOUS R_F (LOW BIAS MODE)

Typical Performance Curves (Continued)

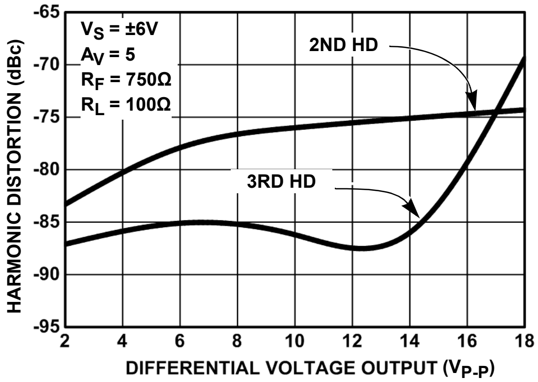


FIGURE 8. HARMONIC DISTORTION AT 2MHz

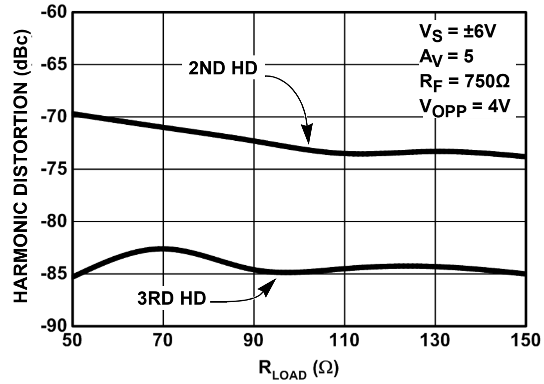


FIGURE 9. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} AT 2MHz

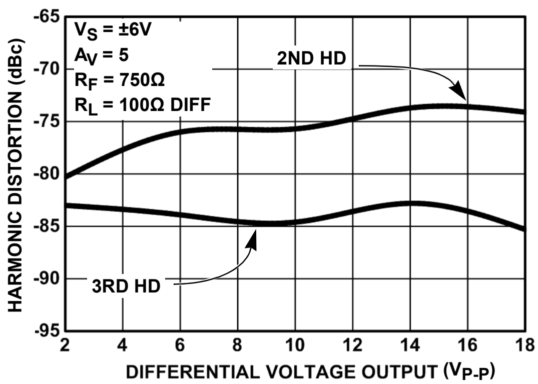


FIGURE 10. HARMONIC DISTORTION AT 3MHz

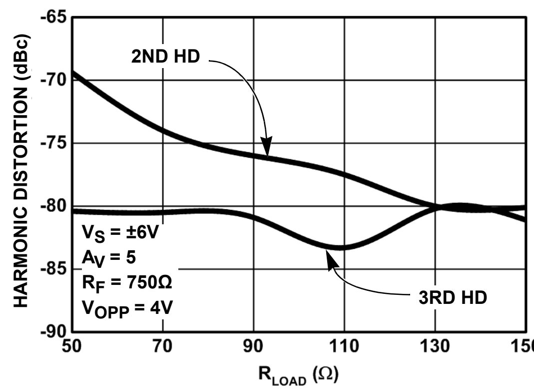


FIGURE 11. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} AT 3MHz

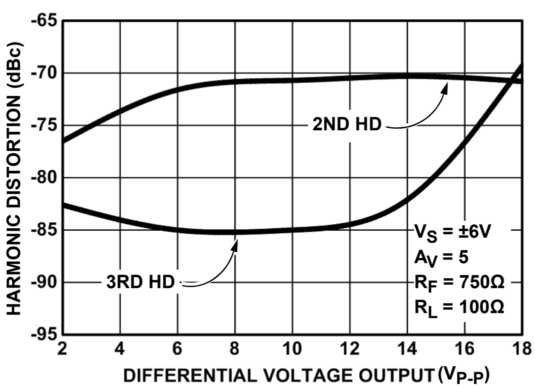


FIGURE 12. HARMONIC DISTORTION AT 5MHz

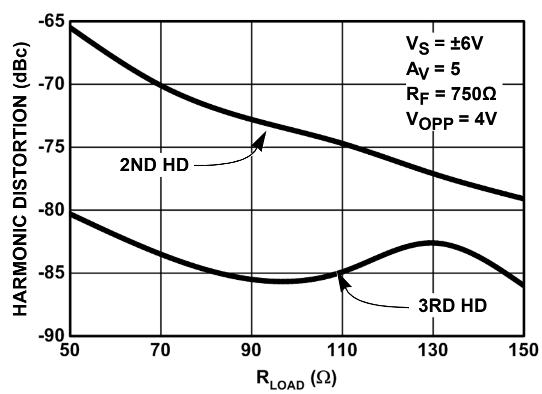


FIGURE 13. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} AT 5MHz

Typical Performance Curves (Continued)

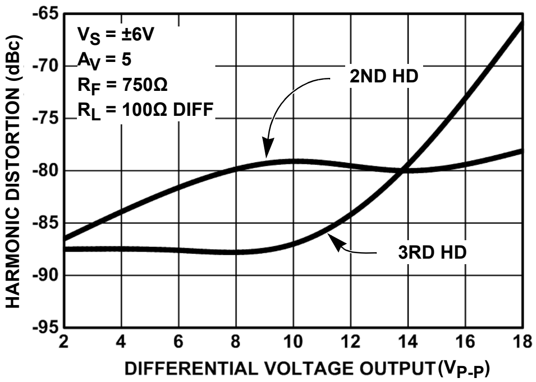


FIGURE 14. HARMONIC DISTORTION AT 10MHz

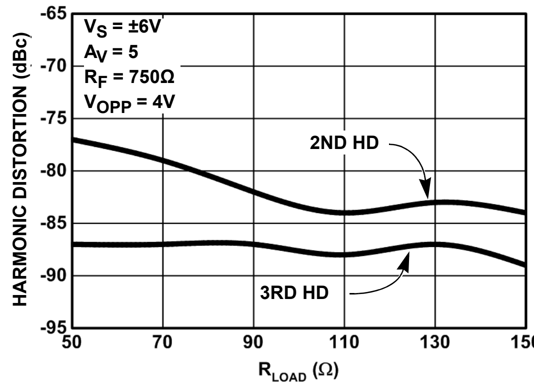


FIGURE 15. 2ND AND 3RD HARMONIC DISTORTION vs R_{LOAD} AT 10MHz

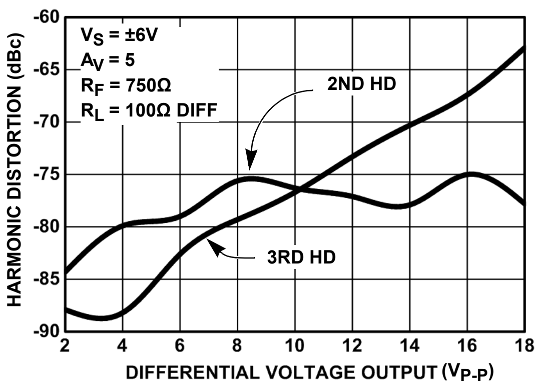


FIGURE 16. HARMONIC DISTORTION AT 17MHz

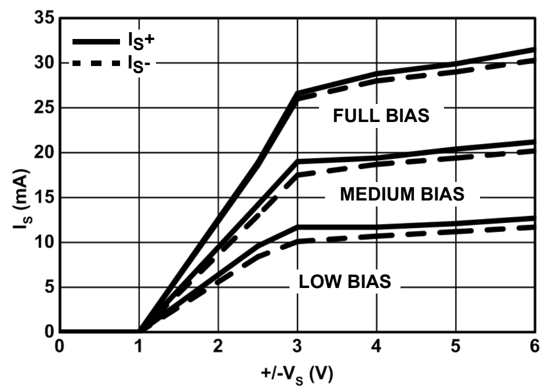


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

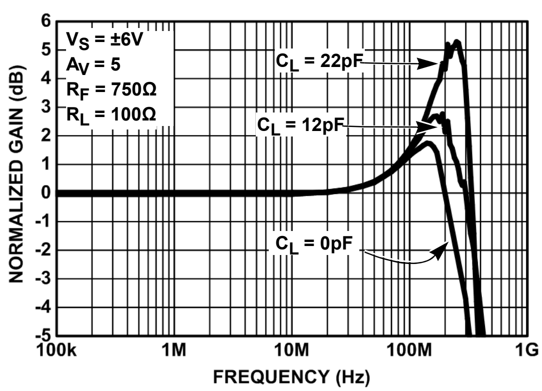


FIGURE 18. FREQUENCY RESPONSE WITH VARIOUS C_L (FULL BIAS MODE)

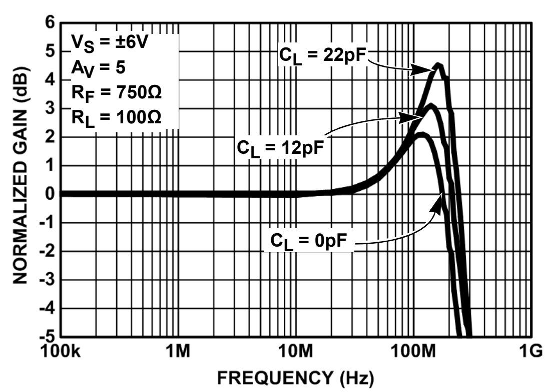


FIGURE 19. FREQUENCY RESPONSE vs VARIOUS C_L (MEDIUM BIAS MODE)

Typical Performance Curves (Continued)

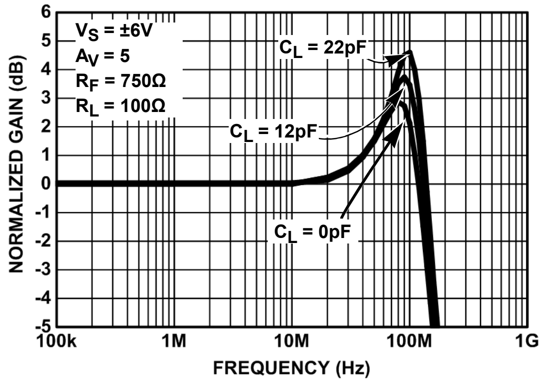


FIGURE 20. FREQUENCY RESPONSE WITH VARIOUS C_L (LOW BIAS MODE)

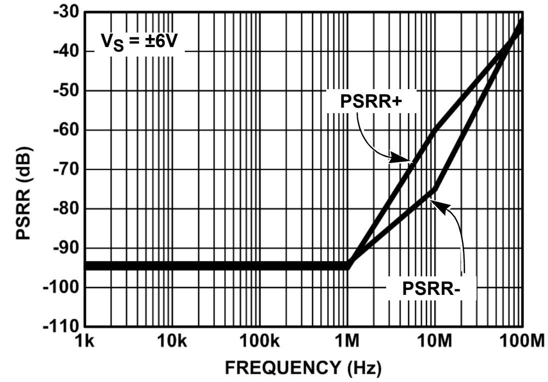


FIGURE 21. PSRR vs FREQUENCY

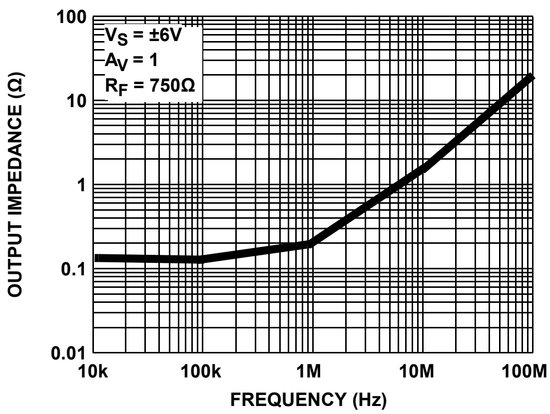


FIGURE 22. OUTPUT IMPEDANCE vs FREQUENCY

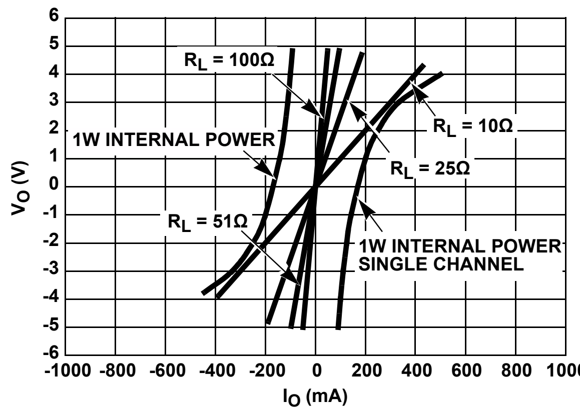


FIGURE 23. OUTPUT VOLTAGE AND CURRENT LIMITATIONS

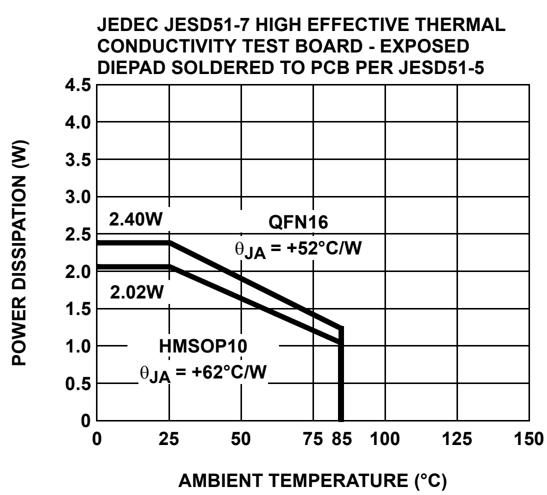


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The ISL1557 is a dual operational amplifier designed for line driving in DMT ADSL2+ and VDSL solutions. It is a dual current mode feedback amplifier with low distortion while drawing moderately low supply current. It is built using the Renesas proprietary complimentary bipolar process and is offered in industry standard pinouts. Due to the current feedback architecture, the ISL1557 closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First, select the desired bandwidth by choosing the feedback resistor, R_F, then set the gain by choosing the gain resistor, R_G. The curves at the beginning of the “Typical Performance Curves” section, on page 6, show the effect of varying both R_F and R_G. The 3dB bandwidth is somewhat dependent on the power supply voltage.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible (below 0.25”). The power supply pins must be well bypassed to reduce the risk of oscillation. A 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor is adequate for each supply pin. During power-up, it is necessary to limit the slew rate of the rising power supply to within 1V/µs. If the power supply rising time is undetermined, a series 10Ω resistor on the power supply line can be used to ensure the proper power supply rise time.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input. This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, but avoid using wire-wound resistors because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will effect the AC and transient performance of the ISL1557 when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect because this point is at a virtual ground and stray capacitance is therefore not “detected” by the amplifier.

Feedback Resistor Values

The ISL1557 has been designed and specified with R_F = 750Ω for A_V = +5. This value of feedback resistor yields extremely flat frequency response with 1dB peaking out to 250MHz. As with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. See the curves in the “Typical Performance Curves” section, beginning on page 6, which shows 3dB bandwidth and peaking vs frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3dB bandwidth drop off at high temperature, the ISL1557 is designed to have little supply current variations with temperature. An immediate benefit is the 3dB bandwidth does not drop off drastically with temperature.

Supply Voltage Range

The ISL1557IRZ is designed to operate with supply voltages from ±2.25V to ±6V nominal. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages.

Single Supply Operation

If a single supply is desired, values from +4.5V to +12V nominal can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either:

- DC bias the inputs at an appropriate common mode voltage and AC couple the signal (Figure 25), or:
- Ensure the driving signal is within the common mode range of the ISL1557. The ISL1557IUEZ must be used in single supply applications.

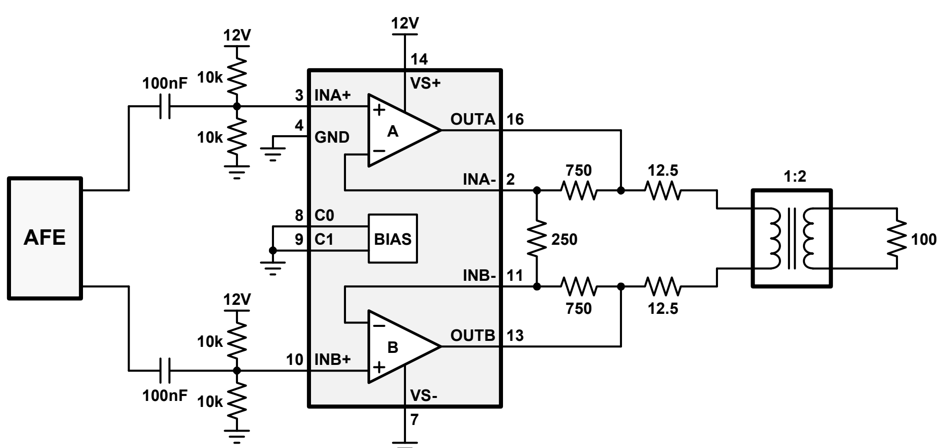


FIGURE 25. SINGLE SUPPLY OPERATION WITH INPUT COMMON-MODE BIASING

ADSL CPE Applications

The ISL1557 is designed as a line driver for ADSL CPE modems. It is capable of outputting 450mA of output current with a typical supply voltage headroom of 1.3V. It can achieve -85dBc of distortion at low 7.1mA of supply current per amplifier.

The average line power requirement for the ADSL CPE application is 14.5dBm (28mW) into a 100Ω line. The average line voltage is $1.67V_{RMS}$. The ADSL DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 7.5V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:2 is selected. The circuit configuration is shown in Figure 26.

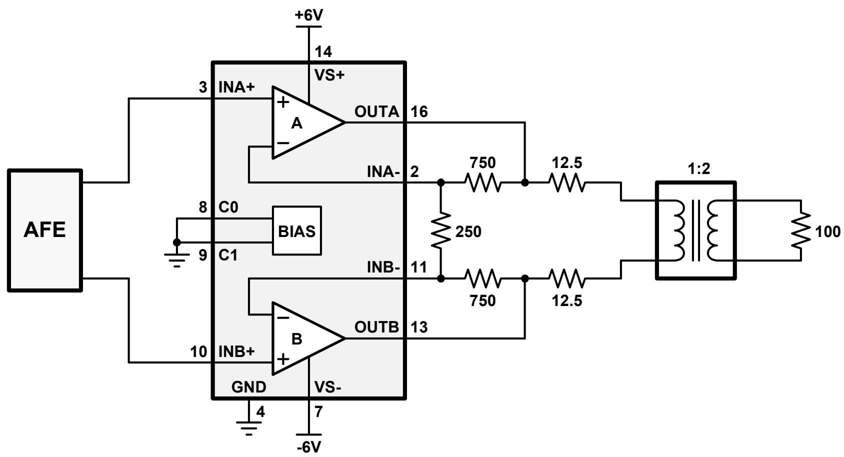


FIGURE 26. ADSL CPE DRIVER

Revision History

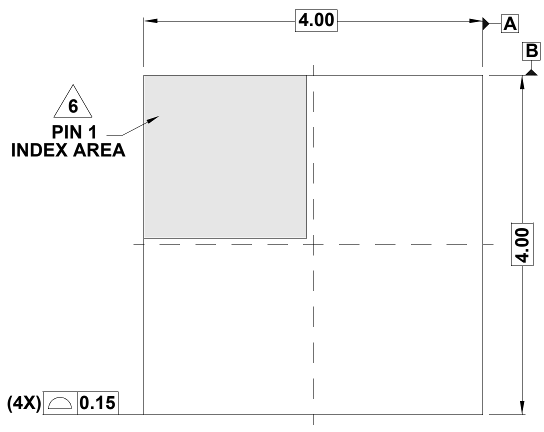
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Nov 7, 2019	FN7522.5	Updated links throughout. Replaced POD MDP0050 with POD M10.118B in the ordering information table and the Package Outline Drawings section. Updated disclaimer
May 2, 2018	FN7522.4	Added Figure 1. Added ISL1557FRZ part information throughout document. Added Pin Description table Added Table 1. Added Theta JA and JC information under the Thermal Information section. Updated Figures 8 through 16. Added Figure 25. Updated Figure 26.
Apr 6, 2018	FN7522.3	Added Related Literature section. Updated Ordering information table. Added Note 3. Moved and updated Note 4 to end of EC table. Added Revision History. Replaced POD MDP0046 (multiple lead counts) with L16.4x4H POD. Updated Disclaimer.

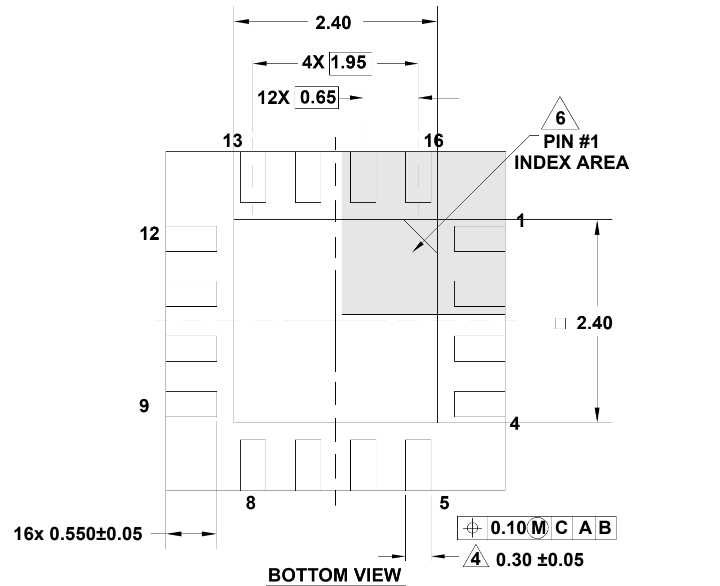
Package Outline Drawings

For the most recent package outline drawing, see L16.4x4H.

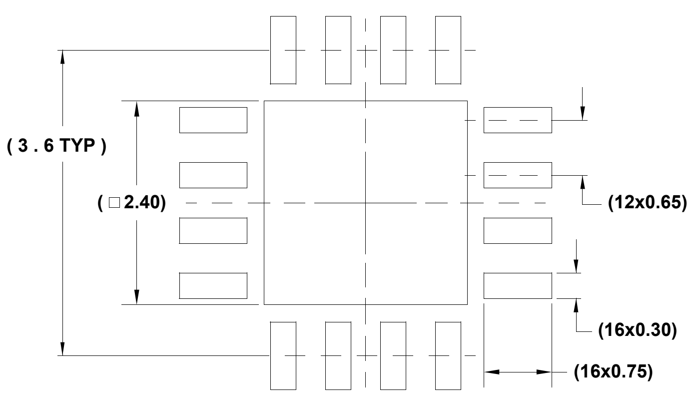
L16.4x4H
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 1/12



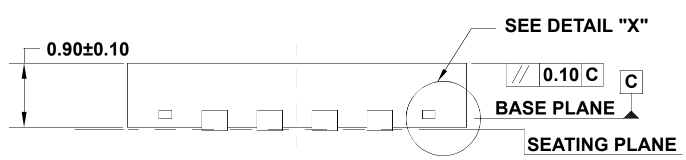
TOP VIEW



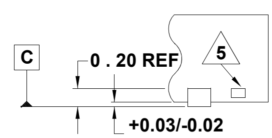
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



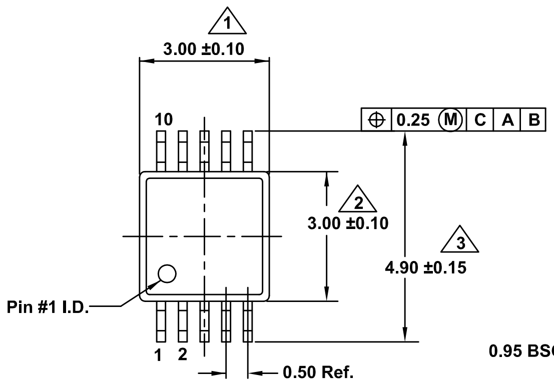
DETAIL "X"

NOTES:

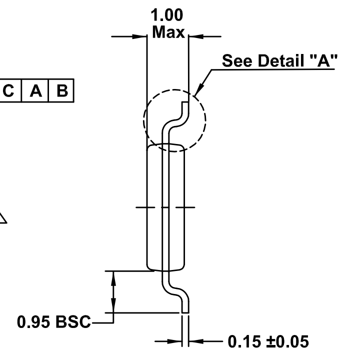
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

M10.118B
10 Lead Heatsink Mini Small Outline Plastic Package (HMSOP, Heatsink MSOP)
Rev 2, 10/19

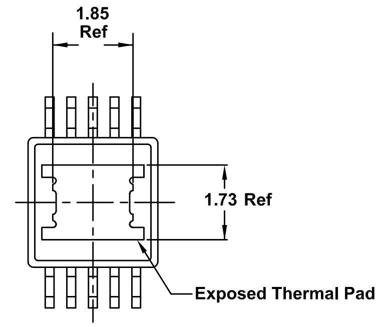
For the most recent package outline drawing, see M10.118B.



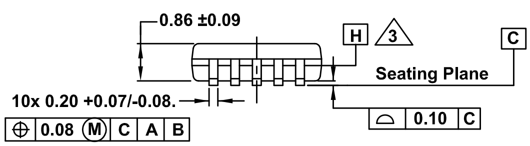
Top View



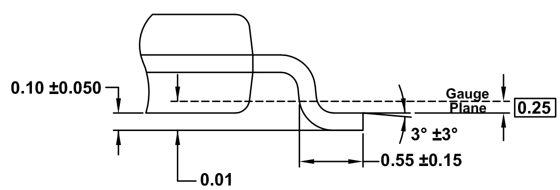
End View



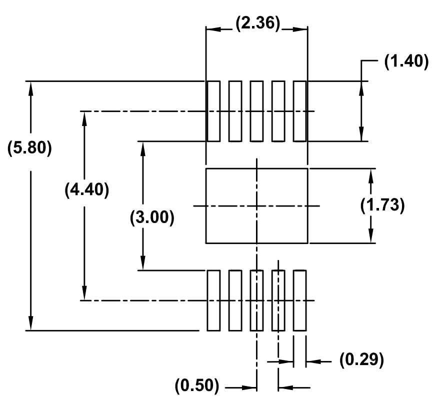
Bottom View



Side View



Detail "A"



Recommended Land Pattern

Notes:

1. Plastic or metal protrusions of 0.15 maximum per side are not included.
2. Plastic interlead protrusions of 0.25 maximum per side are not included.
3. Package body length and width dimensions are measured at Datum Plane "H".
4. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
5. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.

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