

Features

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
- Widest pull range options: ± 25 , ± 50 , ± 80 , ± 100 , ± 150 , ± 200 , ± 400 , ± 800 , ± 1600 , ± 3200 ppm
- 0.23 ps RMS phase jitter (typ) over 12 kHz to 20 MHz bandwidth
- Wide temperature range support from -40°C to 105°C
- Industry-standard packages: 7.0 x 5.0 mm, 5.0 x 3.2 mm, 3.2 x 2.5 mm packages
- For frequencies 220.000001 MHz to 720 MHz, refer to [SiT3373](#)

Applications

- Cable Modem Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors, Remote Radio Head (RRH)
- SATA, SAS, 10Gbps Ethernet, Fibre Channel, PCI-Express



Electrical Characteristics

Table 1. Electrical Characteristics – Common to LVPECL, LVDS and HCSL

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	220	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-15	–	+15	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at 25°C . Contact SiTime for ± 15 ppm.
		-25	–	+25	ppm	
		-35	–	+35	ppm	
		-50	–	+50	ppm	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	$^{\circ}\text{C}$	Extended Commercial
		-40	–	+85	$^{\circ}\text{C}$	Industrial.
		-40	–	+95	$^{\circ}\text{C}$	
		-40	–	+105	$^{\circ}\text{C}$	Extended Industrial
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Voltage Control Characteristics						
Pull Range	PR	± 25 , ± 50 , ± 80 , ± 100 , ± 150 , ± 200 , ± 400 , ± 800 , ± 1600 , ± 3200			ppm	See the APR (Absolute Pull Range) Table 11 . Contact SiTime for custom pull range options.
Upper Control Voltage	VC_U	90%	–	–	Vdd	Voltage at which maximum frequency deviation is guaranteed
Lower Control Voltage	VC_L	–	–	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
Control Voltage Input Impedance	VC_z	–	10	–	M Ω	
Control Voltage Input Bandwidth	V_c	–	10	–	kHz	Contact SiTime for other input bandwidth options
Pull Range Linearity	Lin	–	–	1.0	%	
Frequency Change Polarity	–	Positive Slope		–		
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 2, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 2, OE
Input Pull-up Impedance	Z_in	–	100	–	k Ω	Pin 2, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Startup Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	μs	f = 156.25 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 7 and Figure 8

Table 2. Electrical Characteristics – LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	92	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	61	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Maximum Output Current	I _{driver}	–	–	33	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	V _{OH}	V _{dd} -1.15	–	V _{dd} -0.7	V	See Figure 3
Output Low Voltage	V _{OL}	V _{dd} -2.0	–	V _{dd} -1.5	V	See Figure 3
Output Differential Voltage Swing	V _{Swing}	1.2	1.6	2.0	V	See Figure 4
Rise/Fall Time	T _r , T _f	–	225	290	ps	20% to 80%, see Figure 4
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter ^[1]	T _{jitt}	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.225	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.225	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -40 to 95 °C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V _{dd} levels.
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter ^[1]	T _{jitt}	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.225	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -40 to 95 °C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V _{dd} levels.

Notes:

1. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	84	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	62	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Output Characteristics						
Differential Output Voltage	V _{OD}	250	–	450	mV	See Figure 5
VOD Magnitude Change	ΔV _{OD}	–	–	50	mV	See Figure 5
Offset Voltage	V _{OS}	1.125	–	1.375	V	See Figure 5
VOS Magnitude Change	ΔV _{OS}	–	–	50	mV	See Figure 5
Rise/Fall Time	T _r , T _f	–	400	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 6
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter^[2]	T _{jitt}	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.215	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -40 to 95 °C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V _{dd} levels.
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter^[2]	T _{jitt}	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.235	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -40 to 95 °C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V _{dd} levels.

Notes:

2. Measured according to JESD65B

Table 4. Electrical Characteristics – HCSL

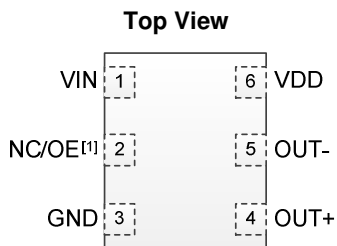
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	97	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	62	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Maximum Output Current	I _{driver}	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	V _{OH}	0.60	–	0.90	V	See Figure 3
Output Low Voltage	V _{OL}	-0.05	–	0.08	V	See Figure 3
Output Differential Voltage Swing	V _{Swing}	1.2	1.4	1.80	V	See Figure 4
Rise/Fall Time	T _r , T _f	–	360	495	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, See Figure 4
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter ^[3]	T _{jitt}	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.220	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -40 to 95 °C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V _{dd} levels.
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter ^[3]	T _{jitt}	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C.
		–	0.230	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dd} levels, includes spurs, pull range = 100 ppm. Temperature ranges -40 to 95 °C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 or 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all V _{dd} levels.

Notes:

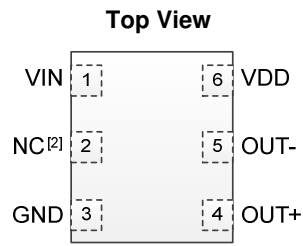
3. Measured according to JESD65B

Table 5. Pin Description

Pin	Symbol	Functionality	
1	VIN	Input	Control Voltage
2	NC/OE	No Connect (NC)	No Connect: Leave floating or connect to GND for better heat dissipation. NC for all 3.2 x 2.5 mm package options.
		Output Enable (OE)	H ^[4,5] : specified frequency output L: output is high impedance. Only output driver is disabled. OE function only available on 7050 package. Pin 2 on 3225 package is NC.
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	Vdd	Power	Power supply voltage ^[6]



**Figure 1. Pin Assignments
(7.0 x 5.0 mm and
5.0 x 3.2 mm packages)**



**Figure 2. Pin Assignments
(3.2 x 2.5 mm package)**

Notes:

4. A pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
5. OE mode is only available in the 7050 and 5032 packages. 3225 package is NC.
6. A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase jitter performance.

Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
V _{IH}		Vdd + 0.3V	V
V _{IL}	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

Table 7. Thermal Considerations^[7]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	80	30
5032, 6-pin	TBD	TBD
7050, 6-pin	52	19

Notes:

7. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 8. Maximum Operating Junction Temperature^[8]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
95°C	120°C
105°C	130°C

Notes:

8. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	<i>g</i>
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	<i>g</i>
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams

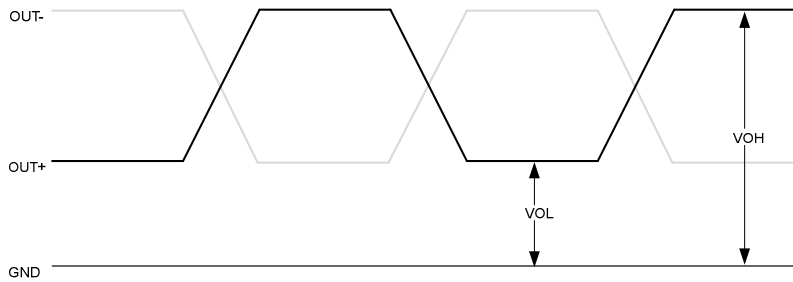


Figure 3. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

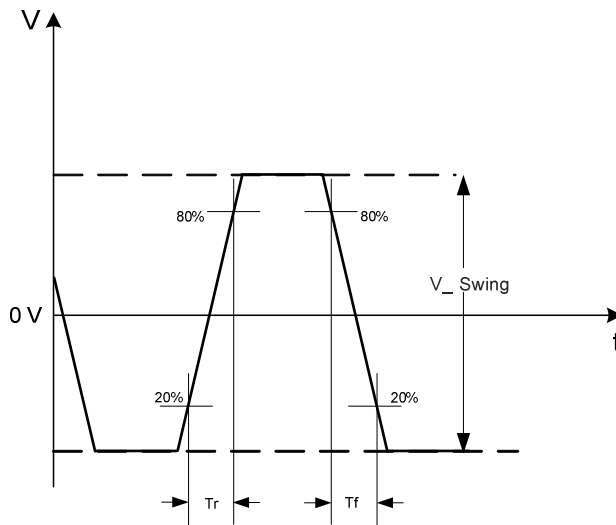


Figure 4. LVPECL/HCSL Voltage Levels across Differential Pair

Waveform Diagrams (continued)

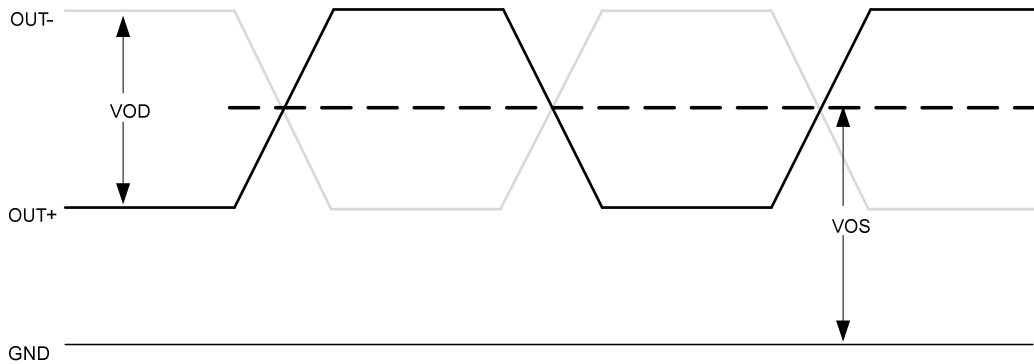


Figure 5. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

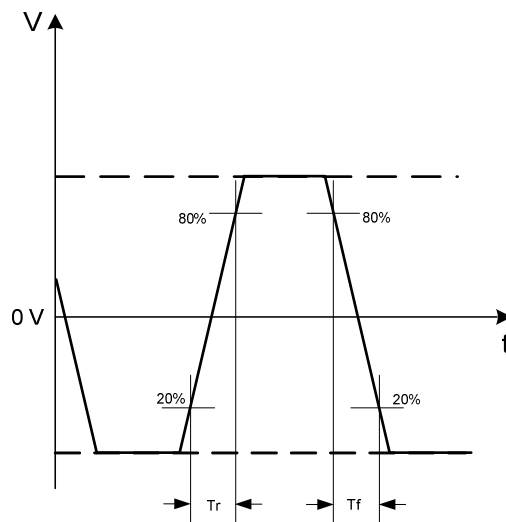


Figure 6. LVDS Differential Waveform

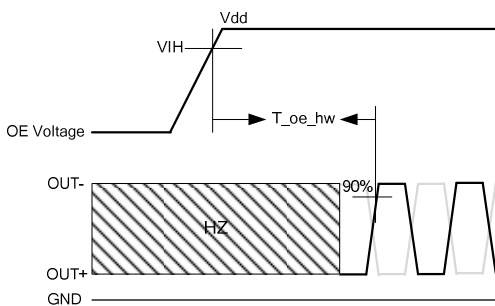


Figure 7. Hardware OE Enable Timing

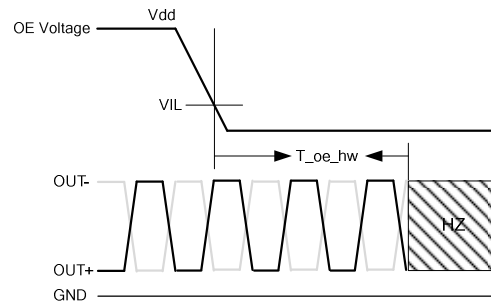


Figure 8. Hardware OE Disable Timing

Termination Diagrams

LVPECL:

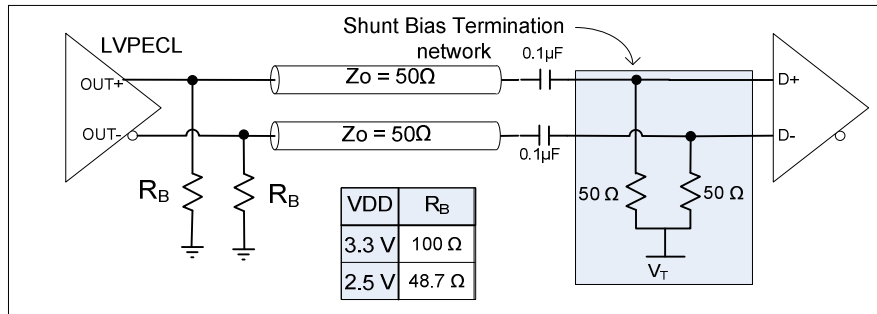


Figure 9. LVPECL with AC-coupled termination

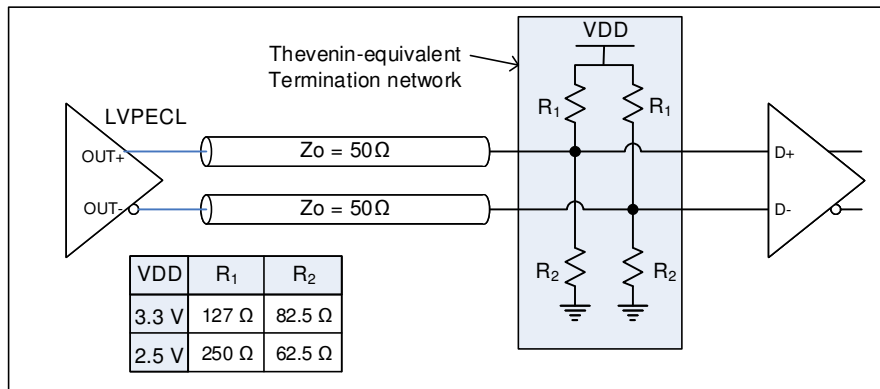


Figure 10. LVPECL DC-coupled load termination with Thevenin equivalent network

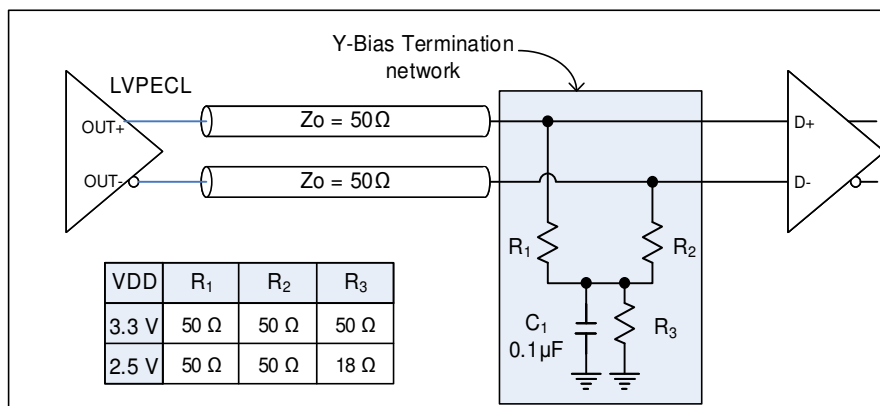


Figure 11. LVPECL with Y-Bias termination

Termination Diagrams (continued)

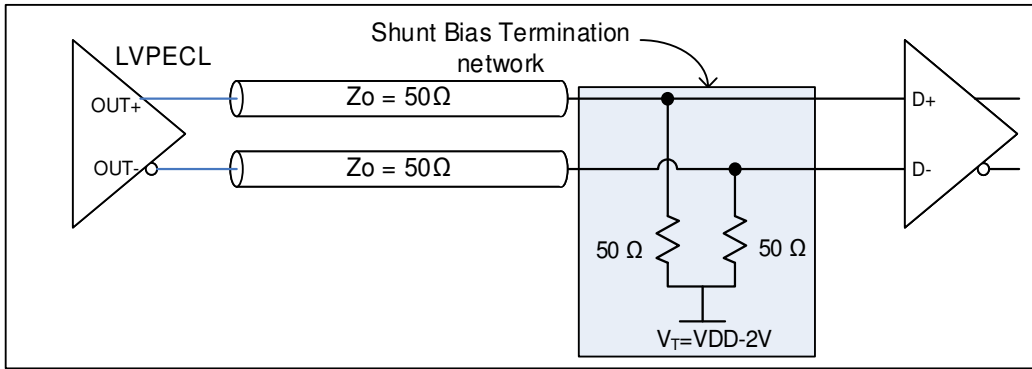


Figure 12. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (continued)

LVDS:

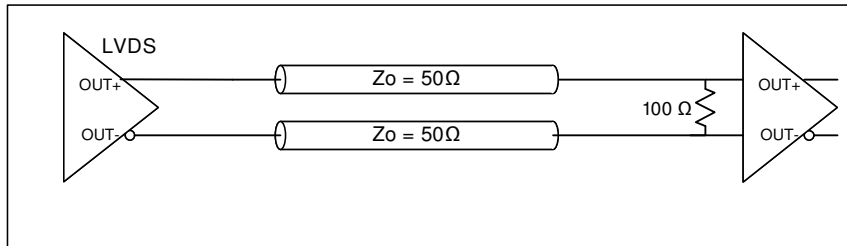


Figure 13. LVDS single DC termination at the load

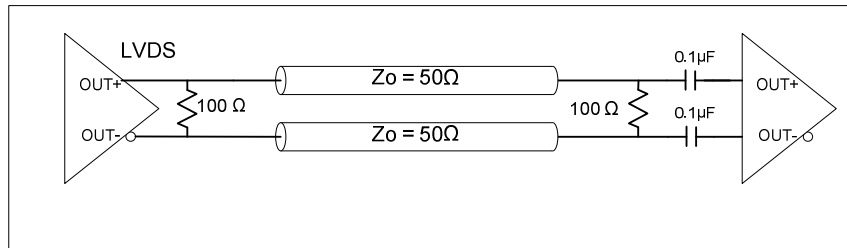


Figure 14. LVDS double AC termination with capacitor close to the load

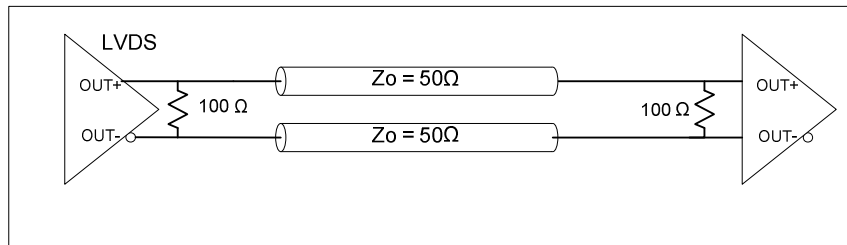


Figure 15. LVDS double DC termination

Termination Diagrams (continued)

HCSL:

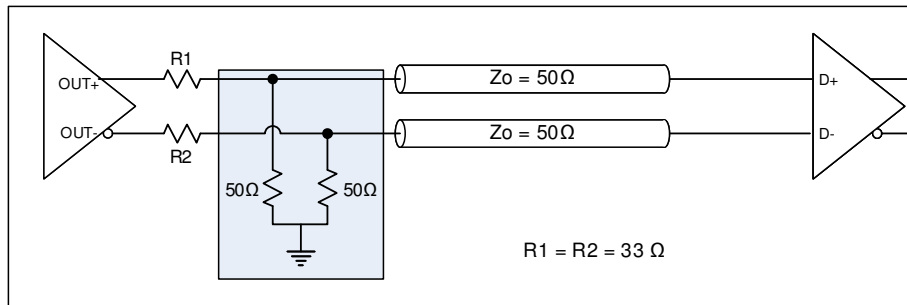
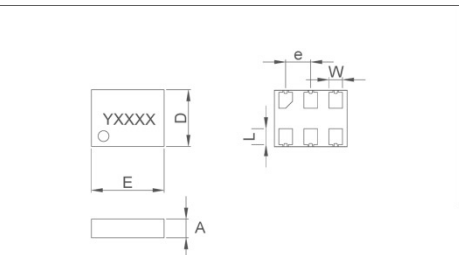

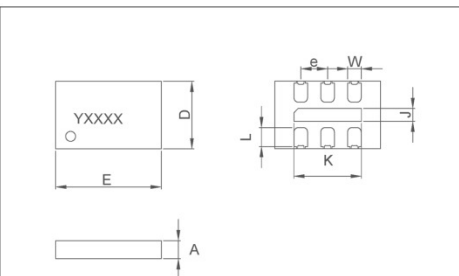
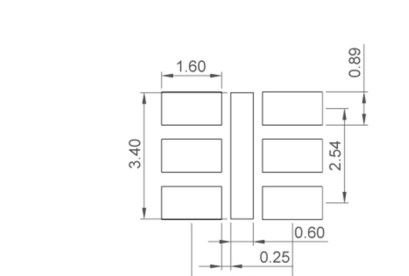
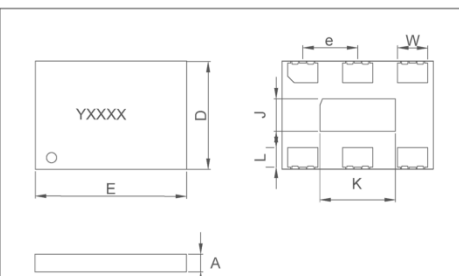
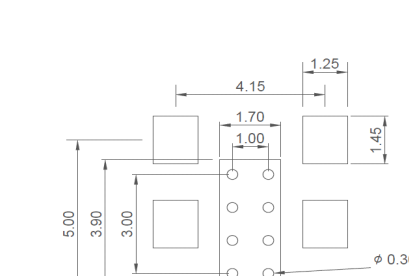


Figure 16. HCSL interface termination

Dimensions and Patterns

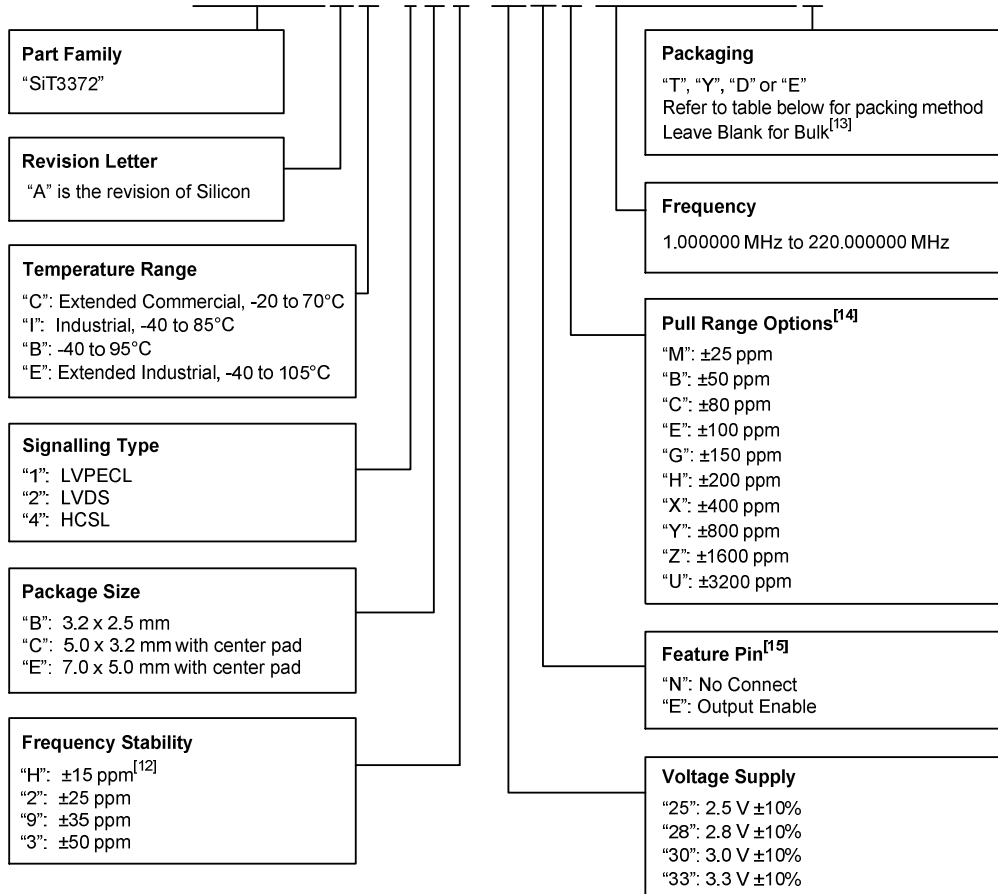
Package Size – Dimensions (Unit: mm) ^[9]	Recommended Land Pattern (Unit: mm) ^[10]																																															
<p>3.2 x 2.5 x 0.85 mm</p>  <table border="1" data-bbox="617 336 941 546"> <caption>Dimension Table</caption> <thead> <tr> <th></th> <th>Symbol</th> <th>Min</th> <th>Nom</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>TOTAL THICKNESS</td> <td>A</td> <td>0.800</td> <td>0.850</td> <td>0.900</td> </tr> <tr> <td rowspan="2">BODY SIZE</td> <td>X</td> <td>D</td> <td>2.400</td> <td>2.500</td> <td>2.600</td> </tr> <tr> <td>Y</td> <td>E</td> <td>3.200</td> <td>3.200</td> <td>3.300</td> </tr> <tr> <td>LEAD PITCH</td> <td>e</td> <td colspan="3">1.100 BSC</td> </tr> <tr> <td>LEAD LENGTH</td> <td>L</td> <td>0.650</td> <td>0.700</td> <td>0.750</td> </tr> <tr> <td>LEAD WIDTH</td> <td>W</td> <td>0.550</td> <td>0.600</td> <td>0.650</td> </tr> </tbody> </table> <div style="display: flex; justify-content: space-between; align-items: center; margin-top: 10px;"> <div data-bbox="617 630 763 724"> <p>6L QFN 3.2 x 2.5 x 0.75 mm POD-38 Rev A</p> </div> <div data-bbox="771 630 941 724"> <p>Package Outline </p> </div> </div>		Symbol	Min	Nom	Max	TOTAL THICKNESS	A	0.800	0.850	0.900	BODY SIZE	X	D	2.400	2.500	2.600	Y	E	3.200	3.200	3.300	LEAD PITCH	e	1.100 BSC			LEAD LENGTH	L	0.650	0.700	0.750	LEAD WIDTH	W	0.550	0.600	0.650	<p>3.2 x 2.5 x 0.85 mm</p> 											
	Symbol	Min	Nom	Max																																												
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Notes:

9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
10. A capacitor of value 0.1 μ F or higher between Vdd and GND is required. An additional 10 μ F capacitor between Vdd and GND is required for the best phase jitter performance
11. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information

SiT3372AC-1B2-33NH122.123456T



Notes:

- 12. Contact [SiTime](#) for ±15 ppm
- 13. Bulk is available for sampling only
- 14. Contact [SiTime](#) for custom pull range options
- 15. "E": Output Enable function is only available in 7.0 x 5.0 mm and 5.0 x 3.2 mm packages

Table 10. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
5.0 x 3.2	—	—	T	Y	—	—
3.2 x 2.5	D	E	T	Y	—	—

Table 11. APR Table

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab)-aging

Nominal Pull Range	Frequency Stability			
	± 15	± 25	± 35	± 50
	APR (ppm)			
± 25	± 5	—	—	—
± 50	± 30	± 20	± 10	—
± 80	± 60	± 50	± 40	± 25
± 100	± 80	± 70	± 60	± 45
± 150	± 130	± 120	± 110	± 95
± 200	± 180	± 170	± 160	± 145
± 400	± 380	± 370	± 360	± 345
± 800	± 780	± 770	± 760	± 745
± 1600	± 1580	± 1570	± 1560	± 1545
± 3200	± 3180	± 3170	± 3160	± 3145

Table 12. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
Part number Generator	Tool used to create the part number based on desired features.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/manufacturing-notes
Product Qualification report	Device reliability report	https://www.sitime.com/sites/default/files/gated/RR45_Third%20Generation%20DEXO%2C%20VCXO%20Product%20Qualification%20Report_A01.pdf
Environmental Reports	RoHS report	https://www.sitime.com/sites/default/files/gated/QI-86_RoHSCert_Third Generation DEXO, VCXO Package_Homogeneous_Materials_A00.pdf
Composition report	Get from Robin	https://www.sitime.com/sites/default/files/gated/QI-87%20Third%20Generation%20DEXO%2C%20VCXO%20Composition%20Report_A01_0.pdf
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Table 13. Revision History

Revision	Release Date	Change Summary
1.0	10/13/2017	Initial release
1.03	05/10/2018	Updated the Part Ordering info with added 5.0 x 3.2 mm package

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