SN75LVCP600S EVM User's Guide

User's Guide

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The SN75LVCP600S User's Guide is intended to assist in the evaluation of the SN75LVCP600S SATA/SAS Redriver/Equalizer, highlighting key features, operating conditions and the configuration of the EVM for system level evaluation.

The construction of the SN75LVCP600S EVM also serves as a reference design which can be easily modified for the vast majority of intended applications such as Servers and Workstations.

Introduction

The SN75LVCP600S is a single channel SATA/SAS signal conditioner supporting data rates up to 6.0 Gbps. The device complies with the SATA Physical Specification Revision 3.0 and SAS Electrical Specification Revision 2.0.

The SN75LVCP600S operates from a single 3.3-V supply and has 100-Ω line termination with self-biasing feature, making the device suitable for AC coupling. The device offers programmable equalization and de-emphasis as well as Auto Low Power Mode triggered when the channel is in electrical idle state > 100 µs.

SN75LVCP600S EVM Configuration

1 SN75LVCP600S EVM Kit Contents

This EVM kit should contain the following items:

- SN75LVCP600S EVM board
- 9-V DC power supply
- This user's guide

2 Description of EVM Board

This EVM is designed to provide easy evaluation of the LVCP600S device though two standard SATA connectors. The EVM is also meant to serve as a reference design to show a practical example of how to design the device in production designs. Figure 1 below illustrates the locations of jumpers for the EVM, Table 1 below highlights the jumper settings and configuration definitions.

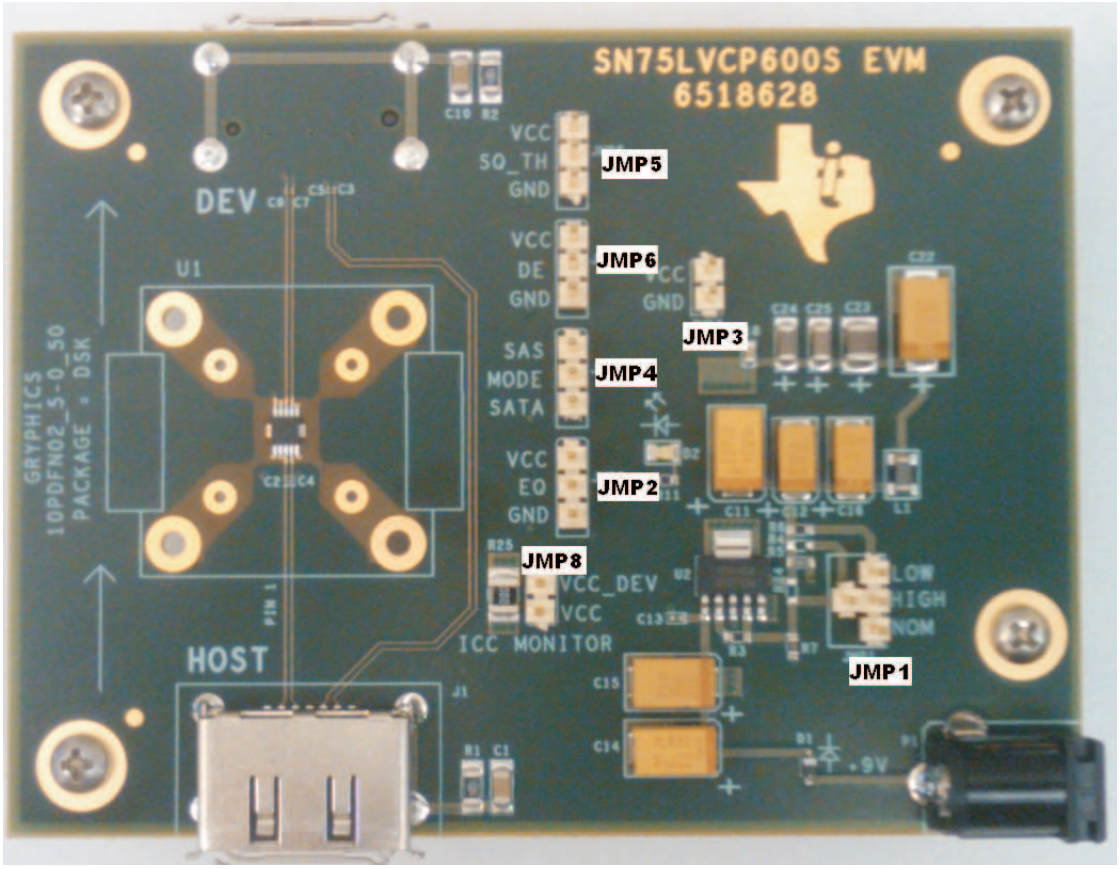

Figure 1. EVM Board Jumper Locations

Table 1. SN75LVCP600S EVM Configuration Jumper Settings

JUMPER NUMBER	FUNCTIONALITY AND CONFIGURATION
JMP1	Device voltage level select
	3.0 V - Shunt pins 2 and 1 (Center pin to "Low")
	3.3 V - Shunt pins 2 and 3 (Center pin to "Nom")
	3.6 V - Shunt pins 2 and 4 (Center pin to "High")
JMP2	Equalization control settings
	Low (7 dB) = Shunt pins 2 and 3 (Center pin to "GND")
	High (14 dB) = Shunt pins 2 and 1 (Center pin to "VCC")
JMP3	VCC
	Pin 1 = 3.3 V VCC
	Pin 2 = GND
JMP4	Mode select
	Low (SATA) = Shunt pins 2 and 3 (Center pin to “SATA”)
	High (SAS) = Shunt pins 1 and 2 (Center pin to “SAS”)
JMP5	Squelch threshold level select
	Low (100%) = Shunt pins 2 and 1 (Center pin to "GND")
	High (80%) = Shunt pins 2 and 3 (Center pin to "VCC")
JMP6	De-emphasis control selector
	High = Shunt pins 2 and 1 (-3 dB at 6 Gbps)
	Low = Shunt pins 2 and 3 (0 dB at 6 Gbps)
JMP8	Test point for measuring current
	Read the "Monitoring Device Current" section before using

3 Power for the SN75LVCP600S EVM

The SN75LVCP600S EVM kit comes with a 9-V DC power supply that fits a standard North American wall socket.

4 Monitoring the Device Current

One of the highlights of the SN75LVCP600S is the power savings features of the device. To observe these power saving features this EVM design includes the option of monitoring the current draw of the device. To enable this feature, the following steps must be taken:

1. Un-install the ferrite bead located at L1.
2. Obtain a 3.3-V power supply (connect current meter in series if power supply does not also display current, or if greater resolution is needed than the power supply can provide). Connect power supply 3 V to pin 1 of the two pin header JMP1. GND from the power supply can be connected to pin 2 of header JMP1.

SN75LVCP600S EVMPCB Construction

The following section details the construction of the EVM board including schematics and layout files to demonstrate how the board was designed and manufactured.

1 SN75LVCP600S EVM Board Schematics

This section shows the board schematic sheets for the EVM.

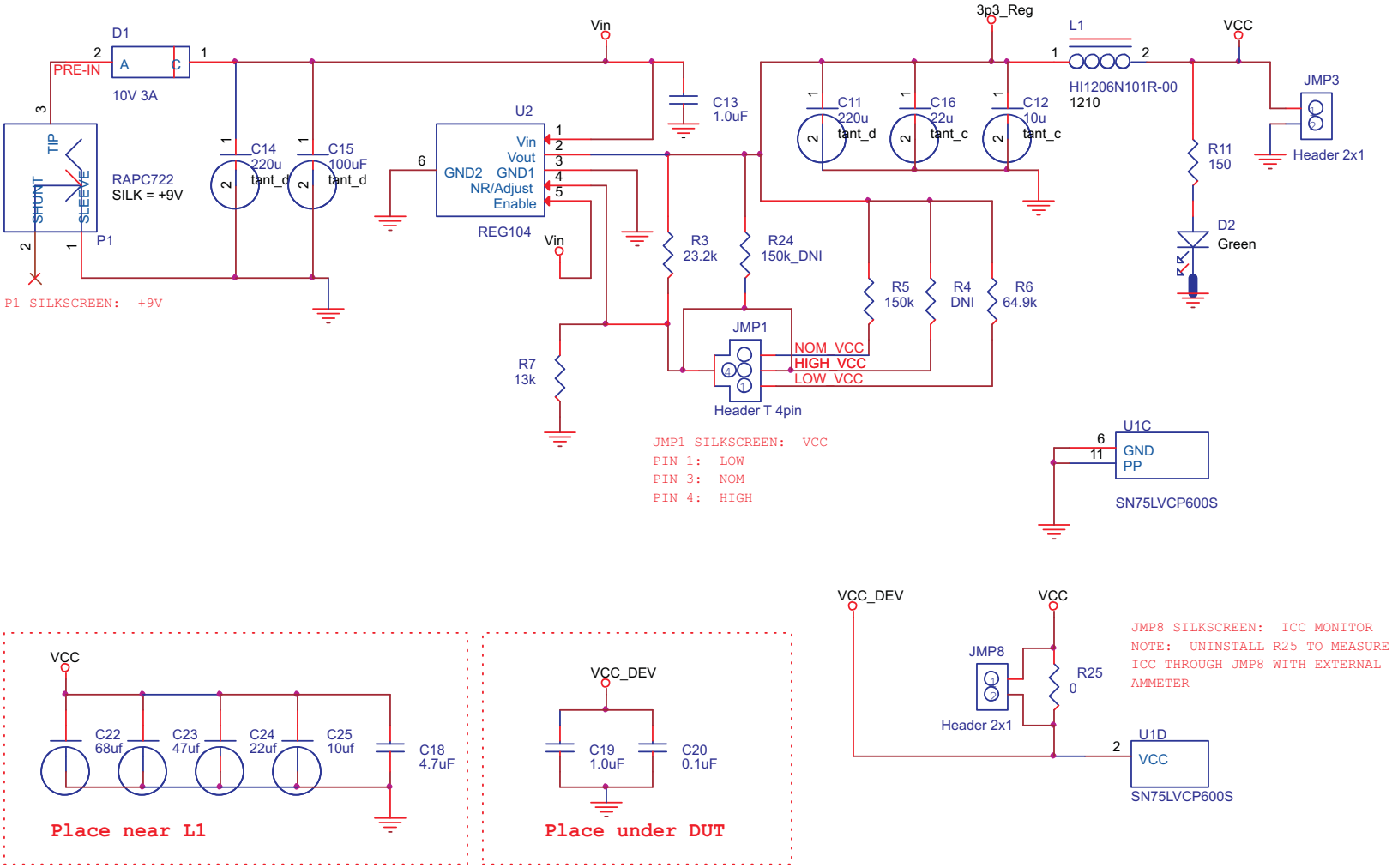

Figure 2. SN75LVCP600S EVM - Power

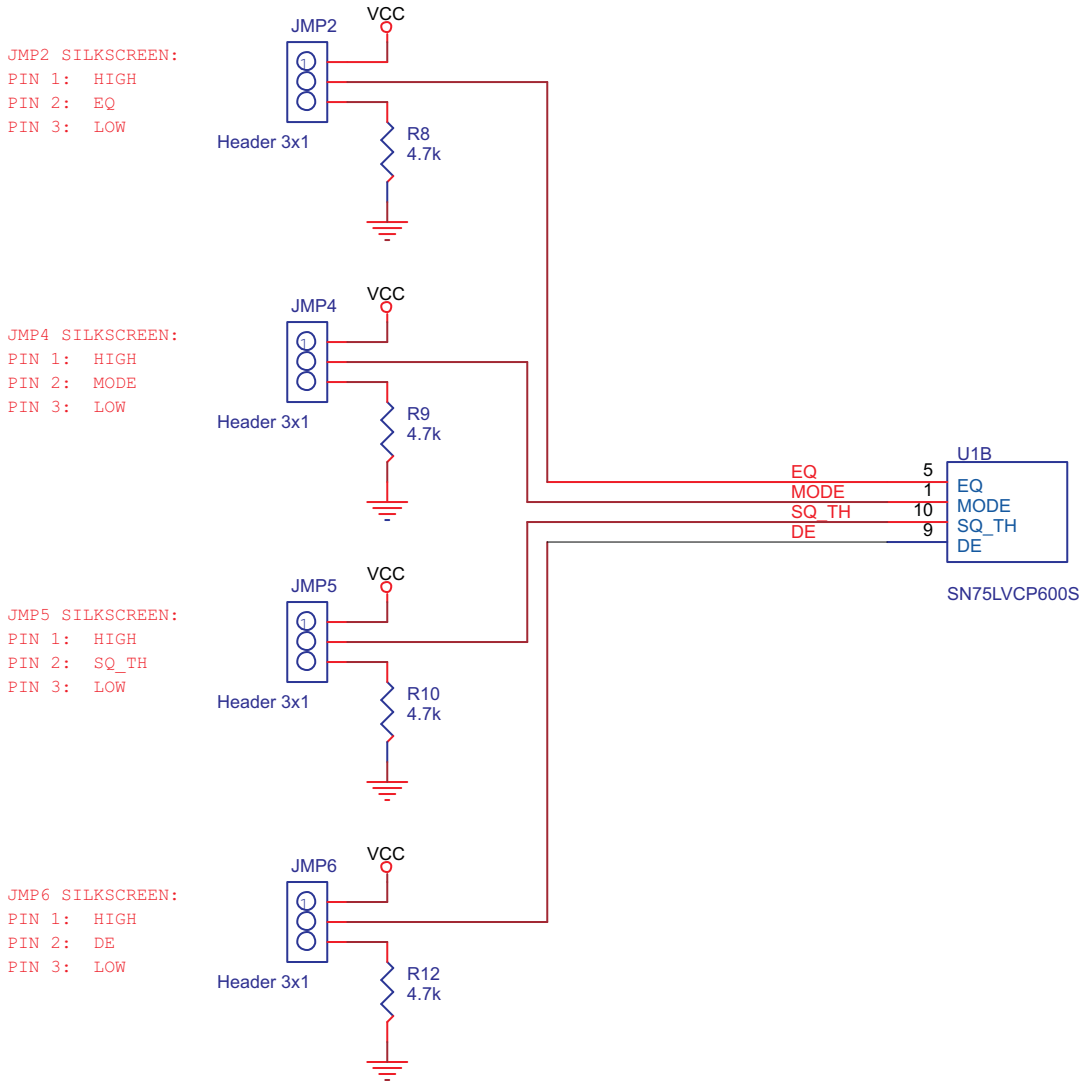

Figure 3. SN75LVCP600S EVM - Control

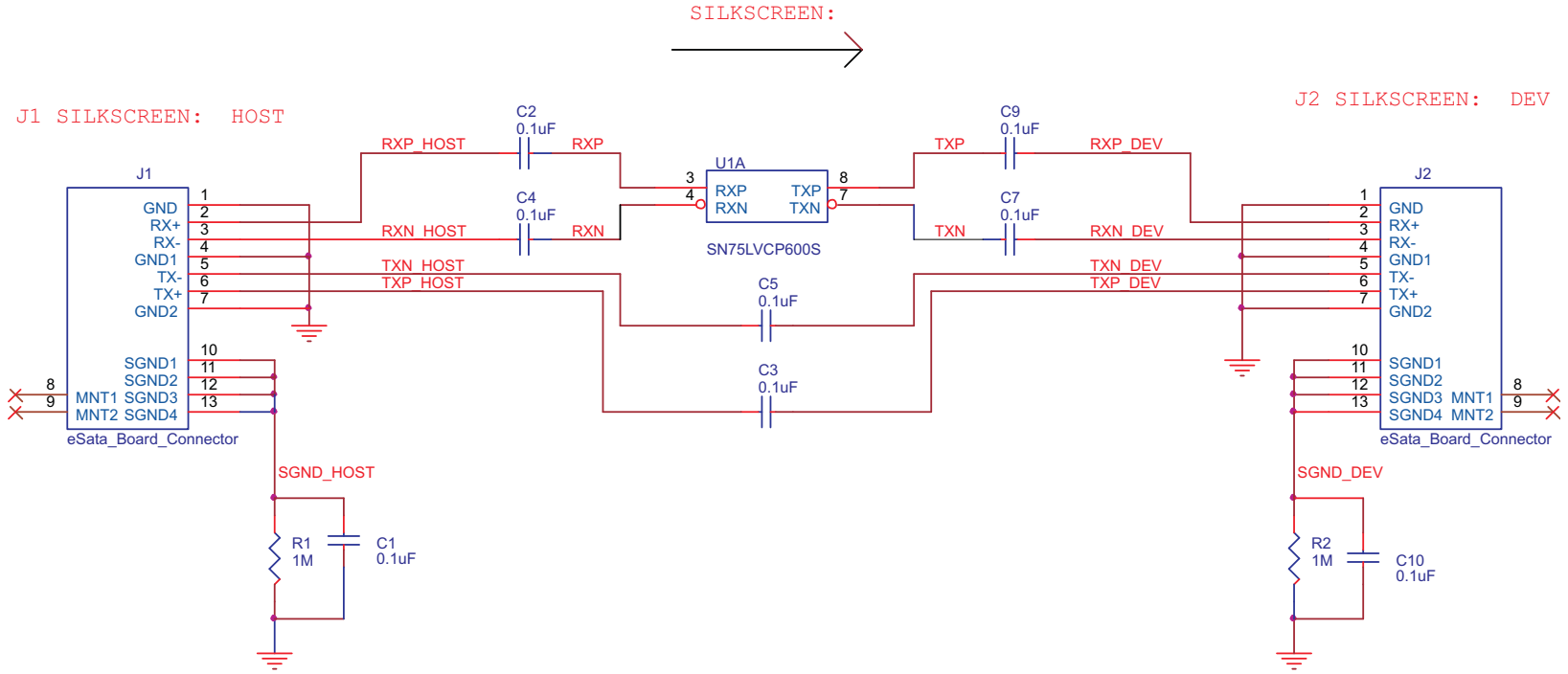

Figure 4. SN75LVCP600S EVM - High Speed

2 SN75LVCP600S EVM Board Layout

The SN75LVCP600S EVM was designed to to demonstrate a 6-layer board layout.

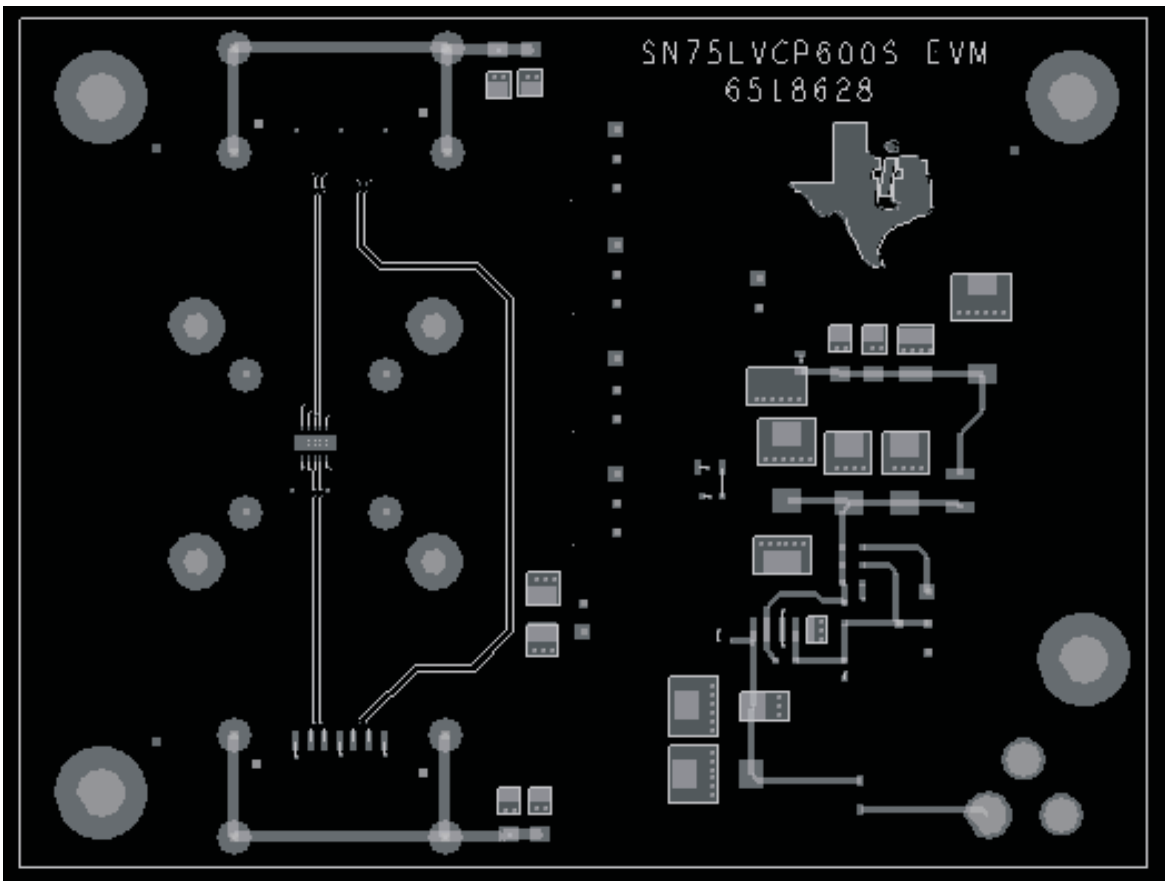

Figure 5. SN75LVCP600S EVM Top Layer

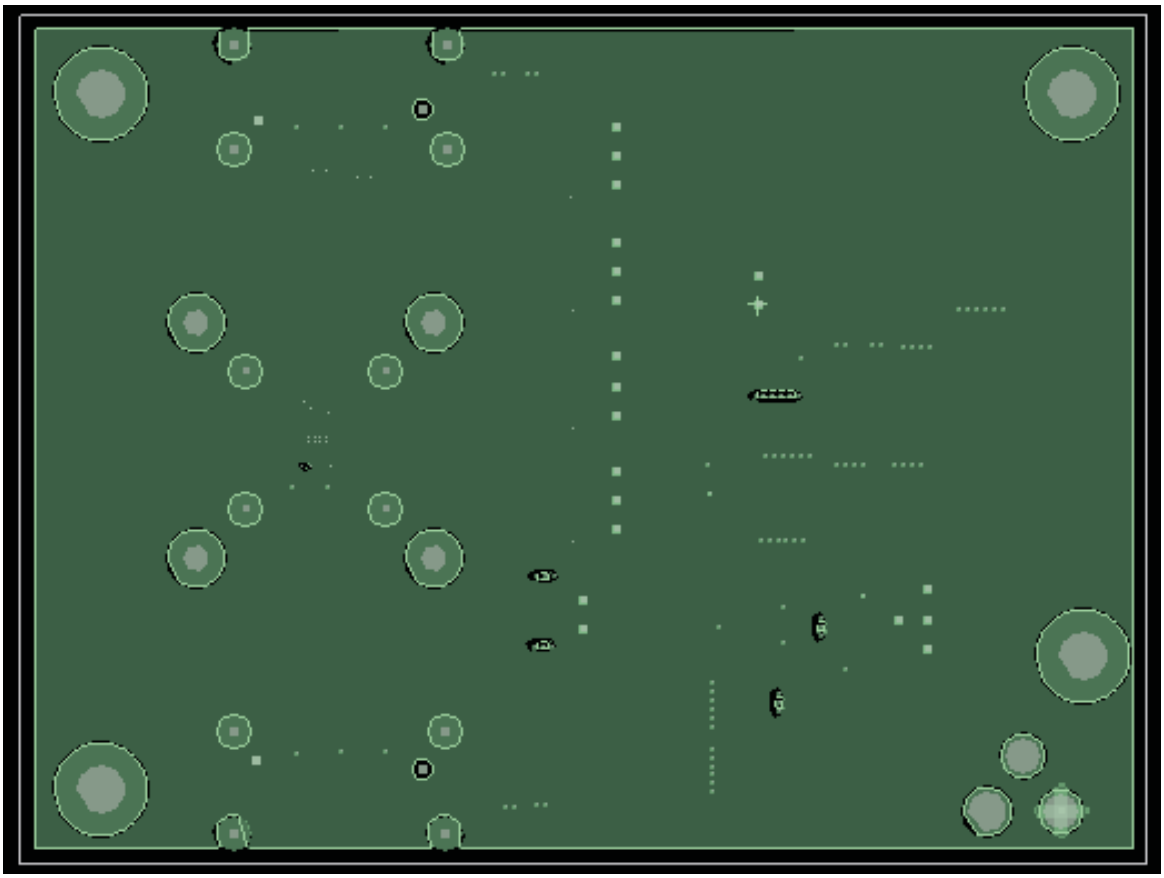

Figure 6. SN75LVCP600S EVM Layer 2 (GND)

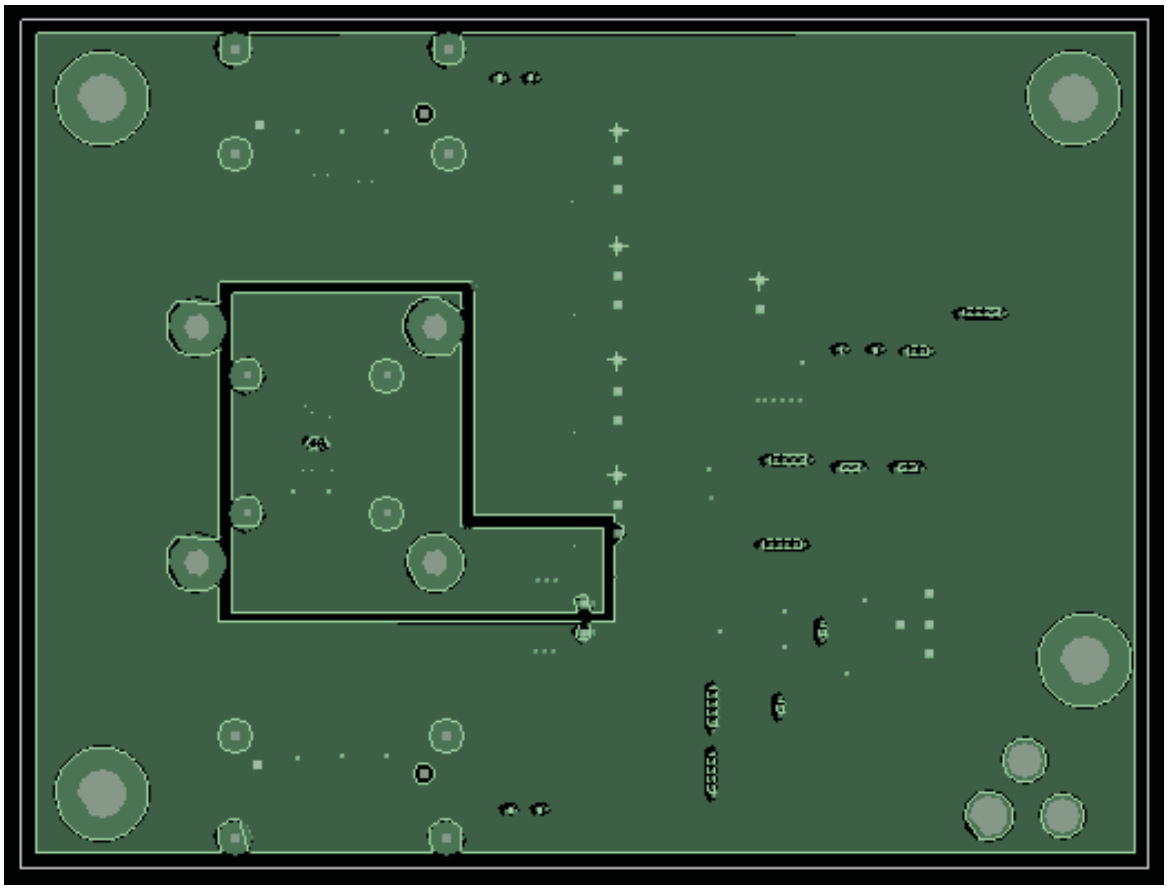

Figure 7. SN75LVCP600S EVM Layer 3 (VCC)

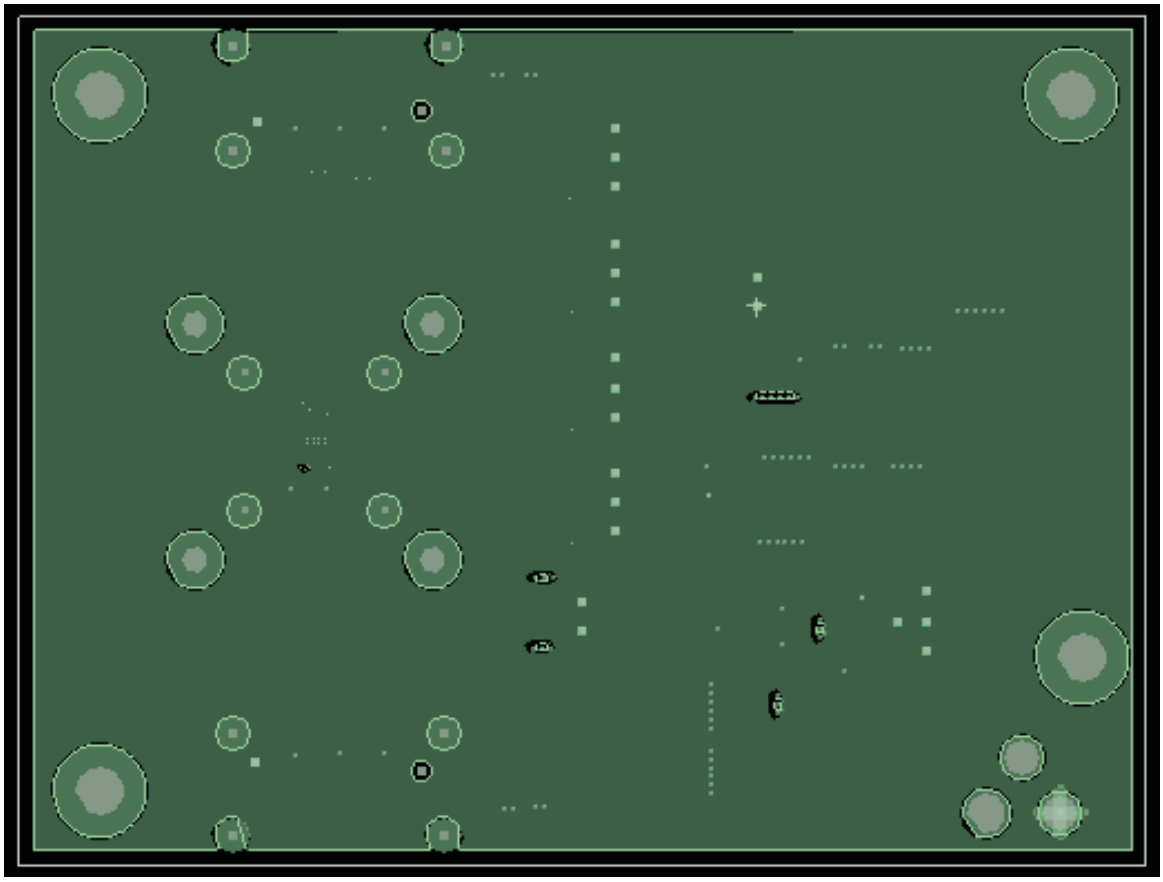

Figure 8. SN75LVCP600S EVM Layer 4 (GND)

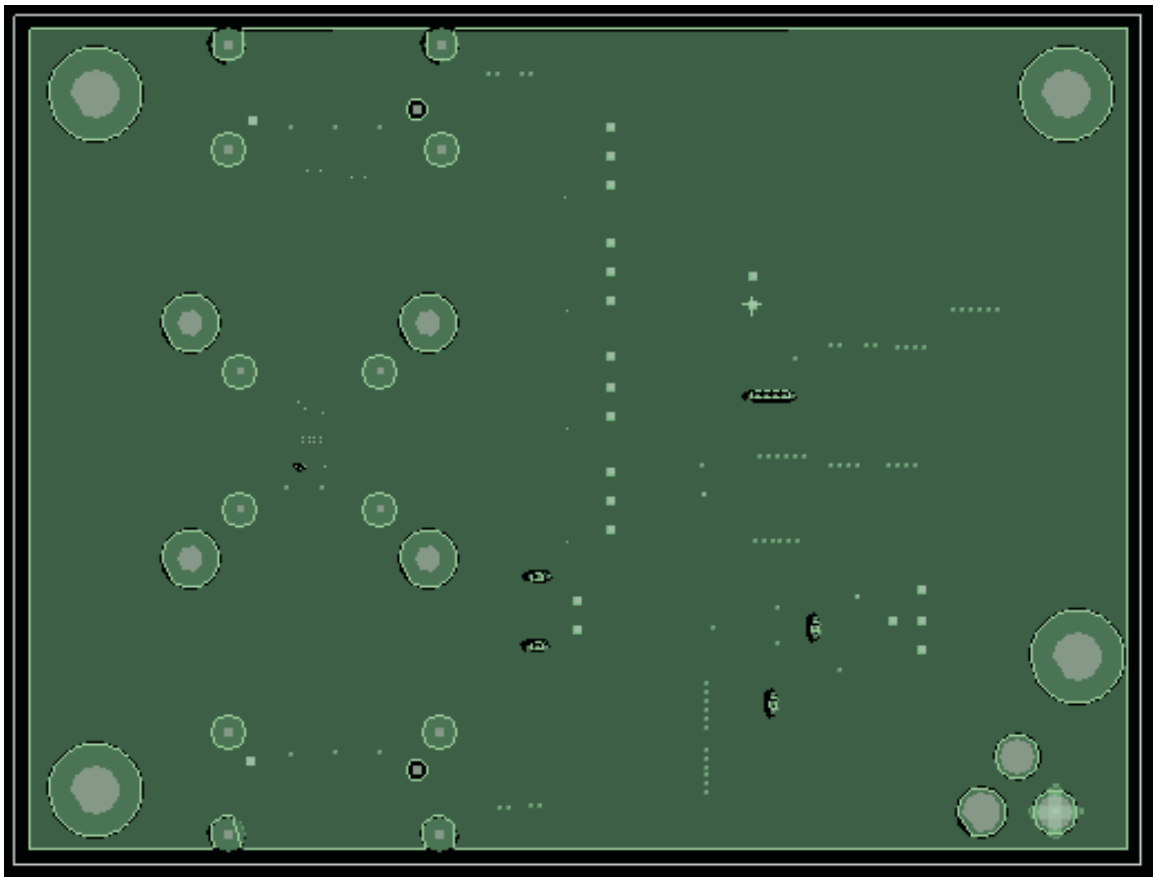

Figure 9. SN75LVCP600S EVM Layer 5 (GND)

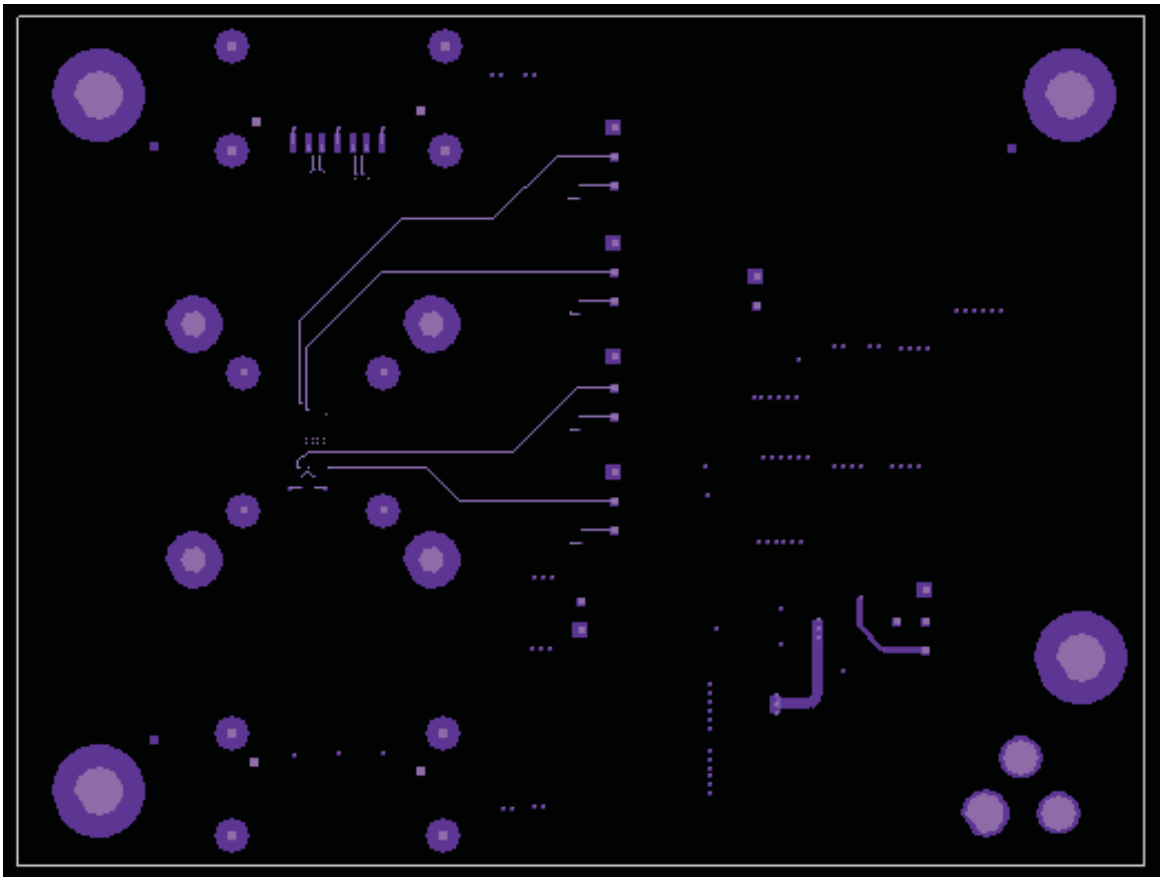

Figure 10. SN75LVCP600S EVM Layer 6 (Bottom)

3 SN75LVCP600S EVM Board Construction

The SN75LVCP600S EVM board is a 6-layer board constructed of FR4 – 370 material. The board stackup consists of a signal layer on top, ground layer, power layer, two ground layers and a signal layer on bottom.

The high-speed data signals of this board were routed as single-ended 50-Ω transmission lines, the differential routing of these signals with 100-Ω impedance matching can be implemented as well.

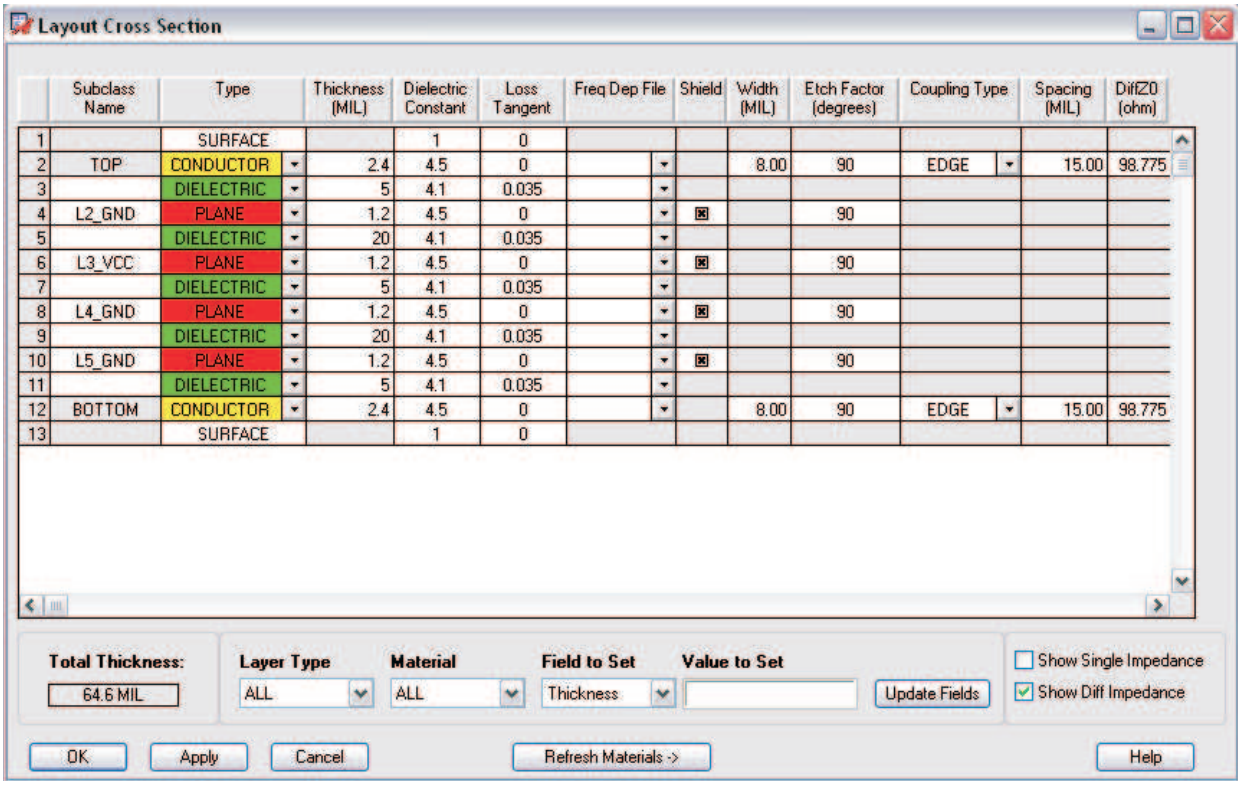

Figure 11. SN75LVCP600S EVM Board Stack-Up

Appendix A SN75LVCP600S EVM Bill of Materials

Table 2. Bill of Materials

Item	Quantity	Value	Reference
1	2	C1, C10	0.1µF
2	6	C2, C3, C4, C5, C7, C9	0.1µF
3	2	C11, C14	220µF
4	1	C12	10µF
5	2	C13, C19	1.0µF
6	1	C15	100µF
7	1	C16	22µF
8	1	C18	4.7µF
9	1	C20	0.1µF
10	1	C22	68µF
11	1	C23	47µF
12	1	C24	22µF
13	1	C25	10µF
14	1	D1	10V 3A
15	1	D2	LED
16	1	JMP1	Header T 4pin
17	4	JMP2, JMP4, JMP5, JMP6	Header 3x1
18	2	JMP3, JMP8	Header 2x1
19	2	J1, J2	eSata_Board_Connector
20	1	L1	HI1206N101R-00
21	1	P1	RAPC722
22	2	R1, R2	1M
23	1	R3	23.2k
24	1	R4	DNI
25	1	R5	150k
26	1	R6	64.9k
27	1	R7	13k
28	4	R8, R9, R10, R12	4.7k
29	1	R11	150
30	1	R24	150k_DNI
31	1	R25	0
32	1	U1	SN75LVCP600S
33	1	U2	REG104

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