Si5xx5x7-EVB

Evaluation Board for Si53x/55x/59x XOs/VCXOs

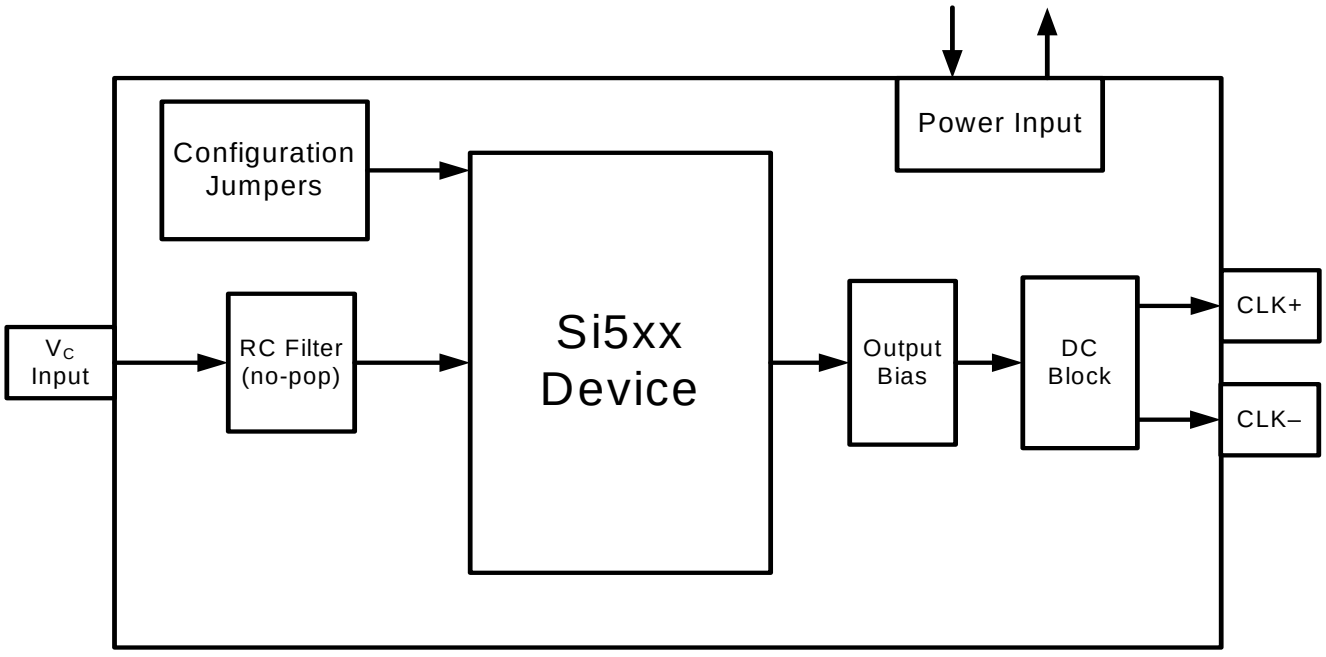
Description

This document describes the operation of the Silicon Laboratories Si5xx5x7-EVB evaluation board to evaluate both Silicon Laboratories' Si55x and Si595 VCXOs and Si53x and Si590/591 XOs. The Si53x/55x/59x devices use Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at high frequencies. The Si55x/Si53x/59x IC-based device is factory configurable for a wide variety of user specifications including frequency, supply voltage, output, and tuning slope. Specific configurations are factory programmed into the Si55x/Si53x/59x at time of shipment, thereby eliminating the long lead times associated with custom oscillators. Si55x/Si53x/59x samples should be ordered at the same time as the Si5xx5x7-EVB since the EVB does not come with the device. This allows end users maximum flexibility. Silicon Laboratories can solder down samples when ordering an EVB; please specify when ordering.

Features

- Evaluation of Silicon Laboratories' Si55x/53x/59x family
- AC-coupled differential output clocks
- Voltage control (V_C) input port (for Si55x/595 devices)
- Jumper selection for multi-frequency outputs
- Jumper selection for output enable

Functional Block Diagram



1. Functional Description

The Si5xx5x7-EVB provides access to all signals for configuring and operating the device. This board allows evaluation of the Si55x/595 VCXO device either by itself (open-loop) or within a prototype PLL (closed-loop). The performance of the Si53x/590/591 XO device can also be evaluated on this board (the Vc port is not used for XO devices).

Table 1. Jumper Control

Part Type	JP1	JP2	JP3	JP4
Si530	N/A	N/A	OE	N/A
Si531	N/A	N/A	N/A	OE
Si532	N/A	N/A	OE	Freq Sel
Si533	N/A	N/A	Freq Sel	OE
Si534	Freq Sel1	Freq Sel2	OE	N/A
Si550	N/A	N/A	OE	V_C
Si552	N/A	N/A	Freq Sel	V_C
Si554	Freq Sel1	Freq Sel2	OE	V_C
Si590	N/A	N/A	OE	N/A
Si591	N/A	N/A	N/A	OE
Si595	N/A	N/A	OE	V_C

Notes:
1. With jumper(s) installed, signal(s) are driven low.
2. With jumper(s) not installed, signal(s) are pulled high.

1.1. Power Supply

The Si55x/Si53x/59x devices support operation from nominal voltages of 1.8, 2.5, and 3.3 V. Review the device data sheet and part number for allowed configurations of output buffer type and device power supply.

1.2. Voltage Control for VCXOs

The voltage control (V_C) input of the Si55x/595 device is conveniently accessible through an SMA jack (J3) but can also be driven (and observed) through 100 mil-centered posts (JP4). For prototyping purposes, two 0603 solder pads are located near the device V_C input (R3 and C3). A traditional PLL might use these as a single-time-constant low-pass filter (RC filter). The EVB is shipped with a 0 Ω resistor soldered at R3; C3 is left open. The voltage control input is not used for XO devices.

1.3. Output Clock

Because the Si55x/Si53x/59x devices can support an LVPECL buffer type (in addition to LVDS and CMOS), pulldown resistors (R1 and R2) are available for proper output biasing. For LVPECL buffers, biasing can be achieved through a variety of equivalent circuits; the Si5xx5x7-EVB allows for 130 Ω pulldown resistors. After the output biasing, the high-speed outputs are dc-blocked for connection to differently biased inputs, such as standard test equipment or a phase detector EVB. Please review “1.4. Preparing the EVB” for non-LVPECL devices.

1.4. Preparing the EVB

By default, the evaluation board is set up to accept LVPECL configured devices. This configuration uses 130 Ω pull-down resistors to bias the LVPECL output stage. If an LVDS, CMOS, or CML based device is to be installed, the output biasing resistors, R1 and R2, should be removed.

2. Schematics

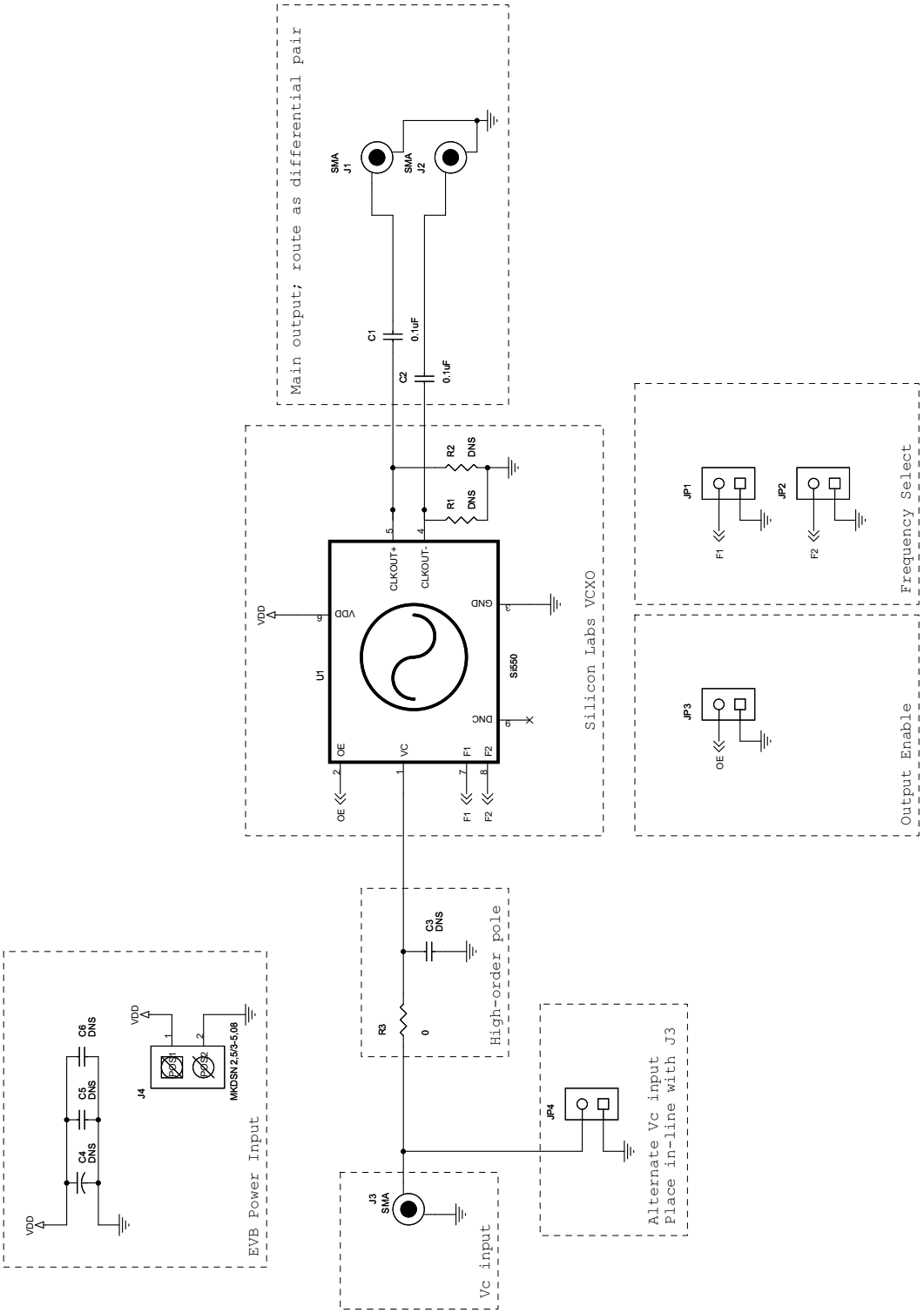


Figure 1. Si5xx5x7-EVB Schematic

3. Bill of Materials

Table 2. Si5xx5x7-EVB Bill of Materials

Item	Qty	Ref	Description	Mfr #	Mfr
1	2	C1,C2	CAP,SM,0.1 µF, 16 V,20%,X7R,0402	C0402X7R160-104KNE	Venkel
2	2	C5	CAP,SM,0.1 µF, 16 V,20%,X7R,0603	C0603X7R160-104KNE	Venkel
3	1	C4	CAP,SM,10 µF, 10 V,10%,TANTALUM,3216	TA010TCM106KAR	Venkel
4	1	C6	CAP,SM,100 pF, 50 V,10%,C0G,0603	C0603C0G500-101KNE	Venkel
5	4	JP1,JP2, JP3,JP4	CONN,HEADER,2X1	TSW-150-07-T-D or TSW-150-07-T-S	Samtec
6	3	J1,J2,J3	CONN,SMA SIDE MOUNT	901-10003	Amphenol
7	1	J4	CONN,POWER, 2 POSITION	1729018	Phoenix Contact
8	1	R3	RES,SM,0 Ω,0603	CR0603-16W-000T	Venkel
9	2	R1,R2	RES,SM,150,1%,0603	CR0603-16W-1500FT	Venkel
No Load					
11	1	C3	CAP,SM,0.1 µF, 16 V,20%,X7R,0603	C0603X7R160-104KNE	Venkel
10	1	U1	Si5xx - Not populated	Si5xx	Silicon Laboratories

4. Layout

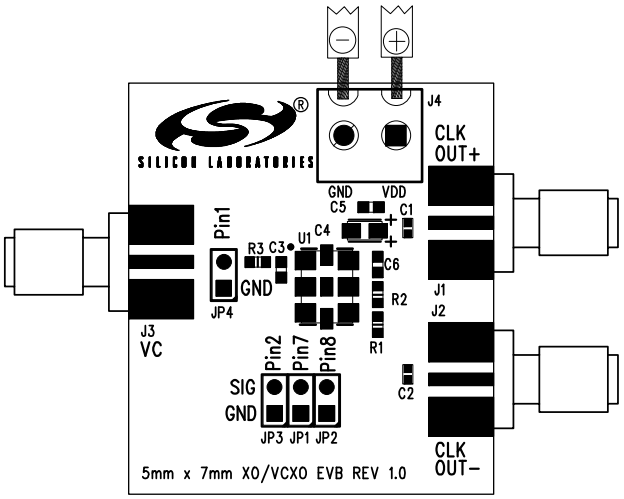


Figure 2. Assembly Drawing

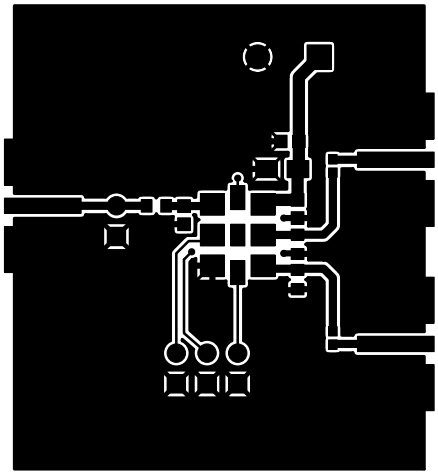


Figure 3. Layer 1 Primary

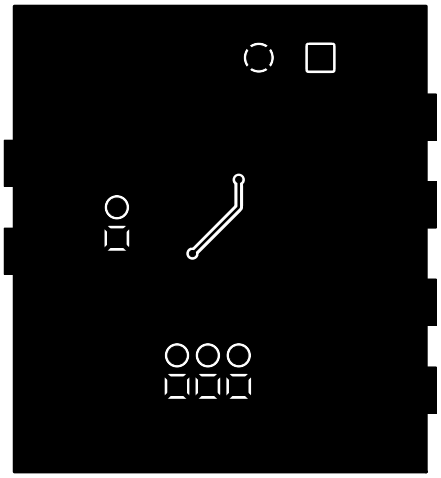


Figure 4. Layer 2 Secondary

Document Change List

Revision 0.13 to Revision 0.14

- Updated "Bill of Materials," on page 4.
- Updated Figure 2, “Assembly Drawing,” on page 5.

Revision 0.14 to Revision 0.2

- Changed Si5xx-EVB to Si5xx5x7-EVB.

Revision 0.2 to Revision 0.3

- Changed instances of Si53x/590/591, Si55x, and Si53x to Si53x/55x/59x throughout.
- Updated Table 1, “Jumper Control,” on page 2.

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com