AN12267

FXPS7xxx series pressure sensor self-test features

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Document information

Information	Content
Keywords	self test, digital barometric absolute pressure (DBAP), absolute pressure sensor, engine management, comfort seating, exhaust gas recirculation (EGR), media resistant, media compatible, serial peripheral interface (SPI)
Abstract	This document describes the diagnostic features present in the NXP DBAP series of sensors. This document is an addition to the information present in the product data sheets and describes the internal working mechanism of all the self-test modes. This application note describes the self-test procedures and presents the diagnostic details. For further information, refer to the safety manual as well as to other functional safety documentation available upon request from NXP.

Revision history

Rev	Date	Description
1	20181115	initial version

1 Introduction

This technical application note provides an overview of the self-test features of the FXPS7xxx digital barometric absolute pressure (DBAP) serial peripheral interface (SPI) based pressure sensors. The devices include analog and digital self-test features to verify the functionality of the transducer and signal chain.

The self-test features described in this application note assume that the user has reviewed the latest released data sheet for the applicable device and is familiar with the recommended application circuit and the register space definition. References to individual registers are made throughout this document and the definition for such registers is present in the product data sheet.

2 Applicable parts

Table 1. Applicable parts

Part number	Part name	Description
FXPS7115DS4T1	DBAP	40 kPa to 115 kPa SPI-based digital absolute pressure sensor
FXPS7250DS4T1	DBAP	20 kPa to 250 kPa SPI-based digital absolute pressure sensor
FXPS7400DS4T1	DBAP	20 kPa to 400 kPa SPI-based digital absolute pressure sensor
FXPS7550DS4T1	DBAP	20 kPa to 550 kPa SPI-based digital absolute pressure sensor

3 Self-test overview

The device includes analog and digital self-test functions to verify the functionality of the transducer and the signal chain. The self-test functions are selected by writing to the ST_CTRL[3:0] bits in the DSP_CFG_U5 register. The ST_CTRL bits determine the desired self test according to the description in the following sections.

Once the ENDINIT bit is set, the ST_CTRL bits are forced to 0000b. Future writes to the ST_CTRL bits are disabled until a device reset.

3.1 Startup P_{abs} common mode verification

When the P_{abs} common mode self test is selected, the ST_ACTIVE bit is set, the ST_ERROR is cleared, and the device begins an internal measurement of the common mode signal of the P cells and compares the result against a pre-determined limit. If the result exceeds the limit, the ST_ERROR bit is set.

The P_{abs} common mode self test repeats continuously every t_{ST_INIT} when the ST_CTRL bits are set to the specified value. Once the test is disabled, the ST_ERROR bit is updated with the final test result within t_{ST_INIT} of disabling the test. The ST_ACTIVE bit remains set until the final test result is reported.

Figure 1 shows an example of a user controlled self-test procedure.

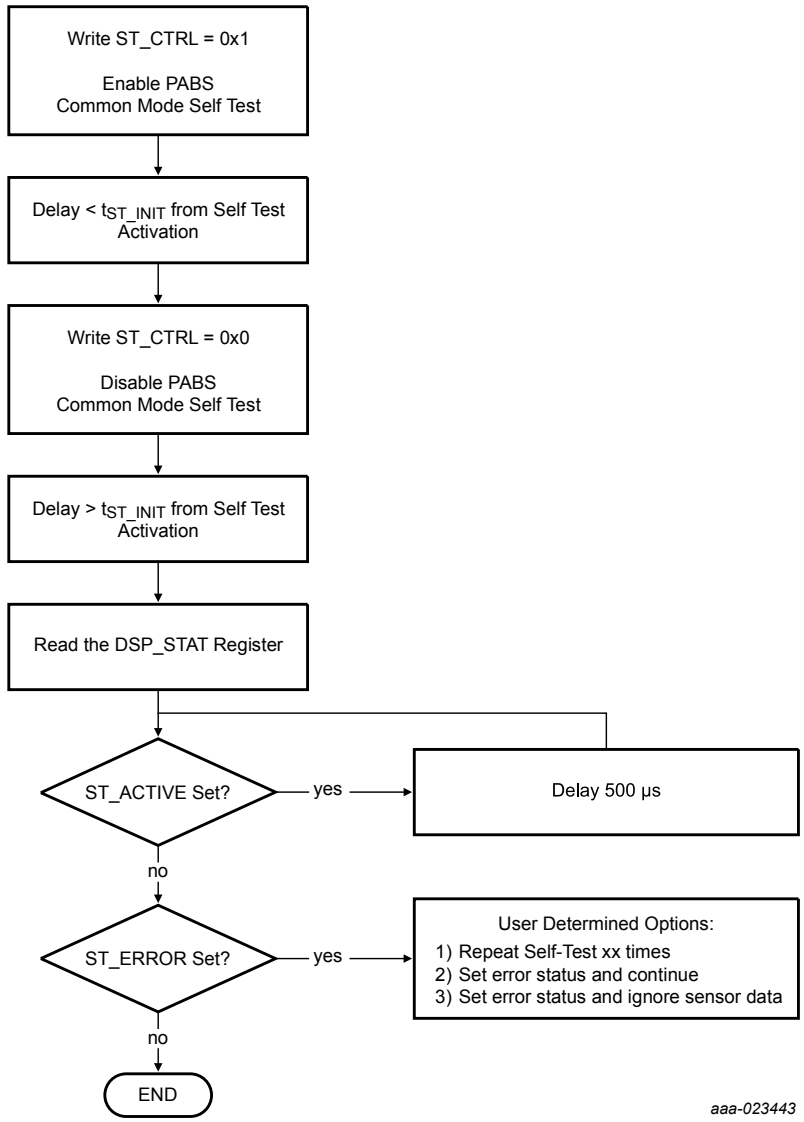

Figure 1. User initiated common mode self test

3.2 Startup digital self-test verification

Four unique fixed values can be forced at the output of the sync filter by writing to the ST_CTRL bits; see Table 2. The digital self-test values result in a constant value at the output of the signal chain. After a specified time, the SNS_DATAx_x register value can be verified against the values in Table 2. When any of these self-test functions are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 2. Self-test control register values for digital self test

ST_CTRL[3:0]				Function	SNS_DATAx_x register content
1	1	0	0	digital self test 1	0x8171
1	1	0	1	digital self test 2	0x6C95
1	1	1	0	digital self test 3	0x807A
1	1	1	1	digital self test 4	0x78AC

3.3 Startup sense data fixed value verification

Four unique fixed values can be forced to the SNS_DATAx_x registers by writing to the ST_CTRL bits; see Table 3. When any of these values are selected, the ST_ACTIVE bit is set. These signals can only be selected when the ENDINIT bit is not set.

Table 3. Self-test control bits for startup sense data fixed value verification

ST_CTRL[3:0]				Function	SNS_DATAx_x register content
0	1	0	0	digital signal processor (DSP) write to SNS_DATAx_x registers inhibited	0x0000
0	1	0	1	digital self test 2	0xAAAA
0	1	1	0	digital self test 3	0x5555
0	1	1	1	digital self test 4	0xFFFF

3.4 Complete self test

The next step is to complete some or all of the various self-test functions available in the device. Figure 2 shows an overview of an example recommended procedure for completing self test. Test repeats on failure are not shown in the diagrams. The user, based on the application, determines the number or test repeats for each test type. Typically test repeats are included at a minimum for the analog self-test procedures to provide immunity to potential misuse inputs that are common during startup.

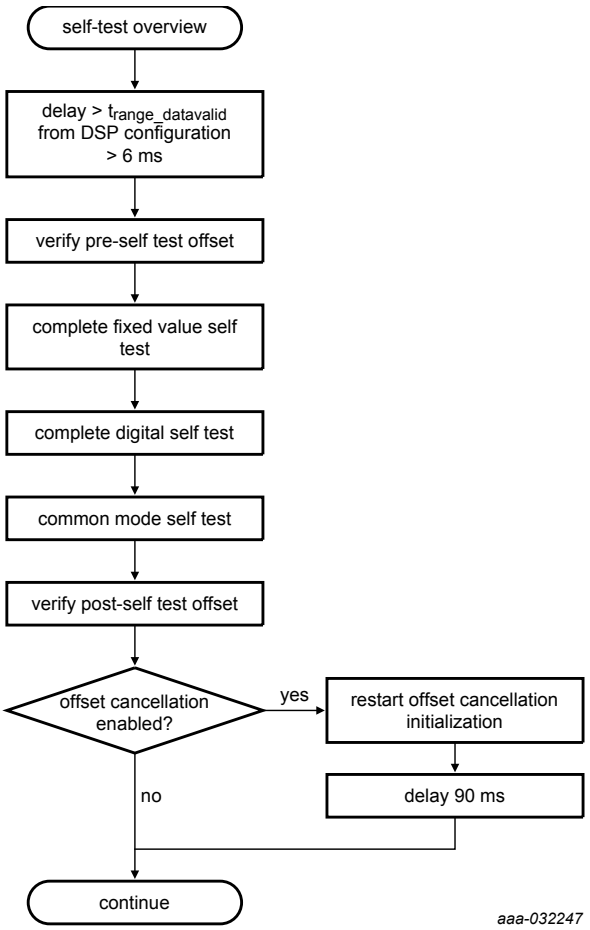

Figure 2. Complete self test

3.4.1 Complete fixed value self-test

The next step is to complete a fixed value self-test verification for each device. The purpose of the fixed value self-test is to confirm that the output data register and communication block have no stuck bit conditions. Figure 3 shows an example procedure for completing self-test with fixed values. Expected responses are included for each self-test request.

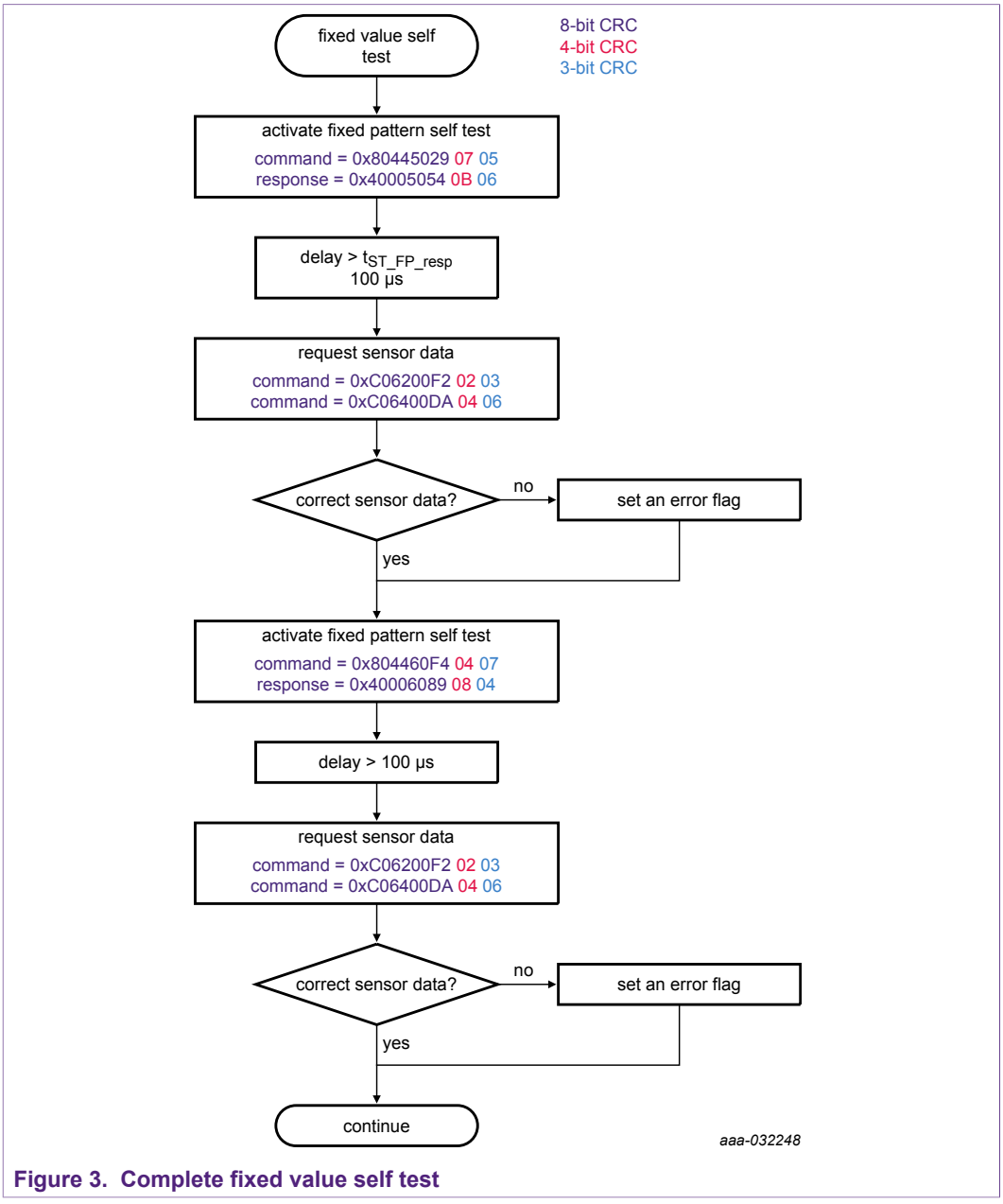

Figure 3. Complete fixed value self test

3.4.2 Complete pre-self test offset

The next step is to complete an offset verification. The purpose of the offset verification is to:

1. Verify the offset of the device and any change in offset before and after the self-test motion.
2. Capture the pre-self test offset that is subtracted from the measured self-test values during analog self-test.

The flowchart in Figure 4 shows an example procedure for capturing the sensor offset.

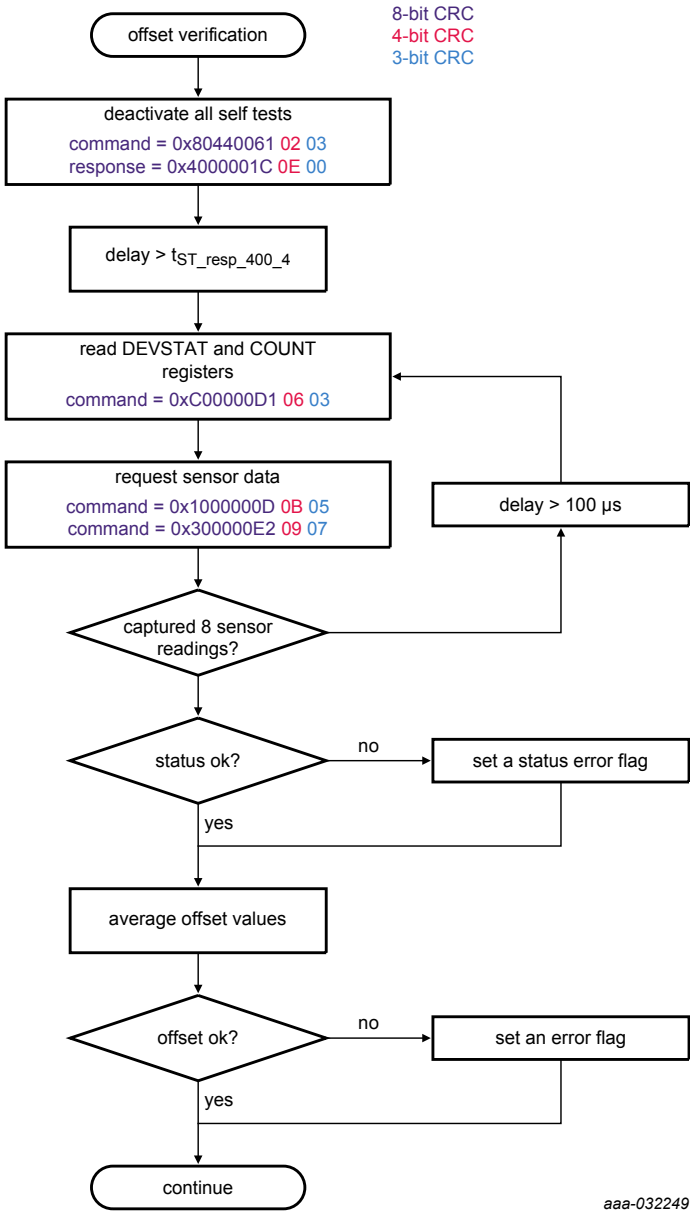

Figure 4. Pre-self test offset

3.4.3 Complete digital self test

The next step is to complete a digital self-test verification for each device. The purpose of the digital self test is to complete a more accurate verification of the digital signal chain. The digital self test forces a known value into the input of the digital signal chain. After a defined interval of time, dependent on the low-pass filter selected, the signal chain output can be verified against an expected value plus or minus a small tolerance. Figure 5 shows an example procedure for completing self test of one digital value (digital self test 0xC) and confirming the expected output value.

If offset cancellation is planned to be used, it is recommended to bypass the offset cancellation filter for digital self test to eliminate the effects of the filter on the digital self-test result. The procedure below includes offset cancellation bypass during digital self test.

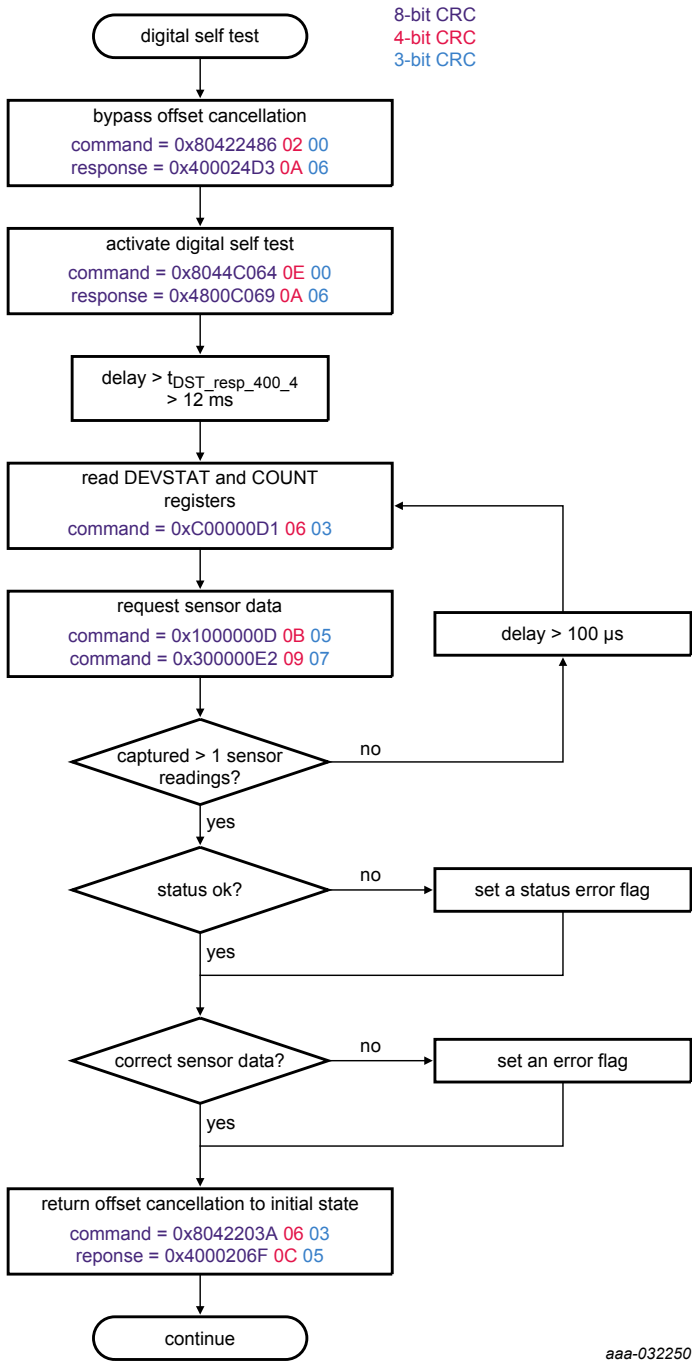

Figure 5. Digital self-test procedure

3.4.4 Complete common mode self test

The next step is to complete an offset and analog common mode self-test verification. The purpose of the analog self test is to:

1. Confirm the P cell health by monitoring the common mode signal of the two P cells implemented in the microelectromechanical system (MEMS) design.
2. Verify the sensitivity accuracy of the device. The FXPS7xxx devices contain multiple self-test capabilities and procedures that have different sensitivity accuracy verification capabilities.
3. Verify the offset of the device and any change in offset before and after the self-test motion.

The flowchart in Figure 6 shows an example analog self-test procedure for measuring common mode self-test values.

When sensor data is read for any of the analog self-test functions, the sensor data can be accessed either by using the sensor data request commands or by reading the SNS_DATAx_x registers directly. For some user gain settings, the analog self test results in a potential railed sensor data output via the sensor data request commands. For these test cases, the data must be read via the SNS_DATAx_x registers.

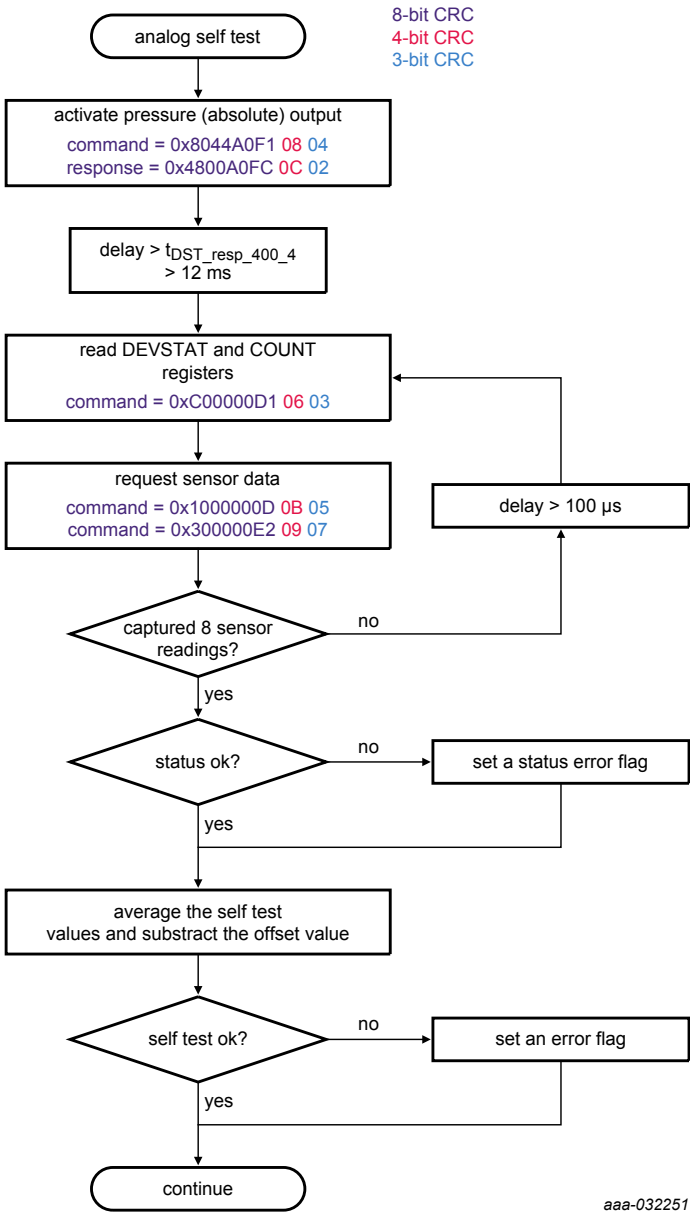

Figure 6. Common mode self-test procedure

4 Transition to normal mode

Once all self-test procedures are complete and verified, the system can transition the device from initialization to normal mode. This transition is done by setting the ENDINIT bit.

The typical time taken to complete all sensor self tests from power-on reset (POR) is ~ 54 ms.

5 Abbreviations

Table 4. Abbreviations

Acronym	Description
ADC	analog-to-digital converter
Analog self test	A method to test the analog signal chain by simulating the transducer input and measuring the device output.
DBAP	digital barometric absolute pressure
Digital self test	A method to test the digital portion of the pressure signal chain by forcing a value or a sequence of values at the output of the ADC and measuring the device output.
DSP	digital signal processor
EGR	exhaust gas recirculation
MEMS	microelectromechanical system
MISO	master input slave output
MOSI	master output slave input
POR	power-on reset
SCLK	SPI device clock
SPI	serial peripheral interface; a full-duplex, synchronous serial interface; the FXPS7xxx devices operate of a 32-bit implementation of SPI
SS_B	slave select bar, active LOW signal from the bus master to select the device
ST	self test

6 References

[1] **Product summary page** — http://www.nxp.com/FXPS7xxx

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